A Miniature Microcontroller Curve Tracing Circuit for Space Flight Testing Transistors

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This paper describes a novel miniature microcontroller based curve tracing circuit, which was designed to monitor the environmental effects on SiC JFET device performance, while exposed to the Low Earth Orbit environment onboard the ISS as a resident experiment on the 7th Materials on the International Space Station Experiment (MISSE7). Specifically the microcontroller circuit was designed to operate autonomously and was flown on the external structure of the International Space Station (ISS) for over a year. This curve tracing circuit is capable of measuring current vs. voltage (I-V) characteristics of transistors and diodes. The circuit is current limited for low current devices and is specifically designed to test high temperature, high drain-to-source resistance Silicon Carbide Junction Field Effect Transistors (SiC JFETs). The results of each I-V data set are transmitted serially to an external telemetered communication interface. This paper discusses the circuit architecture, its design, and presents example results.

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I. Introduction

The International Space Station (ISS) is currently being used for in-situ testing of materials and devices in the low earth orbit (LEO) environment[1]. As a test facility, the ISS has many challenging environments effects such as thermal profiles, atomic oxygen presence, vacuum, and radiation. Developers of materials and devices have found great value in evaluating performance in-situ using the ISS operating environment. The I-V curve tracing circuit in this paper was designed to support an endurance test experiment of Silicon Carbide Junction Field Effect Transistors (SiC JFETs) in the ISS environment. The experiment consisted of two SiC JFETs as the devices under test (DUTs); one in experimental high temperature packaging[2] and one in a commercial room temperature package. The measurements performed are drain-to-source current (I_{DS}) vs. drain-to-source voltage (V_{DS}) curves at various gate-to-source voltages (V_{GS}).

The test platform onboard the ISS is a Materials on the International Space Station Experiment (MISSE) Passive Experiment Container (PEC). This suitcase like container is shown in Figure 1. Figure 1 (A) shows the MISSE7 PEC mounted on an Express Logistics Carrier on the ISS. Figure 1 (B) shows the many types of experiments mounted on the PEC with the SiC JFET experiment outlined. The experiment was contained in a 2 mm thick Aluminum box that provides some radiation shielding and exposed the electronics to a predicted yearly total ionizing dose of approximately 170 Rad Si[3]. The MISSE7 experiment set provided +5 VDC power and a serial communications interface for telemetry data. The MISSE7 PEC also has heaters onboard to maintain the temperature of the electronics to a range of −40°C to +50°C for survivability.

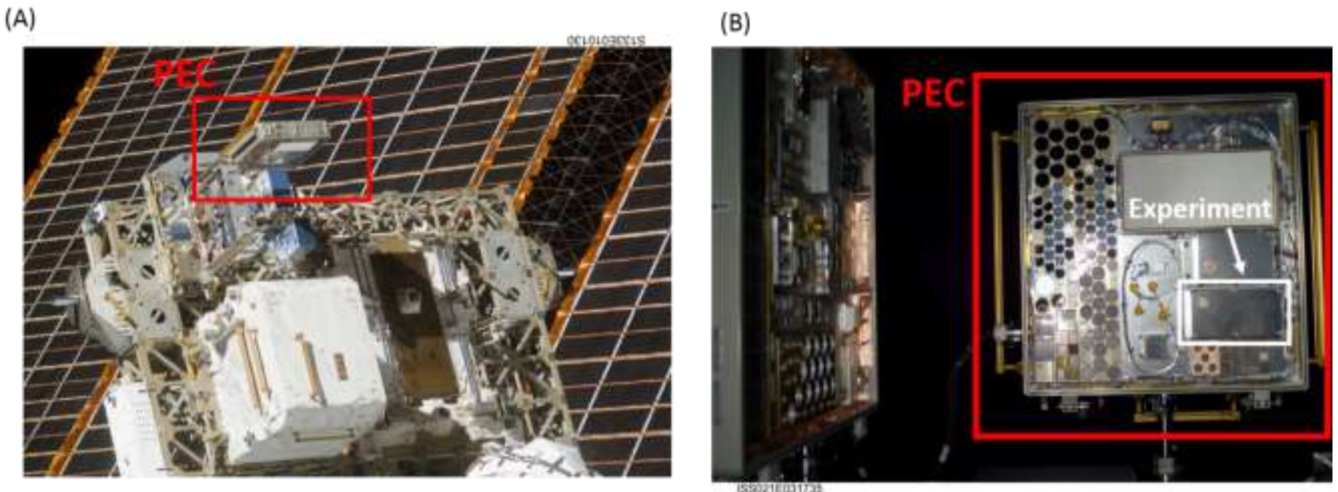

FIG 1 (A) Seventh Materials on the International Space Station (MISSE7) Passive Experiment Container (PEC) mounted the Express Logistics Carrier (ELC). The experiment is shown outlined in (B).

The SiC JFETs were developed at the NASA Glenn Research Center and are capable of surviving harsh environments with a temperature range of −125°C to +600°C. The transistors are small signal JFETS used within instrumentation circuits such as amplifiers and digital logic gates[4]. These transistors have been demonstrated operating for extended periods of time (>10,000 hours) at 500°C and in digital logic ICs operating for over 3,000 hours at 500°C[5]. The SiC JFETs under test have a large drain to source channel resistance greater than 10 KΩ when fully on. These JFETs also need a V_{GS} of −10 V or greater to fully turn off the transistors, and must maintain a zero to negative gate bias so as not to damage the pn junction of the JFET gate. In addition, V_{DS} needs to be near +15 V to reach the saturated drain-to-source current (I_{DSS}). As only a +5 VDC power supply was provided to experimenters, ±15 V supplies needed to be designed and incorporated into the experiment circuit to generate the needed V_{GS} and V_{DS} voltages.

The physical layout for the MISSE7 experiment set allotted a footprint area of approximately 10 cm x 20 cm for the SiC JFET experiment. The experiment circuit board also supported electronics for two additional experiments: the atomic oxygen fluence monitor and a gas sensor. Although these experiments will not be discussed in this paper, they added to the size constraints of the overall design. Since two transistors were under test, it was decided to construct two independent test circuits to include the ±15 V supplies for each test circuit. This allowed redundant JFET testing, since both circuits have similar JFETs with different packaging. In the event of a single circuit failure, some data would be recovered from the redundant circuit.

The physical size constraints of the experiment necessitated a new circuit design for transistor curve tracing, which miniaturizes the curve tracing function. This paper will present a novel miniature standalone transistor curve trace circuit that operates from a single DC voltage source and includes all needed support circuitry. The circuit uses selected integrated

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circuits with a successful ISS flight history, and utilizes a novel load configuration to account for the shortcomings of these components. Designed to use minimal physical space and mass, it is ideal for a space flight test. The circuit enabled the first space flight test of high temperature SiC JFETs while successfully operating on board the International Space Station from November 2009 to May 2011.

II. Curve Tracing Circuit

A curve tracing circuit exercises an electronic device through its operational region. This is done by placing a variable electrical load either in series or parallel with the Device Under Test (DUT). By varying the electrical load, the DUT is swept through varying operating regions. The variable load can consist of a bank of resistors, an active power source or a transistor as shown in Figure 2. Resistor banks being the simplest form of implementation, are passive loads that provide fixed data points of operation, as shown in Figure 2 (A). Unfortunately these circuits increase footprint with the number of desired data points. As well as increased size, these circuits are also not flexible due to the resistors being fixed values. Active power sources or sinks such as the voltage controlled current source shown in Figure 2 (B) are flexible, but use additional power, take up space and can potentially damage the DUT. The third option, the MOSFET, is an ideal choice as a passive load that acts as a variable resistor with system capability limiting resolution in modulating the DUTs gate voltage shown in Figure 2 (C).

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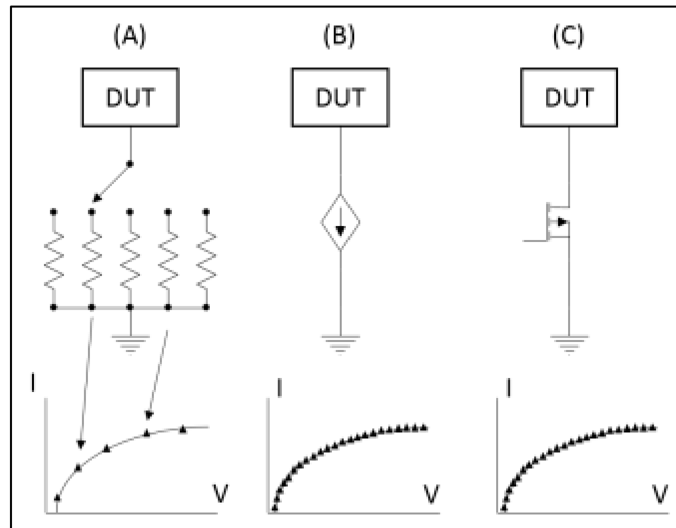

FIG 2. Variable load options for performing a curve trace on the Device Under Test (DUT). (A) shows a resistor bank, where a resistor can be switched in for each point in the curve. (B) shows a voltage controlled current source, where the number of points on the curve is determined by the resolution of the source and controller voltage. (C) shows a MOSFET acting as voltage controlled variable resistor, where the number of points on the curve is determined by the resolution of the controller voltage.

I-V curve tracing circuits for in-situ device characterization are not new, a number of solar cell I-V curve tracing circuits have been demonstrated on flight platforms. Solar cell I-V curve tracing circuits are needed to characterize device

performance degradation in the space environment, and have been demonstrated on MISSE5, which represents the state-of-the-art in space photovoltaic cell curve tracing measurements[5]. MISSE5 used a MOSFET as the load with solar cells as the DUT. In addition to the choice of operating electronic load for the curve trace circuit, the DUT itself may also add complexity to the curve trace circuit. For instance the nature of two-port solar cells differ from transistors in that they are two port devices as opposed to three port and require the generated power to be dissipated, which is not required for transistors. The third port of the transistor complicates the design by adding another port of the DUT to control. Transistor I-V curve tracing circuits have been demonstrated in the laboratory, but these circuits are large because they often depend on external laboratory power supplies and signal generators[7,8].

A. Design Considerations

A number of constraints were taken into consideration during the circuit design. The radiation environment dictated most choices in the design. Component selection was the primary method of mitigating radiation effects on the circuit coupled with some simple design rules. The authors had success with an extended flight of solar cell I-V circuitry on MISSE5 and these same circuit components were chosen for the design of this experiment. The central components of this design were the Silicon Laboratories C8051F121 microcontroller and the LT1013/1014 operational amplifiers. The microcontroller has onboard digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) with multiplexers to provide numerous inputs[9]. The LT1013 op amp is a precision amplifier based on bipolar technology[10] that was shown to perform well as a component of the Forward Technology Solar Cell Experiment instrumentation circuitry during extended an extended flight on the ISS [11,12].

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Together with the chosen components, two design rules were employed in the op amp measurement circuitry. These rules were used to limit errors that might be introduced from increasing bias currents due to radiation damage, one of the major concerns for bipolar linear circuits in a low dose radiation environment[13]. The rules were as follows:

1. Minimize resistance values in the op amp gain circuits.
2. Balance Thevenin resistances as looking out of any op amp input.

Rule 1 will minimize voltage offsets generated by increased bias currents flowing through gain resistors. For instance if a 1 kΩ resistor is used in place a 10 kΩ resistor, then for the same current flowing through those resistors, 1/10th the offset voltage will be generated with the smaller resistor compared to the larger. Rule 2 will minimize input offset voltage errors due to increased bias currents. If the resistances are balanced at the inputs, then for any increase in bias current at the inputs, the offset voltages will shift by equal amounts, assuming the bias current increases equally for both inputs.

The selection of the LT1013/1014 op amp did provide one drawback in that its output voltage swing is not rail to rail (+ Supply to – Supply) but instead as the data sheet lists can be as low as ±12.5 V when used with ±15 V supplies. This becomes an issue when looking at the various circuit topologies that may be constructed using a JFET as the DUT and a MOSFET as the load (Figure 3). Various curve tracing topologies are illustrated: (A), (B), and (C) are series and (D) is a shunt. Figure 3 shows three basic types of circuit topologies: (A) and (B) show a series load sitting above the DUT and (C) shows a series load sitting under the DUT. Each of these series circuits ((A), (B),and (C)) requires one of the gate voltages, either the Load in (A) and (B), or the DUT in (C) to be driven to the +V supply rail: to fully turn on the Load in (A), to fully turn off the load in (B), and to fully turn on the DUT in (C). With the limited output swing of the LT1013/1014, either the DUT will not be tested over the full V_{DS} range of the positive supply rail, or the DUT will not be tested over the full range of V_{GS}. While rail-to-rail operational amplifiers are available that can overcome this output voltage swing limit, an alternative topology will also work. This is shown in (D) of Figure 3. In this configuration the load is in parallel with the DUT and acts as a shunt. The load MOSFET controls the voltage across the DUT by acting as a voltage controlled resistor. One drawback of this configuration is when the load is fully turned on, its resistance is in the mΩs, which can lead to excessive current. This in turn leads to the need of a current limiting resistor. The current limiting resistor will also limit the maximum V_{DS}, but with small I_{DSS} transistors such as the SiC JFETs, the maximum V_{DS} is closer to the supply rail compared to any of the series configurations. The maximum span of V_{DS} needs to be balanced with acceptable supply current.

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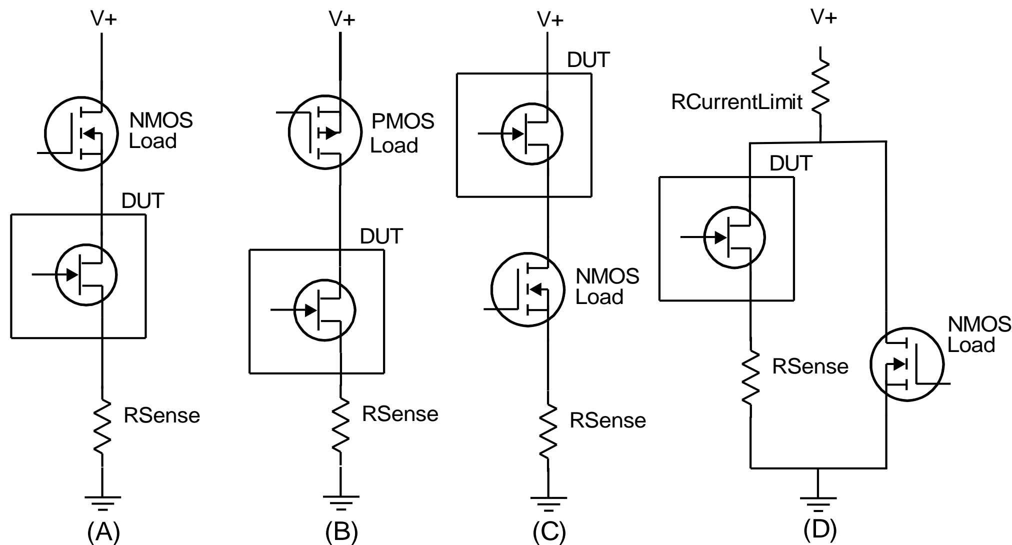

FIG 3. Various curve tracing topologies. (A), (B), and (C) are series and (D) is a shunt

A simplified schematic diagram showing the curve tracing circuit from a systems view is shown in Figure 4. Microcontroller power is provided by a 3.3 V low drop out linear regulator. The microcontroller has two onboard 12-bit DACs and two onboard ADCs, a 12-bit and 8-bit respectively. Additionally, each ADC has a built in multiplexer, allowing

each ADC to make measurements at 8 input pins. The microcontroller contains an internal voltage reference of 2.4 V for its analog components, which defines the full-scale measurement voltage. The 8-bit ADC uses the +3.3 V supply voltage of the microcontroller as its reference, allowing a larger measurement range but less resolution. These references give 586 μV resolution step for the 12-bit components and 12.9 mV resolution step for the 8-bit ADC. The 12-bit ADC also has a built in temperature sensor attached to its multiplexer, so the board temperature can be sampled at the time of a curve.

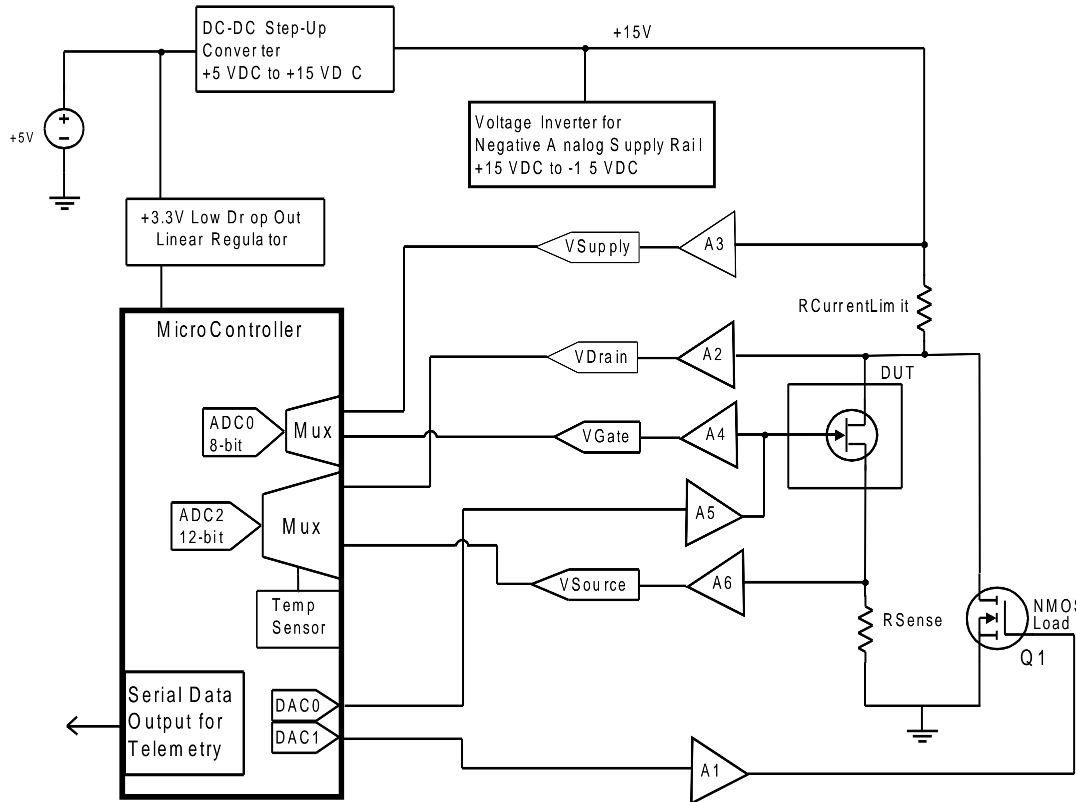

FIG 4. Diagram of circuit to perform curve tracing of Silicon Carbide Junction Field Effect Transistor (SiC JFET) as the Device Under Test (DUT)

The circuit operates by sweeping two control voltages in the circuit. The first is the gate voltage of the DUT (V_{Gate}) or SiC JFET and is controlled by the digital-to-analog converter zero (DAC0) through amplifier (A5). The second is the drain voltage of the DUT (V_{Drain}) and is controlled by varying the NMOSFET Load (Q1s) channel resistance. So V_{Drain} is controlled by the voltage at the gate of the Q1 from DAC1 through amplifier (A1).

The circuit is capable of making four voltage measurements with the respective ADC:

1. DUT Drain Voltage (V_{Drain} in Figure 4), 12-bit ADC
2. DUT Source Voltage (V_{source} in Figure 4), 12-bit ADC
3. DUT Gate Voltage (V_{Gate} in Figure 4), 8-bit ADC

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4. The circuit Supply voltage (V_{supply} in Figure 4), 8-bit ADC

Each of the measured voltages is amplified as shown in Figure 4. The amplifiers provide a corresponding gain, a high impedance load to the circuit being measured, and a low impedance driver into the ADC.

The sweep of V_{Gate} is controlled by DAC0 through amplifier A5. A5 is an inverting amplifier to provide the negative gate voltage needed to turn off the DUT. The DACs onboard the microcontroller have a maximum output value of +2.4 V (limited by the onboard voltage reference). This necessitates the need for an amplifier to multiply the DAC0 output voltage by a factor of −6 times to generate a close to full-scale negative voltage at the gate of the DUT (−15 VDC) to fully turn off the DUT.

A software control loop is implemented to guarantee V_{Gate} is set correctly. Using closed loop software control of V_{Gate}, the controller is able to monitor the voltage at the gate and log the actual value. This is in contrast to open loop control where the microcontroller would write a value to the DAC from a look-up table and have no feedback from the current voltage reading at the gate. Monitoring V_{Gate} during closed-loop control allows logging and telemetering of V_{Gate} and can be used to show the circuit is operating correctly.

The software feedback loop algorithm used to set the control voltages is shown in the flow chart of Figure 5. The algorithm consists of a binary search within the DAC output range. The search is implemented by stepping through each of the 12 bits of the DACs range, starting by writing the most significant bit of the DAC (or half the full scale). Once the DAC value is written, the controlled value ($V_{Drain,}$ V_{Gate}) is then sampled by the ADC 100 times and averaged to yield *CurrentValue*. If *CurrentValue* is greater than the requested value, nothing is done, but when the *CurrentValue* is less than the requested value, the value of the current DAC bit is added to a temporary variable, "Temp" in the flowchart. All successive DAC bits, as they are stepped through are added to this temporary variable, producing the final DAC value. After the final, or 12th iteration of this loop, the *CurrentValue* written to the DAC leaves the controlled value within one least significant bit (LSB) of the requested value.

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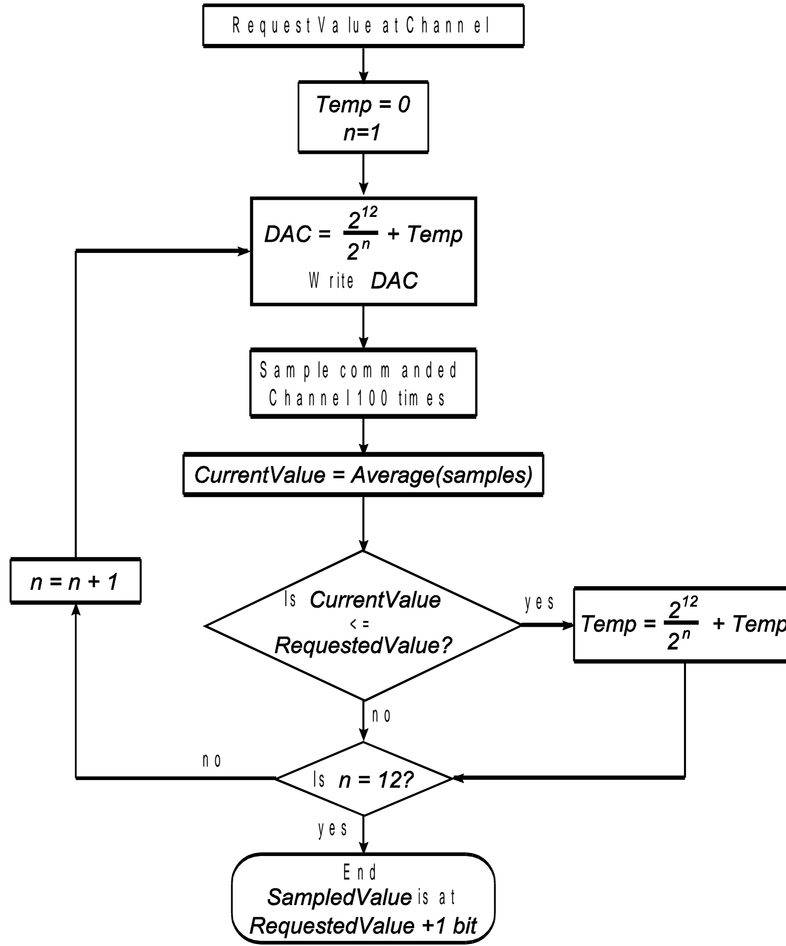

FIG 5. Flow Chart of closed loop control of commanded circuit variables.

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A V_{Drain} sweep is performed similar to that of the V_{Gate}, but is controlled by current steering through Q1. As the gate voltage of Q1 is changed, the channel resistance of Q1 ($R_{DS,Q1}$) changes, thus the current flowing through Q1 is varied. This current flowing through Q1 generates the drain voltage (V_{Drain}) by varying the resistance divider between $R_{CurrentLimit}$ and the parallel combination of $R_{DS,DUT}$ (the resistance of the DUT from Drain to Source) and $R_{DS,Q1}$ according to the equation (1):

$$V_{DRAIN} = V_{SUPPLY} \times \left(\frac{R_{DS,DUT} || R_{DS,Q1}}{R_{DS,DUT} || R_{DS,Q1} + R_{CurrentLimit}} \right). \qquad (1)$$

This equation is non-linear and $R_{DS,DUT}$ is dependent on the voltage between its gate to source (V_{GS}) and temperature, which can fluctuate over 50 °C. R_{Sense} is omitted from equation (1) because it is much smaller than $R_{DS,DUT}$, 10Ω compared to over 10kΩ, the voltage across R_{Sense} is also omitted for that reason. The complexity of these relationships makes necessary the need for closed loop control of V_{Drain}, also using the algorithm described in Figure 5. V_{Drain} is sampled while DAC1 writes to the gate of Q1 through amplifier A1. Also to note, since the temperature of the environment was only controlled to a survival range, no attempt was made to compensate for temperature drift, instead the temperature was sampled at the time of the curve and recorded as part of the curve data set.

The drain to source current flowing the DUT (I_{DS}) is derived from the sense Resistor (R_{Sense}) and the source voltage (V_{Source}) using Ohms law:

$$I_{DS} = \frac{VSource}{Rsense}\,. \qquad (2)$$

B. Circuit Description

A schematic for the complete curve tracing circuit is shown in Figures 6 and 7. Figure 6 demonstrates the corresponding power circuit containing the +5 VDC to +15 VDC boost converter and +15 VDC to −15 VDC voltage inverter, and Figure 7 shows the curve tracing load and measurement circuits. The boost converter needed to generate +15 VDC is made up of integrated circuit (IC) U2 and the surrounding parts in the left side of Figure 6: Q2A/Q2B, Q3, L1, D1, R5, R11, R16, R12, and R7. The +15 VDC supply is connected to the positive supplies for operational amplifiers U3A and U3B. The +15 VDC to −15 VDC voltage inversion circuit is shown in the right half of Figure 6, made up of Q4A, Q4B, Q5, Q2B, C10, C11, D3, D4, D5, D6, and the surrounding resistors. The circuit is a common charge transfer voltage inversion circuit, charging C10 to the +15 VDC supply rail through the diode D5. Then connecting the positive lead of C10 to ground, generating −15 VDC on the negative lead of C10, which shows up on the negative lead of C11 by the current flowing through D6. The negative voltage across C11 provides the −15 VDC rail to the operational amplifiers U3A and U3B. The voltage inverting circuit is driven by two non-overlapping clocking signals provided by programmable counter arrays within the microcontroller, named VInv_CLK and not_Vinv_CLK, controlling the direction of current through Q4B and D5, then Q4A and D6. Zener diodes D3 and D4 provide voltage transient protection to the microcontroller outputs.

Because this curve tracing circuit is duplicated twice on the printed circuit board, the option to shut down this circuit is provided by the microcontroller JFET_EN signal to minimize power consumption. JFET_EN is connected to the enable pin of U2, disabling the +15 VDC, and the gate of MOSFET Q1B, disabling the voltage inverter.

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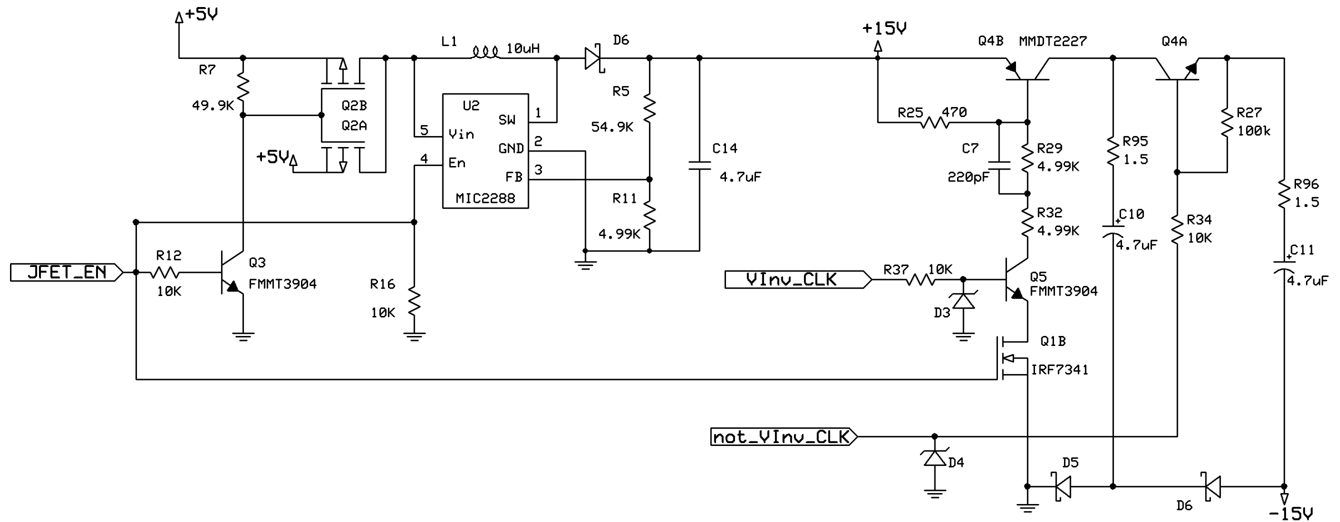

FIG 6. Schematic of Curve tracing circuit +5 VDC to +15 VDC boost converter, and +15VDC to −15VDC voltage inverter.

Figure 7 shows the curve tracing load and measurement circuit schematic. Op amp U3A and its associated resistor network amplifies the DAC0 signal with a gain factor of −6 times to drive the DUT gate. U3B samples the gate voltage and attenuates the DUT gate voltage by a factor of −6 times, (or provides a gain of −1/6 times) to provide the JFET_Gate signal to the 8-bit ADC. U3A and U3B provide the loop to control the DUT gate voltage. One of the features of the DUT gate circuitry is the path to ground: R18 and R23. During power down, each of the DUT terminals should have a path to ground, allowing any charge buildup to have a discharge path so the DUT will not be damaged if unbiased. U3A and U3B are the only op amps powered by the ±15 VDC supplies, all others use +5 VDC. U1A samples the +15 VDC supply, attenuates by a factor of 1/6 times and provides that voltage (V_{Supply}) to the 8-bit ADC. U1B samples the DUT Drain voltage, attenuates it by a factor of 1/6 times and provides V_{Drain} to the 12-bit ADC. U1C samples the DUT source voltage generated by the DUT drain current (I_{DS}) flowing through a 10 Ω R_{Sense}, and provides a gain of 69 times. This voltage labeled V_{Source} in the schematic is sampled by the 12-bit ADC and is used to derive I_{DS}. The final op amp U1D provides a gain of 1.5 times to the DAC1 output to drive the gate of the current shunt NMOSFET Q1.

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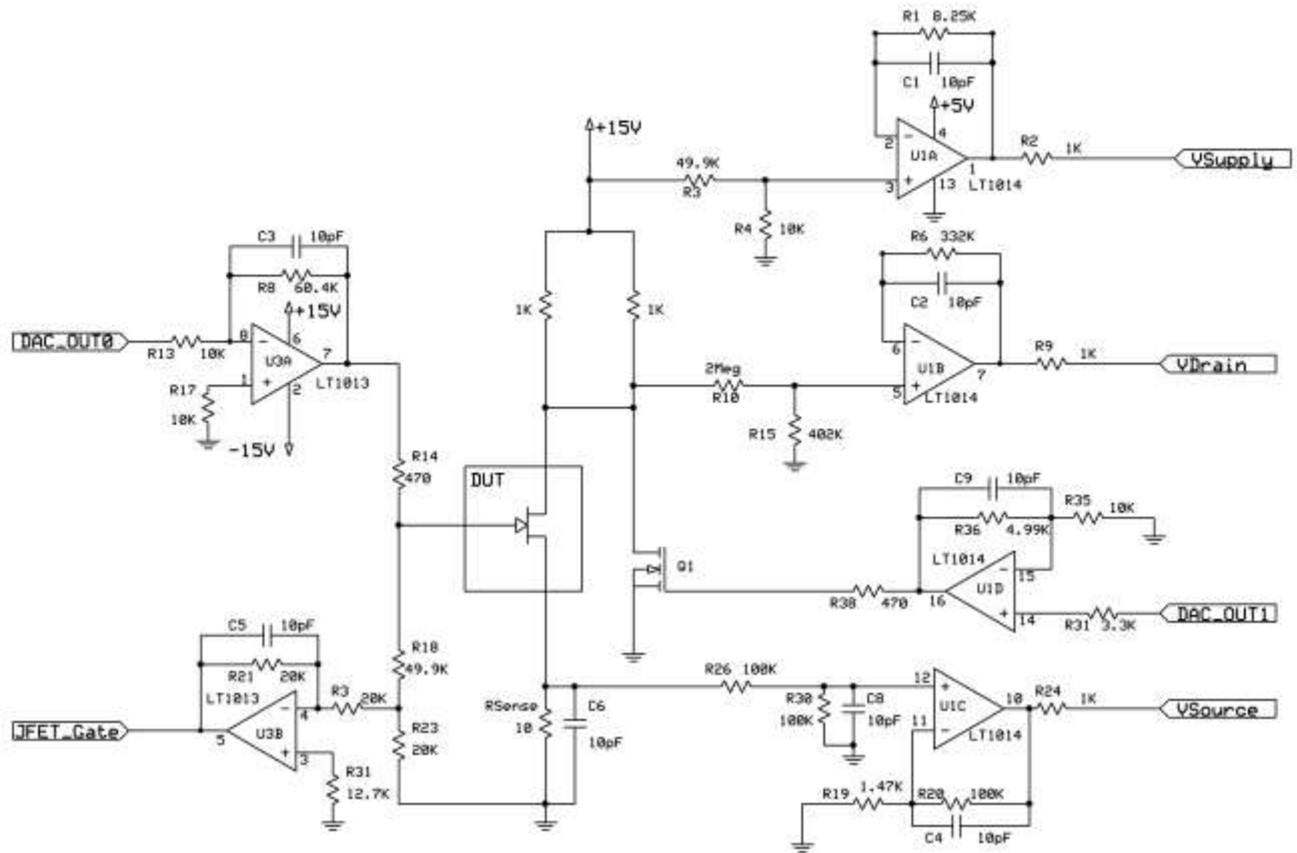

FIG 7. Schematic of curve tracing circuit.

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III. Results

Figure 8 shows an example curve trace of the room temperature packaged SiC JFET by the miniature circuit in comparison with the laboratory source measurement units, both taken at room temperature. In red are curve traces taken by laboratory source measurement units prior to integration into the flight circuit board. The blue traces show the curves taken by the miniaturized flight curve trace circuit during preflight tests. These curves are from the room temperature packaged SiC JFET shown in Figure 9. Included in the curve data set are the gate voltages shown in the legend of Figure 8 and the circuit board temperature with other housekeeping data. There is a disagreement between the miniature curve tracer and the commercial units of approximately 2% for the max I_{DS} or $V_{GS} = 0$ curve. All resistors used in the design have a one percent tolerance which will introduce some error into the measurements. This discrepancy may also be attributed to added resistance from the conductive epoxy used to connect the transistor leads to the circuit board traces and the epoxy used to fasten the transistor package to the circuit board and encase the transistor leads.

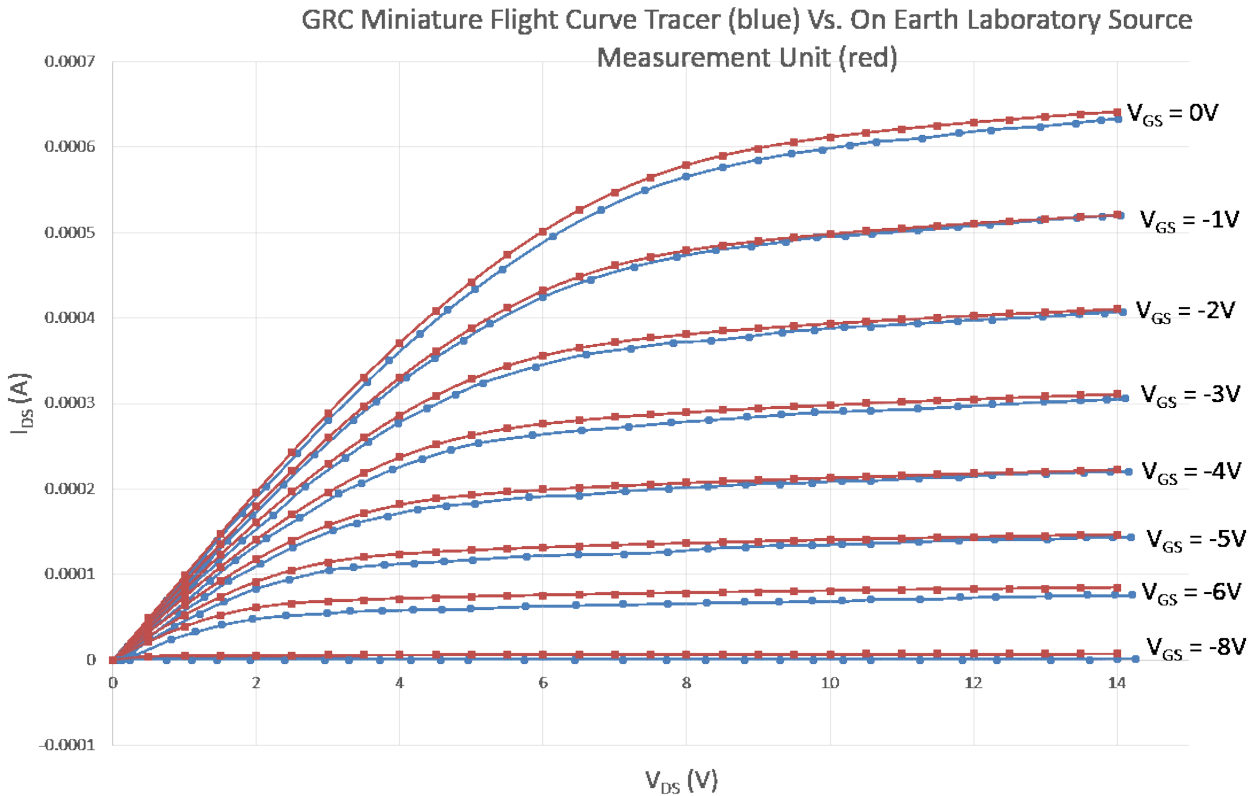

FIG 8. Plot of the Miniature curve trace circuit outputs (blue) and laboratory source measurement units performing curve traces (red) on the same room temperature packaged SiC JFET transistor. Drain-to-Source Current (I_{DS}) vs. Drain to Source Voltage (V_{DS}) at varying Gate to Source Voltages (V_{GS}).

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No performance degradation of the JFETS was seen during the flight test[14]. Experiment data was sampled hourly when power was applied and transmitted over a serial link to the MISSE7 Communications Interface Board, which handled all telemetry operations. The circuit successfully operated on orbit from November 2009 until its return to earth in May 2011. While the circuit operated successfully, one issue was identified during the flight period. The circuit's −15 VDC supply would not operate fully at lower temperatures, (temperatures below 16°C). There was a correlation in the maximum V_{GS} output voltage and temperature, where the maximum voltage would fall with temperature. This was due to the bipolar junction transistors used in the voltage inversion circuit, where the current gain decreases with temperature. This was verified post flight and on the flight back up hardware. The correction to this problem is to decrease the biasing resistors, so more current will flow. While this error did not allow the circuit to perform all the gate voltage sweeps, the circuit always allowed the sweep at ~V_{GS}=0.

A photograph of the flight circuit board is shown in Figure 9. The flight circuit board contains two complete curve tracing circuits, one to support the high temperature packaged JFET and the other the room temperature packaged JFET, both controlled by a single microcontroller. The circuit board is much larger due to the support of two additional experiments not

discussed. Each curve tracing circuit requires less than 32.3 cm^2 board area, allowing for multiple independent circuits to be used on a single small printed circuit board. This small footprint enables in-situ testing of devices in variety of environments.

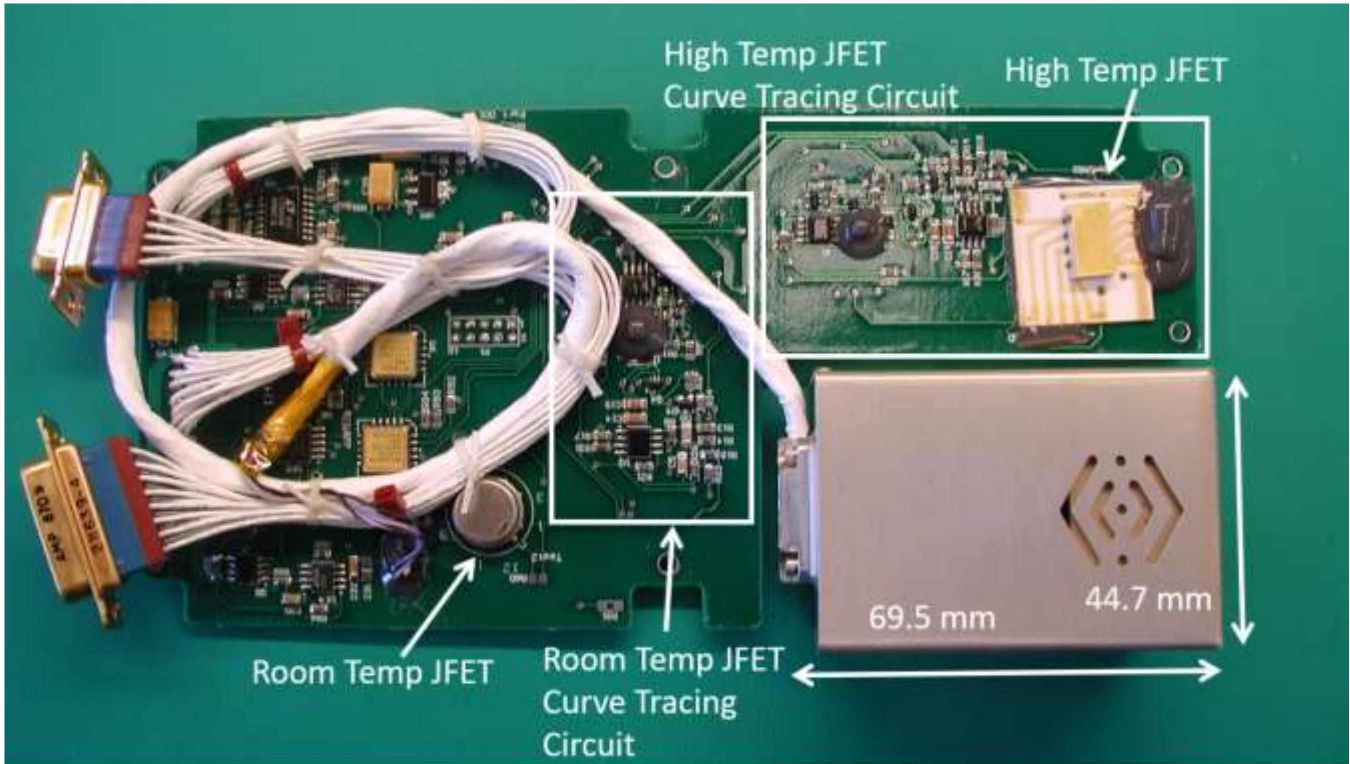

FIG 9. Photograph of flight circuit board incorporating two JFET transistor curve tracing circuits. The microcontroller is mounted on the bottom of the printed circuit board and is not shown in the photograph.

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IV. Conclusion

A novel miniature microcontroller based curve tracing circuit was designed to enable a flight test of SiC JEFT transistors. The circuit was successfully flown and operated on the exterior of the International Space Station for over a year, periodically characterizing Silicon Carbide JFETs. There was an issue with the negative voltage supply circuitry that affected circuit performance in temperatures below 16°C. The cause of this issue was identified as low bias current in the negative supply circuit and it is noteworthy to highlight that this not damage the circuit nor the Devices Under Test. The described circuit uses minimal space and mass and it is ideal for recurring space flight experiments. Even though this circuit was designed for characterizing JFETs, the circuit topology is applicable for MOSFETs, Diodes, and BJTs with minor modifications.

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(A)

S133E010130

PEC

CTC-3

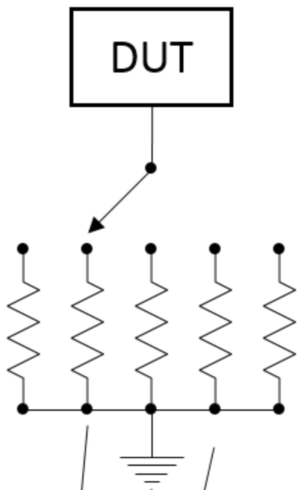
(B)

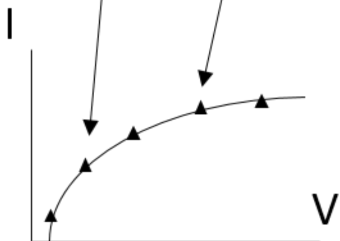
PEC

Experiment

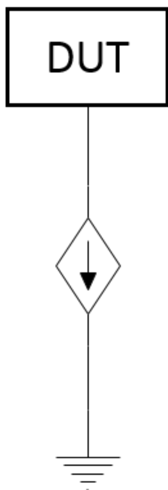
ISS021E031735

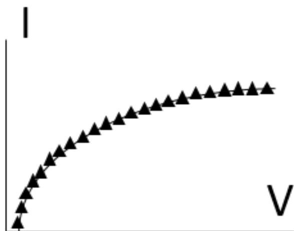
(A)



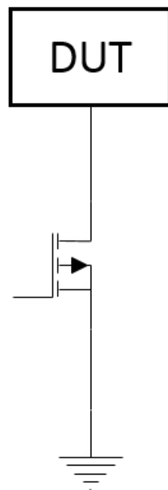


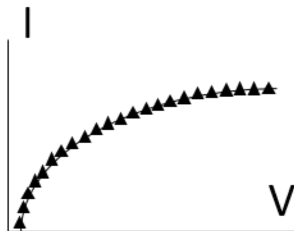
(B)



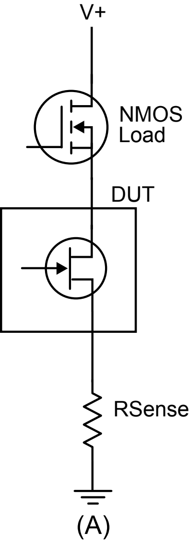


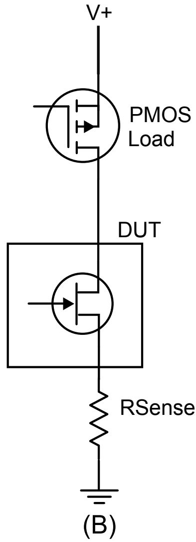
(C)

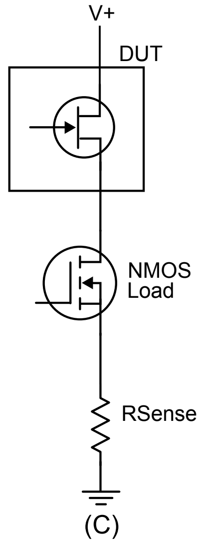




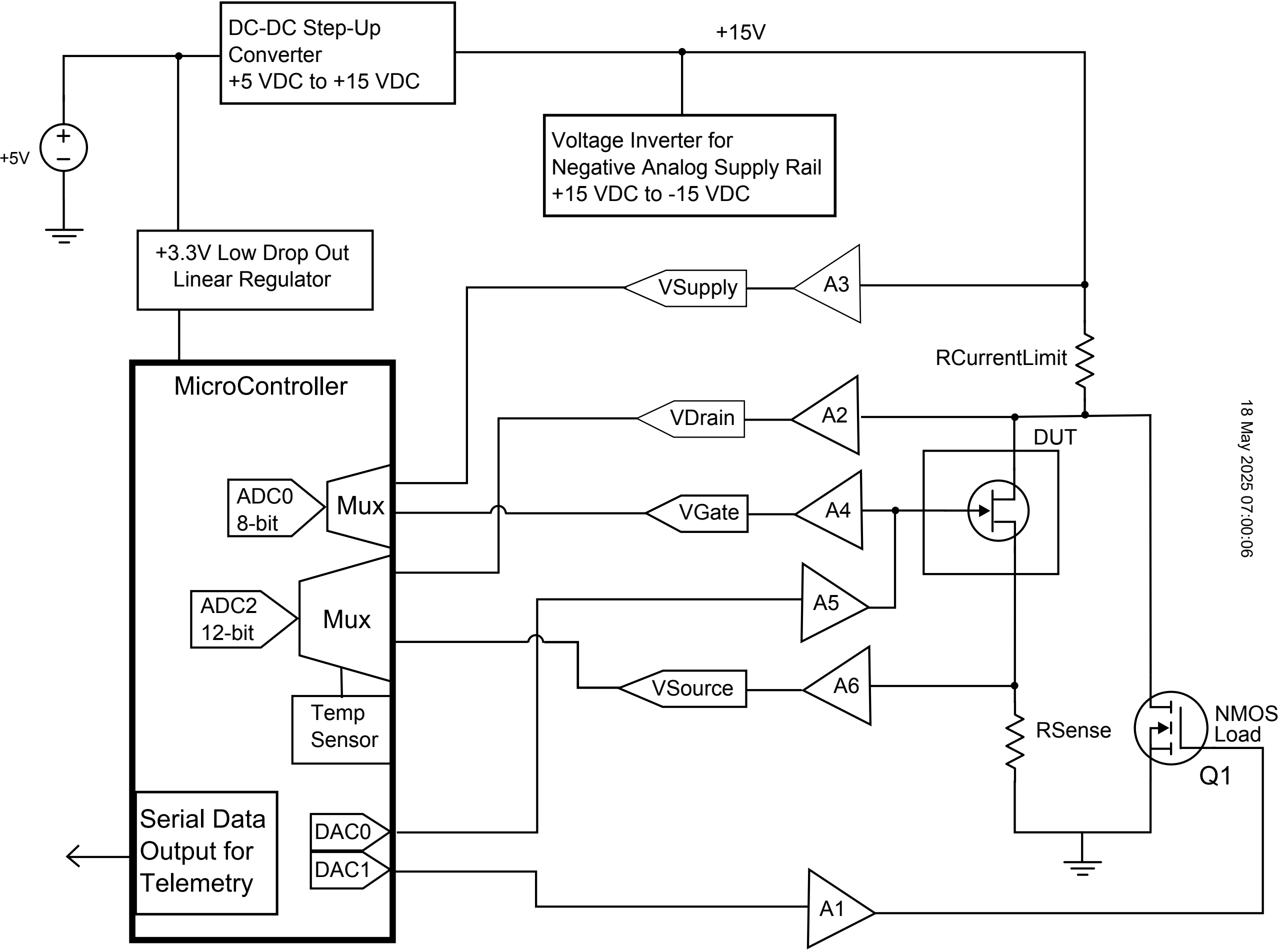
18 May 2025 07:00:06







V+
RCurrentLimit
DUT
NMOS
Load
RSense
(D)


DC-DC Step-Up Converter +5 VDC to +15 VDC
+15V
+5V
Voltage Inverter for Negative Analog Supply Rail +15 VDC to -15 VDC
+3.3V Low Drop Out Linear Regulator
VSupply
A3
RCurrentLimit
MicroController
VDrain
A2
DUT
ADC0 8-bit
Mux
VGate
A4
ADC2 12-bit
Mux
A5
VSource
A6
Temp Sensor
RSense
NMOS Load
Q1
Serial Data Output for Telemetry
DAC0
DAC1
A1
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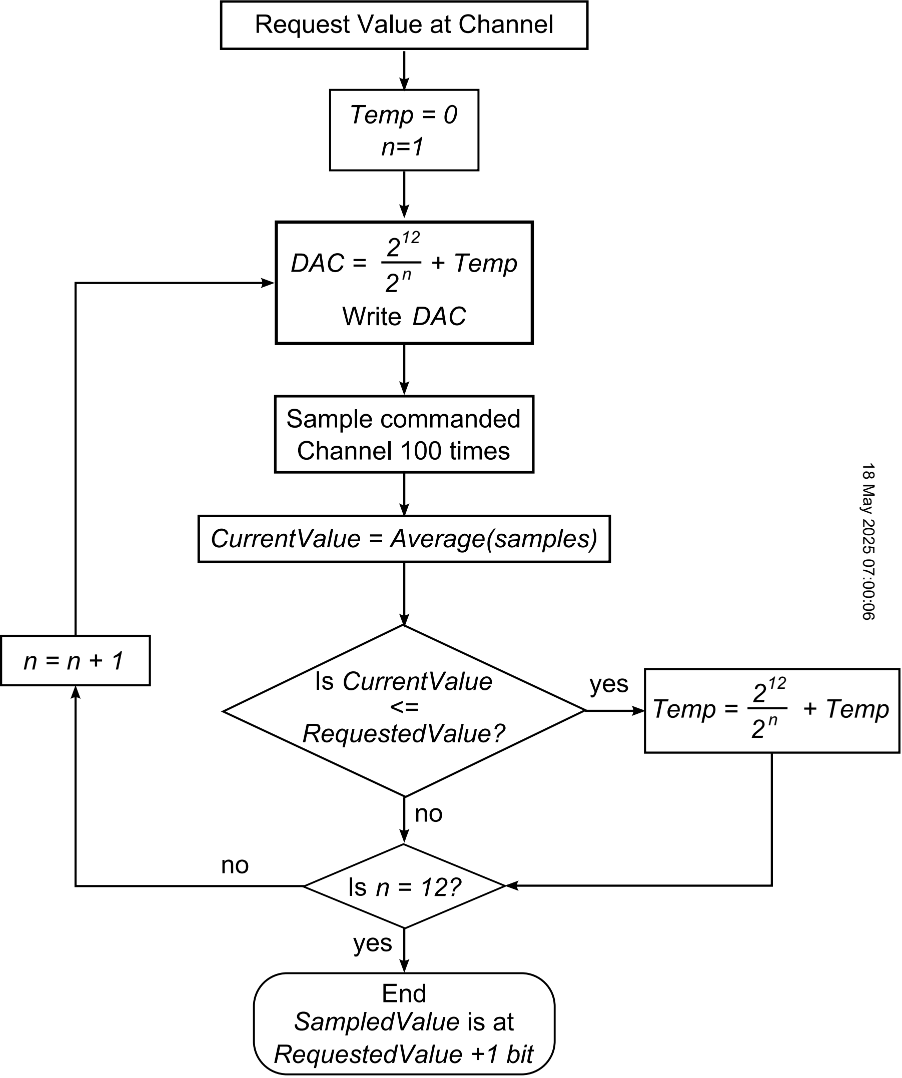

Request Value at Channel
Temp = 0
n=1
DAC = 2^12 / 2^n + Temp
Write DAC
Sample commanded Channel 100 times
CurrentValue = Average(samples)
Is CurrentValue <= RequestedValue?
yes
Temp = 2^12 / 2^n + Temp
no
Is n = 12?
no
n = n + 1
yes
End
SampledValue is at RequestedValue +1 bit
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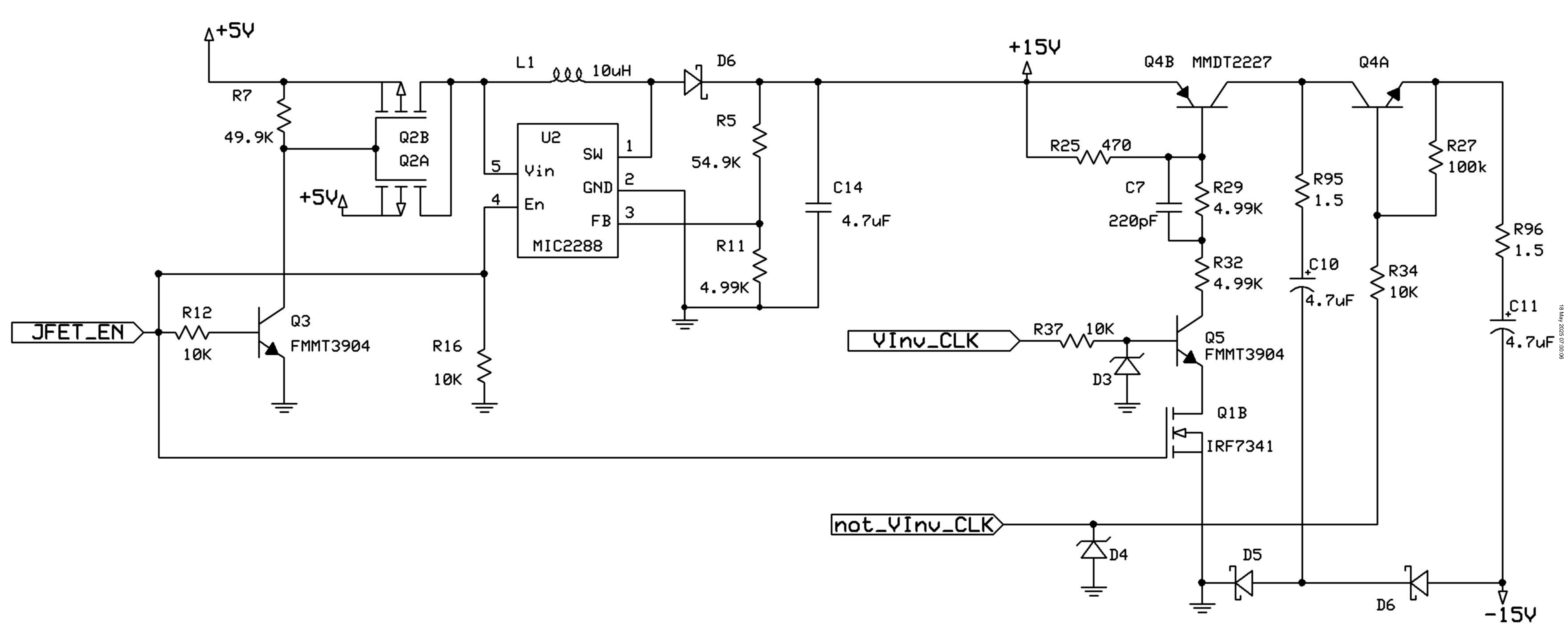
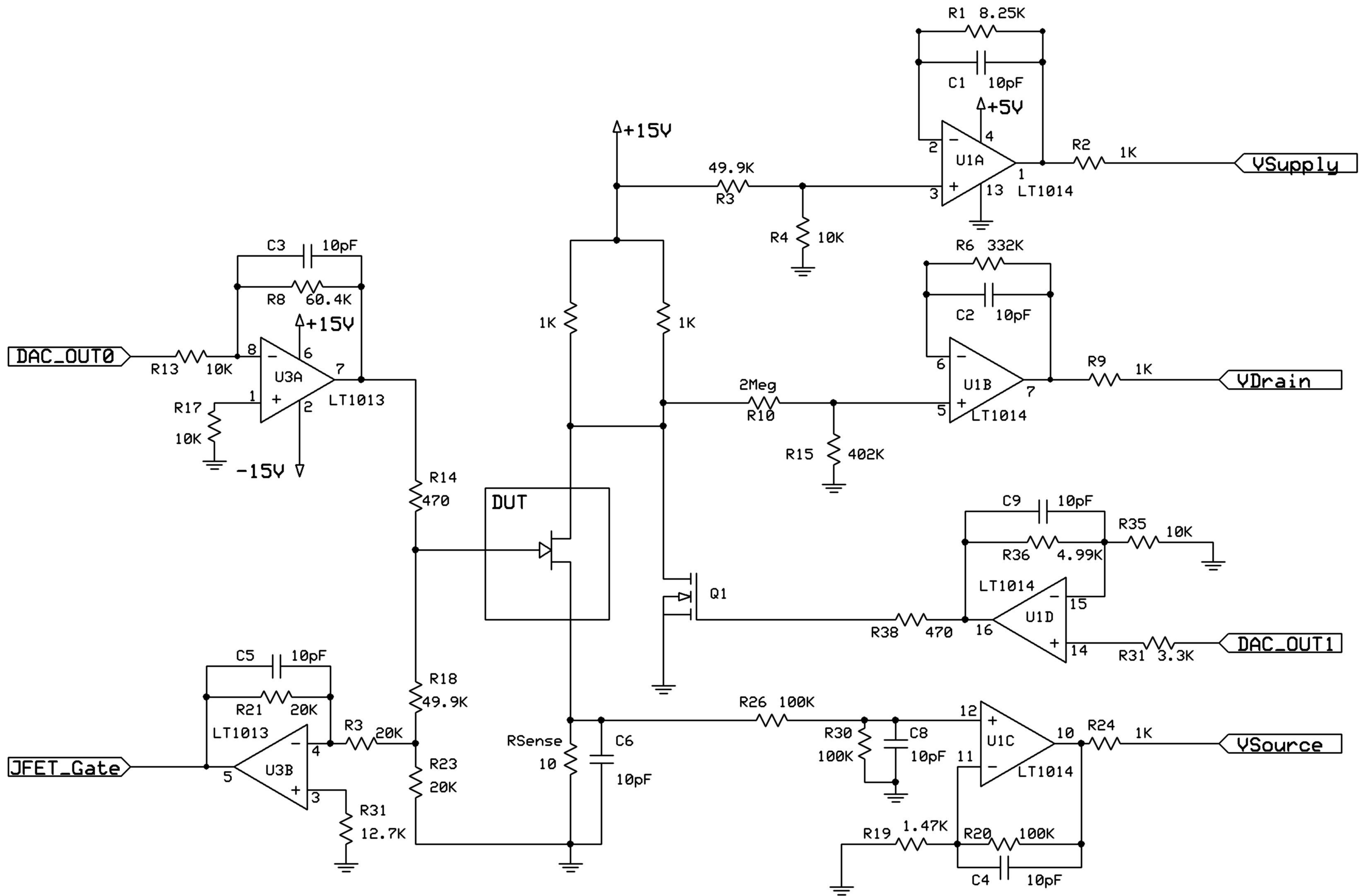
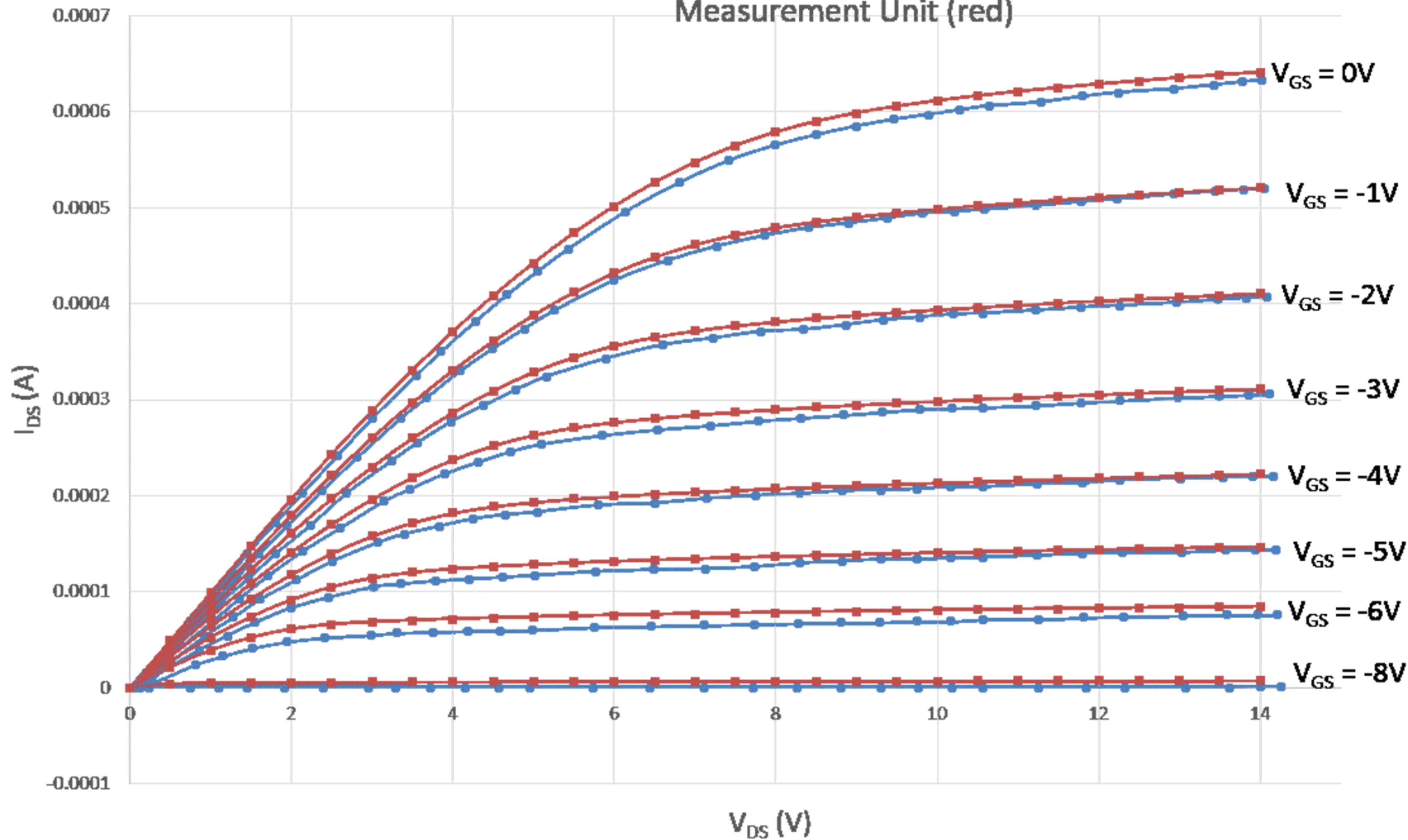
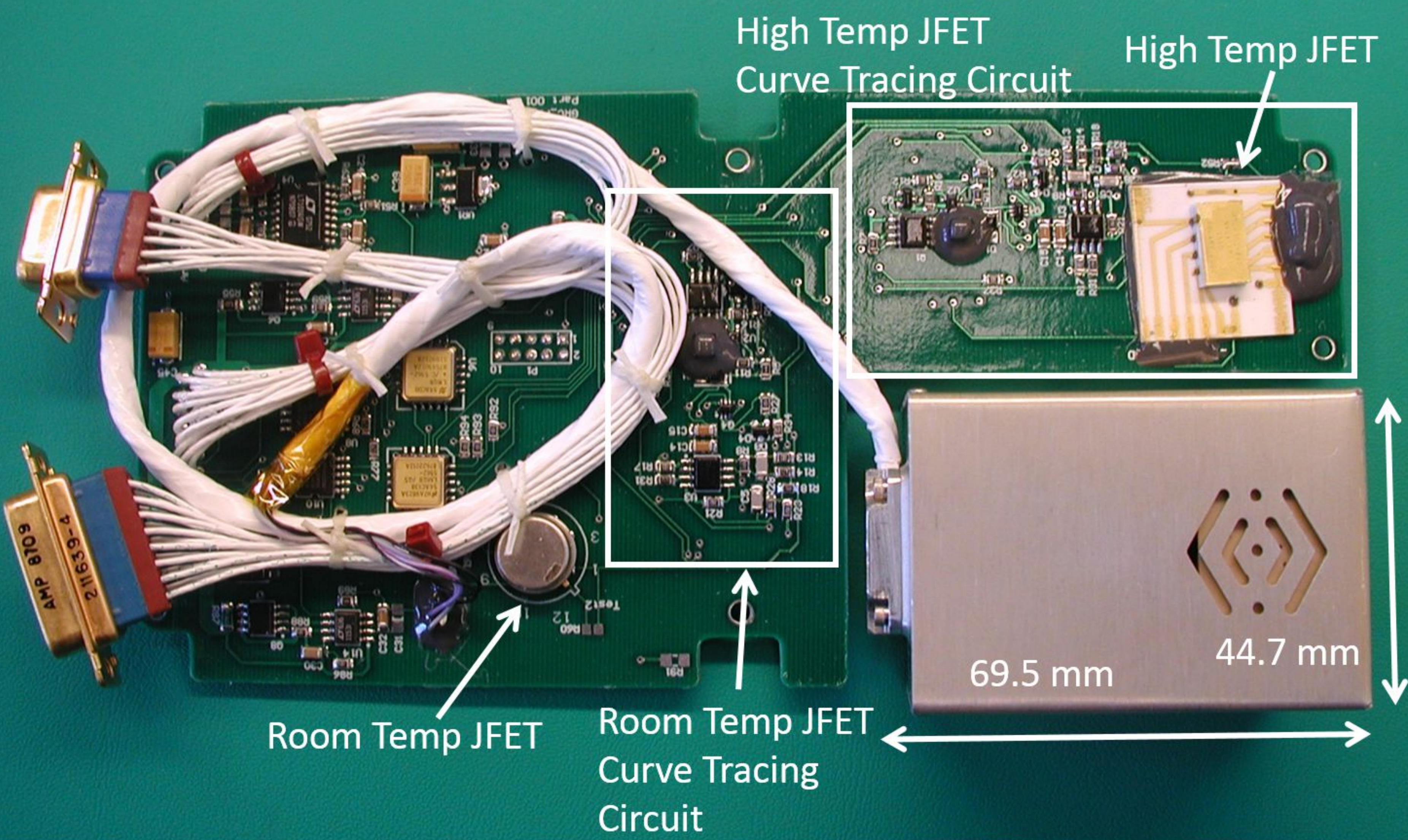

+5V
R7
49.9K
Q2B
Q2A
+5V
L1
10uH
D6
U2
SW
1
5
Vin
GND
2
4
En
FB
3
MIC2288
R5
54.9K
R11
4.99K
C14
4.7uF
+15V
Q4B
MMDT2227
Q4A
R25
470
C7
220pF
R29
4.99K
R32
4.99K
R95
1.5
C10
4.7uF
R27
100k
R34
10K
R96
1.5
C11
4.7uF
JFET_EN
R12
10K
Q3
FMMT3904
R16
10K
VInv_CLK
R37
10K
D3
Q5
FMMT3904
Q1B
IRF7341
not_VInv_CLK
D4
D5
D6
-15V


R1 8.25K
C1 10pF
+5V
U1A
LT1014
R2 1K
VSupply
+15V
49.9K
R3
R4 10K
R6 332K
C2 10pF
U1B
LT1014
R9 1K
VDrain
2Meg
R10
R15 402K
C3 10pF
R8 60.4K
+15V
DAC_OUT0
R13 10K
U3A
LT1013
R17 10K
-15V
1K
1K
R14 470
DUT
C9 10pF
R35 10K
R36 4.99K
LT1014
U1D
Q1
R38 470
DAC_OUT1
R31 3.3K
C5 10pF
R21 20K
LT1013
U3B
JFET_Gate
R3 20K
R18 49.9K
R23 20K
R31 12.7K
RSense 10
C6 10pF
R26 100K
R30 100K
C8 10pF
U1C
LT1014
R24 1K
VSource
R19 1.47K
R20 100K
C4 10pF



18 May 2025 07:00:06



18 May 2025 07:00:06