TI Low-Leakage130nm Digital Process with Nonvolatile FRAM for Ultra-Low-Power Medical Electronics

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Both external and implantable devices are becoming more sophisticated and are requiring more on-chip memory to store data from biological sensors. To deal with this complexity, chip designs are moving toward smaller process geometries, which provide added functionality, reduced size, or both, often along with a reduction in dynamic power. However, leakage power begins to increase significantly at the 130nm node if steps are not taken to mitigate the increased transistor leakage. Lower operating voltages and careful transistor design can offset some of this increase. These very changes, however, make it difficult to design a dense, stable low-power SRAM. Nonvolatile memories like FRAM (F-RAM) avoid these difficulties and save power by simply turning off the memory when not in use. This is particularly valuable since many medical devices have very low duty cycle. FRAM provides the added benefit of providing SRAM-like active power, unlike competing nonvolatile technologies. To meet the challenging power requirements of medical devices, a new ultra-low-power 130nm process has been developed. The new process includes a very-high-density, SER-resistant, nonvolatile FRAM and an ultra-low-leakage transistor, coupled with a library that is optimized for low-power operation. This paper compares the power, area and performance of competing process technologies for a typical implantable medical design and highlights the advantages that FRAM provides in low static power through a transparent power-down capability and in low SRAM-like active power.