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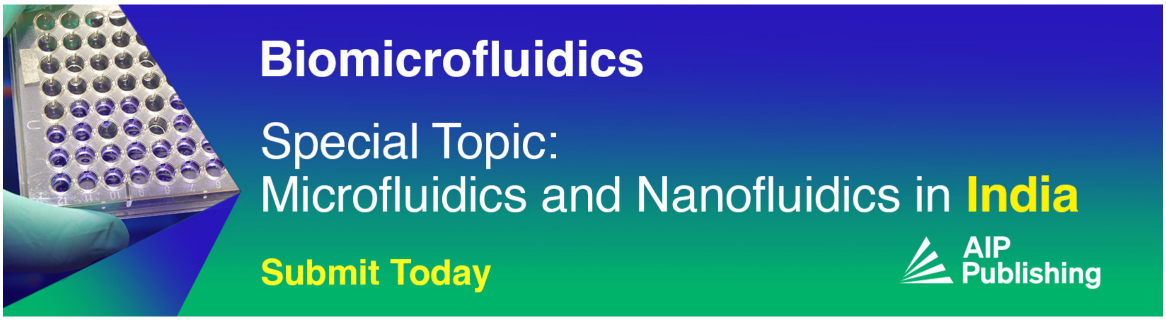

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Moore's law realities for recording systems and memory storage components: HDD, tape, NAND, and optical

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This paper describes trends in the storage technologies associated with Linear Tape Open (LTO) Tape cartridges, hard disk drives (HDD), and NAND Flash based storage devices including solid-state drives (SSD). This technology discussion centers on the relationship between cost/bit and bit density and, specifically on how the Moore's Law perception that areal density doubling and cost/bit halving every two years is no longer being achieved for storage based components. This observation and a Moore's Law Discussion are demonstrated with data from 9-year storage technology trends, assembled from publically available industry reporting sources.
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INTRODUCTION

Data are stored in isolated regions on media in storage components, i.e. in magnetic bits on tape media in cartridges, in magnetic bits on disk platters in HDDs, or in electric charge levels on silicon based NAND chips in SSDs. This paper examines the storage landscape trends for bit density and cost/bit associated with technologies that produce TAPE, HDD, and NAND/SSD components. Storage application decisions are dependent on density (i.e. component capacity) and cost. In the past, such decisions have assumed geometric progress, i.e. that an increasing figure of merit (density) grows by a factor $(1+\alpha)^n$ where n is the number of years, 100α is the annual percentage increase and that a decreasing figure of merit (cost/bit) reduces by a factor $(1-\beta)^n$ where n is the number of years, 100β is the annual percentage decrease. Ideal Moore's Law progress has $\alpha=0.41$ (bit density doubles every two years) and $\beta=0.29$ (cost/bit halves every two years). An observation of this paper is that storage technologies are not achieving ideal Moore's Law metrics. Physics and economic trends will be cited as reasons for this observation.

MOORE'S LAW

In 1965, Gordon Moore projected that the number of components (transistors, resistors, capacitors) in an integrated circuit (IC) would increase exponentially and the individual components would decrease in cost exponentially.[1] In 1975 Gordon Moore refined this projection by specifying that IC complexity would double on a two-year basis for the same cost.[2] For an IC, the doubling of the number of components and the halving of cost per component on a two-year basis became Moore's Law. For storage applications, Moore's Law is two-fold. First, it sets the expectation that any increase in bit density yields a proportional decrease in cost/bit; a statement that the cost to produce a unit area of storage stays constant when Moore's Law expectations are satisfied. Second, it sets the ideal expectation that the increase in bit density doubles on a two-year basis and the cost/bit halves on a two-year basis. These two criteria imply $\beta=\alpha/(1+\alpha)$ with $\alpha=0.41$ and $\beta=0.29$ corresponding to the ideal Moore's Law expectation.

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TABLE I. 9 Year Storage Technology Trends.

	2008	2009	2010	2011	2012	2013	2014	2015	2016
HDD									
Units (M)	540	557	652	620	577	551	564	470	425
EB Shipped (EB)	125	200	330	335	380	470	549	565	693
Density (Gb/in^2)	380	530	635	750	750	900	900	1000	1100
Revenue ($B)	34.0	34.0	33.0	33.5	37.5	33.4	33.4	28.3	26.8
$/GB	0.272	0.170	0.100	0.100	0.100	0.071	0.061	0.051	0.039
NAND									
Wafers (12”) (M)	7.3	8.3	9.7	11.3	12.1	13.7	14.8	15.9	17.0
EB Shipped (EB)	3.0	5.4	10.5	18.6	28.0	39.0	62.5	83.0	120.0
Density (Gb/in^2)	200	280	330	550	550	850	1200	1500	2000
Revenue ($B)	10.1	12.1	18.5	21.5	22.0	24.0	32.2	33.2	38.7
$/GB	3.33	2.23	1.77	1.16	0.78	0.615	0.515	0.401	0.320
LTO TAPE									
Cartridges (M)	27.1	24.3	25.0	24.3	23.4	21.6	22.2	19.4	19.4
EB Shipped (EB)	11.05	12.00	15.34	18.42	20.68	24.27	30.10	33.02	40.32
Density (Gb/in^2)	0.9	0.9	1.2	1.2	2.1	2.1	2.1	4.1	4.1
Revenue ($B)	1.0	0.7	0.7	0.7	0.62	0.54	0.50	0.59	0.65
$/GB	0.091	0.059	0.046	0.038	0.030	0.022	0.017	0.018	0.016

9-YEAR STORAGE LANDSCAPE HISTORY

In order examine the cost/bit and areal density characteristics for storage technologies, Table I presents updated 9-year technology trends[3] for three storage media classes: NAND Flash, HDD, and LTO Tape Media. Data for this table are obtained from publically available sources: LTO Consortium, DRAMeXchange, Quarterly Report Statements from Seagate, Western Digital, Samsung, and Micron. Cost/bit data represents a value averaged over all products; total component revenue divided by total bits shipped in a year. Areal density refers to the maximum areal density in any product recognizing

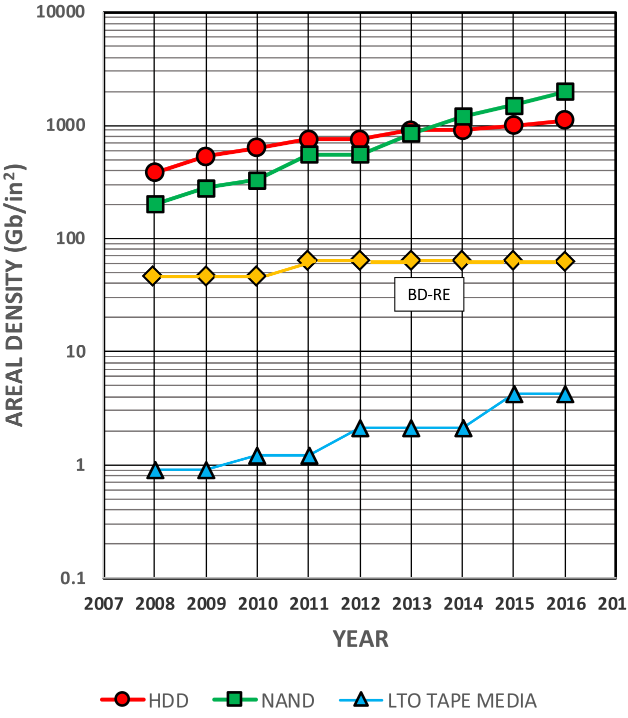

FIG. 1. 9 year history of areal density increases for HDD, NAND, LTO Tape, and Optical Blu-ray.

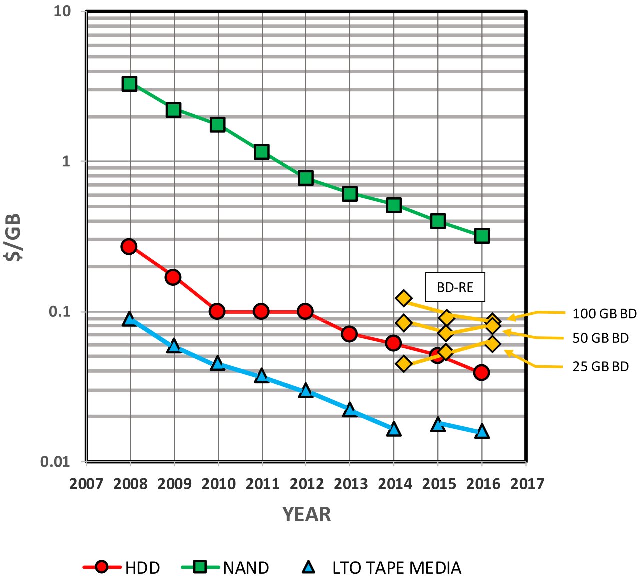

FIG. 2. 9 year history of cost/bit decreases for HDD, NAND, LTO Tape, and Optical Blu-ray.

that technologies offer an array of products using different areal densities. Tape media data is for the LTO product space. NAND data is for manufactured dies and excludes solid-state drives using these components. LTO Tape Media data is for cartridges. After 2014 there is a discontinuity in the LTO Tape Media data for cost/bit related to changes in the LTO Consortium reporting of cartridge and bit shipments.

From these data, areal density and cost/bit trends are shown in Figure 1 and Figure 2. These logarithmic plots illustrate geometric characteristics as anticipated. Optical disc BD-XL media data are added for reference. Note that cost/bit data is for unit counts > 50 disks and that no public data exist for Exabyte shipments or industry revenue for this class of optical media.

AREAL DENSITY AND COST/BIT DISCUSSION

Areal density and cost per bit data from Table I are recast in Table II by examining annual change trends over the last 8-year, 3-year, and 1-year ranges to better compare the growth of storage metrics relative to Moore's Law performance. It should be noted that 1-year trends are subject to variability due to new product introduction timing. The 3-year averages are more representative of technology performance. From Table II areal density trends show no technology achieving the ideal 41% Moore's Law metric for areal density; the driver for increased component capacity. NAND aided by lithography for fabricating smaller features and a migration from 2 bit/cell to 3 bit/cell structures has realized 33% annual increases in areal density. The typical two-year product cycles for LTO

TABLE II. Annual percentage changes for areal density and cost/bit for NAND, HDD, LTO Tape for three time periods: last 8 years, last 3 years, last 1 year.

	Annual Change (8 yr., 2008-2016)	Annual Change (3 yr., 2013-2016)	Annual Change (1 yr., 2015-2016)
Areal Density NAND	33%	33%	33%
Areal Density HDD	14%	7%	10%
Areal Density LTO TAPE	21%	25%	0% (2 year cycle)
$/GB NAND	-25%	-20%	-20%
$/GB HDD	-21%	-18%	-23%
$/GB LTO TAPE	-19%	-10%	-10%

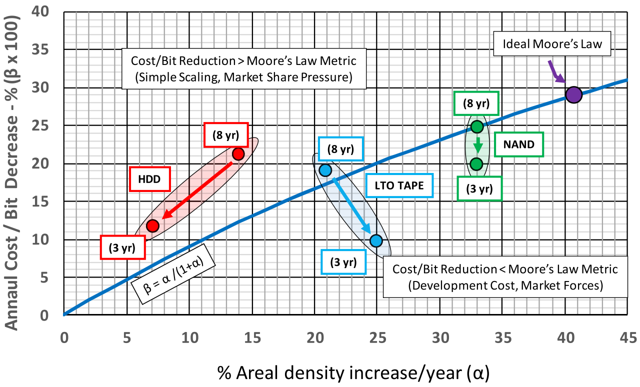

FIG. 3. Annual cost/bit vs areal density changes for HDD, LTO Tape, NAND for periods: last 8 years and last 3 years. Data are compared with ideal Moore's Law curve of β=α/(1+α).

TAPE distort its 1-year areal density trend since the next LTO Tape product will be introduced in 2017. HDD areal density increases lag by a factor of ∼2 both the NAND and TAPE values. $/GB trends for NAND, HDD, and LTO Tape Media show annual decreases in the 20% range rather than the perceived Moore's Law metric of 29%.

A graphical representation of these observations is shown in Figure 3 where cost/bit decrease (β) is plotted vs areal density increase (α) for the 8-year and 3-year time ranges along with the ideal Moore's Law curve β=α/(1-α). For both LTO TAPE and NAND the 8-year data are **on** the Moore's Law curve while 3-year data fall below the Moore's Law curve implying 1) market forces and/or 2) more cost with attaining the higher areal density. For HDD 8-year and 3-year data are above the Moore's Law curve implying 1) market force competition with multiple suppliers and/or 2) incremental areal density improvements are cost effective since less development investment is required. General observations show that while 8-year cost/bit reductions were in the 20% to 25% range the 3-year cost per bit reductions were significantly reduced. The technology reality is that bit scaling is becoming more difficult with significant deviations from the Moore's Law relationship between cost and density.

BIT SCALING DISCUSSION

Bit scaling strategies for storage technologies are illustrated in Figure 4. Magnetic based technologies use traditional two-dimensional (2-D) scaling while NAND, and to some extent, optical

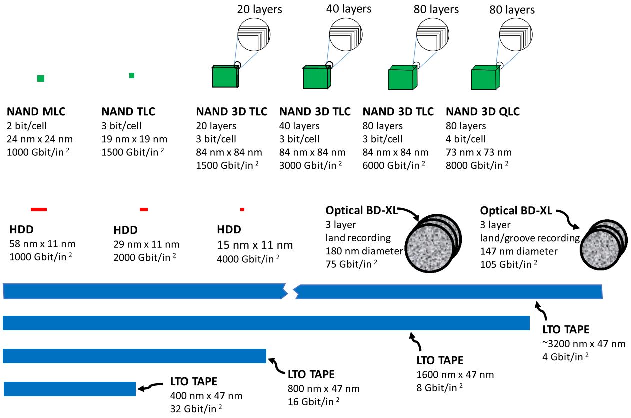

FIG. 4. Scaling strategies for bit cells associated with HDD, NAND, LTO Tape, and Optical BD-XL. Bit cells are drawn to scale.

technologies are moving to three-dimensional (3-D) scaling. The issue for 3-D scaling is processing multiple layers of bit cells simultaneously to control cost while the issue for 2-D scaling is the physics associated with smaller bit cells and the signal to noise ratio (SNR) associated with fewer state variables (i.e. charge, magnetic grains, phase change grains) within the bit cell.

For LTO Tape, large bit cells, in comparison with present day HDD cell sizes, are retained during scaling.[4] Successful scaling to higher densities should be achieved since sensors and bit cells would be in the 500nm length scale range, significantly larger than present day HDD products. Further, LTO Tape bit cells can use the present and proven HDD technology to support these scaled bits. Moore's Law metrics will be sustained assuming economic issues (single source suppliers) do not impact cost. Conversely, the scaled bit cells in HDD must approach the <20nm length scale (~40X smaller than LTO Tape media length scales) which implies sensor widths/mechanical positioning in the sub 10nm range. These dimensions suggest that future scaling would be challenging for HDD and require new and costly magnetic, i.e. heat assisted,[5] strategies. The HDD's present low areal density annual rate increases of ~10% demonstrate this deviation from Moore's Law performance.

Recognizing processing issues associated with producing bit cells below the 25nm length scale, NAND is designing multi-layer or 3-D bit cell structures.[6] NAND is increasing the physical bit area by a factor of N but adding N layers of cells in a stack and, most critically, processing all N layers simultaneously. As an example, for a NAND areal density of 1500 Gbit/in^2, a traditional planar cell with 19nm x 19nm or 379nm^2 area is equivalent to a 3-D cell with 84nm x 84nm or 7056nm^2 area if 19 layers of cells are stacked above this cell. Cost efficiency is achieved since all cells in the 20-layer stack are processed simultaneously like a planar cell.

Optical bits are recorded on the land region of a grooved media surface on which thermally sensitive material is deposited. Optical scaling uses two strategies:[7] moving to recording on both the land and the valley region of the groove by increasing the groove pitch and using multiple layers of grooved media surfaces on the disc. The multi-layer strategy does not provide significant cost/bit benefits (Figure 2) since each layer on the disk is individually processed. Moving from 3-layer single sided disks to 6 layer double-sided disks adds twice the processing cost for twice the capacity. The cost/bit stays constant.

SUMMARY

Moore's Law has served as a technology metric for storage components for 40+ years. Tape, HDD, and NAND, and Optical technologies are no longer achieving the cost benefits from bit cell scaling relative to Moore's law expectations. For non-magnetic based technologies planar scaling has moved to 3-D scaling strategies with significant success for NAND structures but with cost/bit deficiencies for Optical. Magnetic based technologies do not have 3-D scaling options. For HDD, 2-D scaling has become problematic with density increase rates significantly below Moore's law expectation. For Tape, 2-D scaling continues since bit cells are 100X larger in area than HDD bit cells. In sum, both NAND and Tape should provide several generations of storage products that approach Moore's Law expectations for component capacity and component cost.

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