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Physicists Plan Supercollider Simulations Meeting FREE

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Physicists Plan Supercollider Simulations Meeting

High energy physicists will meet to map out software designs for future billion-event experiments that they hope to conduct on the Superconducting Super Collider (SSC). The three-day meeting, Future Directions in Detector R&D for Experiments at Proton-Proton Colliders, is sponsored by the Division of Particles and Fields of the American Physical Society and will be held July 5 through July 7, in Snowmass, Colo. "We are looking at computing power requirements for event simulation, and formal design methods for software development," says Lawrence Berkeley senior physicist Stewart Loken.

Independent groups working at Brookhaven National Laboratory, Upton, N.Y., and the Stanford Linear Accelerator Center (SLAC), Stanford, Calif., among others, are presenting software programs for SSC event simulation and central tracking system simulation. Brookhaven physicists Frank Paige and Serban Protopopescu will describe potential SSC implementations of ISAJET, an event simulation program they began work on in 1980.

The three-day meeting on computing is part of the DPF's 1988 Summer Study on High Energy Physics in the 1990s, which will be held from June 27 through July 15 in Snowmass, Colo.

For information, contact: Stewart Loken, Lawrence Berkeley Laboratory, Berkeley, Calif., 94720; (415) 486-4000.

Cray and Convex Compete For Computing Crown

Cray Research Inc., Minneapolis, Minn., has just announced the Y-MP/832, its follow-on to the X-MP line of multiprocessing supercomputers. The $20 million, eight-processor system has a six nanosecond clock cycle and 32 megawords of memory (256 megabits). By comparison, a top-of-the-line four-processor X-MP has an 8.5 nanosecond clock cycle and 16 megawords of memory.

Los Alamos National Laboratory, Los Alamos, N.M., expects to receive the first of two Y-MPs it has ordered by the end of 1988. The National Center for Supercomputing Applications, Champaign, Ill., the Pittsburgh Supercomputing Center, and the Ohio Supercomputer Center, Columbus, also hope to acquire Y-MPs.

At the same time, Convex Computer Corp., Richardson, Texas, said it will begin shipping the C240, its 200 megaflops parallel processing supercomputer, in the fourth quarter of 1988. The $1.3 million C240 tops off the six-mainframe C Series that Convex introduced this past March.

For more information, contact: Tina Bonetti, Cray Research Inc., 608 Second Ave. South, Minneapolis, Minn. 55402; (602) 333-5889; and Convex Computer Corp., 701 N. Plano Road, Richardson, Texas 75081; (214) 952-0200.

SDSC Molecular Modeling Teleconference On Way To Video Stores

The San Diego Supercomputer Center's recent teleconference on molecular design using supercomputers is now available on videotape. Speakers at the four-hour teleconference, which was held this past April, addressed supercomputing issues in molecular modeling, protein complexes, and computational chemistry. Participating speakers included SDSC director Sidney Karin, SDSC computational chemist Richard Hildebrandt, Erich Wimmer, Cray marketing manager, and Frank Momany, Polygen Corp., Waltham, Mass., scientific director.

San Diego State University's (SDSU) College of Extended Studies, San Diego, Calif., broadcast the April teleconference from its KPBS studios to satellite links for interactive question and answer sessions with the teleconference audience. The teleconference came as a follow-up to an initial telecast on supercomputing that SDSC held in March, 1987.

VHS videotapes of the teleconference, accompanied by lecture notes, are available from SDSU. For information, contact: SDSU College of Extended Studies, PROFNET Teleconference, San Diego, Calif., 92182; (619) 229-2286.

Minnesota Researchers Design Systolic Array Building Blocks

If fabrication of a just-designed Systolic Array Controller (SAC) goes as planned, physicists could have a new low-cost tool for matrix computations and signal processing applications. Researchers in the Department of Electrical Engineering, University of Minnesota, Minneapolis, completed design of the SAC at the end of last year and submitted a fabrication proposal this past March to IBM's VLSI Academic Program, Manassas, Va. The SAC is expected to go into fabrication sometime this summer.

"Our basic philosophy is to try and generate an inexpensive building block for implementing systolic arrays that would use just two chips," says Gerald Sobelman, associate professor of electrical engineering and one of the SAC's designers. A systolic array is an array of processors where pipelined computations take place along all dimensions of the array, in a manner similar to the rhythmic pumping of a heart, to achieve higher computational throughput. The SAC is designed to be an inexpensive building block for use in large multiprocessing architectures.

For more information, contact: Gerald Sobelman, Department of Electrical Engineering, 123 Church Street, S.E., Minneapolis, Minn., 55455; (612) 625-8041. ■