Physical insight into the abnormal $V_{TH}$ instability of Schottky $p$-GaN HEMTs under high-frequency operation

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Physical insight into the abnormal $V_{\text{TH}}$ instability of Schottky $p$-GaN HEMTs under high-frequency operation

In this Letter, we investigate the threshold voltage ($V_{\text{TH}}$) instability of Schottky $p$-GaN gate high electron mobility transistors (SP-HEMTs) under high-frequency operation by a resistive-load hard switching method. The abnormal $V_{\text{TH}}$ instability is observed, which is different between fully and partially depleted SP-HEMTs (FD- and PD-HEMTs). Notably, for FD-HEMT, $V_{\text{TH}}$ shifts positively with effective stress time. However, the $V_{\text{TH}}$ instability in PD-HEMT is more complex. At low $V_{\text{GS}}$ (e.g., 3 V) and high $V_{\text{GS}}$ (e.g., 6 V), $V_{\text{TH}}$ shifts positively with stress time consistently. Nevertheless, at intermediate $V_{\text{GS}}$ levels (e.g., 4 and 5 V), $V_{\text{TH}}$ initially shifts positively and then negatively, displaying a non-monotonous variation. Furthermore, the frequency dependence of $V_{\text{TH}}$ is contingent upon $V_{\text{GS}}$. At low $V_{\text{GS}}$, $V_{\text{TH}}$ exhibits a negative shift with the increase in frequency. This trend inverses when $V_{\text{GS}}$ exceeds 4 V. And it should be noted that the extracted $V_{\text{TH}}$ under high-frequency operation is lower than their quasi-static values for both transistor types. This work depicts the physical process and mechanism of the abnormal $V_{\text{TH}}$ instability; different from the quasi-static case, hole accumulation effects will be enhanced due to the high $dV_{\text{GS}}/dt$, which results in a lower $V_{\text{TH}}$. The distinct $V_{\text{TH}}$ behaviors of FD- and PD-HEMTs are closely related to the trapping effects, as well as hole accumulation and insufficiency, within the two different $p$-GaN gate layers.

ABSTRACT

In this Letter, we investigate the threshold voltage ($V_{\text{TH}}$) instability of Schottky $p$-GaN gate high electron mobility transistors (SP-HEMTs) under high-frequency operation by a resistive-load hard switching method. The abnormal $V_{\text{TH}}$ instability is observed, which is different between fully and partially depleted SP-HEMTs (FD- and PD-HEMTs). Notably, for FD-HEMT, $V_{\text{TH}}$ shifts positively with effective stress time. However, the $V_{\text{TH}}$ instability in PD-HEMT is more complex. At low $V_{\text{GS}}$ (e.g., 3 V) and high $V_{\text{GS}}$ (e.g., 6 V), $V_{\text{TH}}$ shifts positively with stress time consistently. Nevertheless, at intermediate $V_{\text{GS}}$ levels (e.g., 4 and 5 V), $V_{\text{TH}}$ initially shifts positively and then negatively, displaying a non-monotonous variation. Furthermore, the frequency dependence of $V_{\text{TH}}$ is contingent upon $V_{\text{GS}}$. At low $V_{\text{GS}}$, $V_{\text{TH}}$ exhibits a negative shift with the increase in frequency. This trend inverses when $V_{\text{GS}}$ exceeds 4 V. And it should be noted that the extracted $V_{\text{TH}}$ under high-frequency operation is lower than their quasi-static values for both transistor types. This work depicts the physical process and mechanism of the abnormal $V_{\text{TH}}$ instability; different from the quasi-static case, hole accumulation effects will be enhanced due to the high $dV_{\text{GS}}/dt$, which results in a lower $V_{\text{TH}}$. The distinct $V_{\text{TH}}$ behaviors of FD- and PD-HEMTs are closely related to the trapping effects, as well as hole accumulation and insufficiency, within the two different $p$-GaN gate layers.

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Enhancement-mode (E-mode) GaN power high electron mobility transistors (HEMTs) are promising candidates for the next-generation high-efficiency power conversion applications, as GaN HEMTs exhibit low on-resistance and fast switching speed. Among several technologies implemented to realize the E-mode operation, the Schottky $p$-GaN gate HEMTs (SP-HEMTs) dominate the scene of commercial E-mode GaN HEMTs because of the balanced combination of performance, reliability, and manufacturability. Nevertheless, trapping effects or charge accumulation effects at different locations of the gate stack under various bias conditions can adversely affect the threshold voltage ($V_{\text{TH}}$) stability.

The $V_{\text{TH}}$ stability of SP-HEMTs is sensitive to the gate stress, which has been extensively investigated by various testing techniques, such as measurement-stress-measurement sequences, pulsed $I$-$V$, and fast sweeping characterization. Commonly, the $V_{\text{TH}}$ instability is explained by electron trapping, hole injection, and hole depletion in the $p$-GaN/AlGaN stack. However, for high-frequency operation, the high gate voltage ($V_{\text{GS}}$) rise rate needs to be considered. Tang et al. recently reported that the SP-HEMTs exhibit a negative $V_{\text{TH}}$ shift under high $dV_{\text{GS}}/dt$ and the false turn-on of GaN device during fast switching transient is also observed, which is attributed to the negative $V_{\text{TH}}$ shift. He et al., however, reported a positive $V_{\text{TH}}$ shift under high-frequency gate stress by a resistive-load setup. With the distinct $V_{\text{TH}}$ shift under high-frequency operation, further study on $V_{\text{TH}}$ stability under actual switching operation is necessary, which is important.
to understand the detailed physical mechanism and is important for
system designers to design appropriate gate drivers.

In this work, a time-resolved $V_{TH}$ is extracted by a resistive-load
hard switching method under high-frequency operation conditions.
The abnormal $V_{TH}$ instability of SP-HEMTs with fully depleted $p$-
GaN gate (FD-HEMT) and partially depleted $p$-GaN gate (PD-
HEMT) is observed. By comparing the different $V_{TH}$ behaviors
between FD-HEMT and PD-HEMT, the physical mechanisms of the
abnormal $V_{TH}$ instability under high-frequency operation conditions
are analyzed.

The devices under test (DUTs) in this work are commercially
available SP-HEMTs of EPC2052 (DUT A) from Efficient Power
Conversion Corporation and GS66104B (DUT B) from GaN System.
The measured gate capacitance ($C_G$) characteristics of DUTs are
shown in Fig. 1. The $C_G$ of SP-HEMTs can be modeled as the combi-
nation of series-connected Schottky junction capacitance ($C_{Sch}$)
and $p$-GaN/AlGaN/GaN pin capacitance ($C_{pin}$), when the SP-HEMT is
fully turned on, $C_{pin}$ can be simply modeled as the plate capacitor with
a fixed value, and $C_{Sch}$ will be changed with a variation in the width
of the depletion region. For DUT A, the on-state $C_G$ exhibits a negligible
change, indicating a fixed depletion region width in the $p$-GaN layer,
thus, DUT A is an FD-HEMT. For DUT B, the on-state $C_G$ decreases
with the increase in $V_G$, indicating the extension of the depletion
region in the $p$-GaN layer, thus, DUT B is a PD-HEMT. It should be
noted that the $p$-GaN layer of DUT A is depleted fully when $V_{GS}$
$> V_{TH}$, because the $V_{TH}$ of DUT A is much higher than the $V_{TH}$ of
the FD-HEMT with a fully depleted $p$-GaN layer at zero gate voltage.

In order to extract the time-resolved $V_{TH}$ of DUTs under high-
 frequency operation, the resistive-load hard switching test method is
implemented and the schematic of the test circuit is shown in
Fig. 2(a), in which the high-frequency square pulses are applied to
the gate terminal of DUTs. The waveforms of $V_{DS}(t)$ and $V_{GS}(t)$
can be simultaneously recorded by a high-resolution oscilloscope with 2.5-
GSa/s sampling rate, and the propagation delay of probes has been cal-
brated before measurement. Figure 2(b) shows the measured $V_{DS}(t)$
and $V_{GS}(t)$ waveforms with a $V_{GS}$ of 5 V, a $V_{DD}$ of 10 V, and a rise
time ($t_r$) and fall time ($t_f$) of 150 ns. The current flowing through $R_L$
($I_{DS}$) and DUT channel ($I_{DS}$) can then be calculated based on the mea-
sured $V_{GS}(t)$ and $V_{DS}(t)$, as shown in Fig. 2(c), in which the displace-
ment current ($I_{Dis}$) is considered. $V_{TH}$ is defined at an $I_{DS}$ of 10 mA
according to $V_{GS}$ during the rise section.

Figure 3 shows the extracted time-resolved $V_{TH}$ of FD-HEMT
under high-frequency operation conditions (200 kHz, 500 kHz, and
1 MHz) with the same $dV_{GS}/dt$ of 50 mV/ns and $V_{GS}$ of 3, 4, 5, and
6 V, respectively. Due to the log-type of effective stress time axis, the
$V_{TH}$ of 1.14 V extracted from the first pulse is missing $V_{TH}$, which is

![FIG. 1. Measured $C_G$ characteristics of DUT A and DUT B under the frequency of 1 MHz.](image1)

![FIG. 2. (a) Schematic diagram of the resistive-load hard switching test circuit. (b) Measured $V_{DS}(t)$ and $V_{GS}(t)$ waveforms and calculated $I_{DS}$ and $I_{DS}$ with an $R_L$ of 100 $\Omega$, a $t_r$ of 150 ns, and a $V_{DD}$ of 10 V.](image2)

![FIG. 3. Extracted time-resolved $V_{TH}$ of FD-HEMT with different frequencies from 200 kHz to 1 MHz under a $V_{GS}$ of (a) 3 V, (b) 4 V, (c) 5 V, and (d) 6 V.](image3)
lower than the quasi-static measurement value (1.67 V), and a similar phenomenon is reported in Refs. 16 and 21. With the increase in effective stress time, $V_{TH}$ shifts positively under all test conditions. Moreover, when $V_{GS}$ is low (e.g., 3 V), $V_{TH}$ decreases with the increase in frequency, as shown in Fig. 3(a). However, this trend will be reversed with the increase in $V_{GS}$ as shown in Figs. 3(b)–3(d). The difference in $V_{TH}$ among different frequencies will be more significant under high $V_{GS}$ levels.

Meanwhile, the PD-HEMT is characterized under the same conditions as FD-HEMT, as shown in Fig. 4, the $V_{TH}$ of 1.04 V extracted from the first pulse is also lower than the quasi-static value (1.55 V). When $V_{GS}$ is 3 V, as shown in Fig. 4(a), the dependence of $V_{TH}$ on stress time is the same as FD-HEMT. However, under a $V_{GS}$ of 4 and 5 V, a non-monotonous $V_{TH}$ dependence on stress time is observed for the PD-HEMT, as shown in Figs. 4(b) and 4(c). $V_{TH}$ exhibits a positive shift first, then $V_{TH}$ begins shifting negatively. It can be seen that $V_{TH}$ is insensitive to frequency and the maximum value of $V_{TH}$ decreases with the increase in frequency under a $V_{GS}$ of 4 V. Nevertheless, under a $V_{GS}$ of 5 V, $V_{TH}$ is sensitive to frequency, and a higher maximum value of $V_{TH}$ can be obtained at a higher frequency, but when $V_{TH}$ reduces to a stable value, $V_{TH}$ will decrease with the increase in frequency. Moreover, at 6 V gate bias, the reduction process of $V_{GS}$ will disappear and $V_{GS}$ increases with the stress time, as shown in Fig. 4(d).

Interestingly, it is worth noting that the $V_{GS}$ range that $V_{TH}$ exhibits different behaviors between FD- and PD-HEMT overlaps the $V_{GS}$ range that $C_{th}$ of PD-HEMT decreases with $V_{GS}$ which is not found in FD-HEMT. Therefore, it can be inferred that the distinct $V_{TH}$ behaviors of PD-HEMT may originate from the electrically floating p-GaN layer and the extension of the depletion region in the p-GaN layer, which can induce the complex competition among the hole accumulation effect at the p-GaN/AlGaN interface, the electron/hole trapping effect, and the hole insufficiency effect.

When the DUTs are turned on with high $dV_{GS}/dt$, $C_{th}$ and $C_{pin}$ will be charged the same charges for both FD-HEMT and PD-HEMT ($V_{GS} \sim V_{TH}$), because displacement current dominates the gate current ($I_d$), and holes will accumulate at the p-GaN/AlGaN interface as shown in Figs. 5(a) and 5(d). Nevertheless, $I_d$ is dominated by electron/hole current and limited by the reverse-biased p-GaN/AlGaN diode ($D_{pin}$) under the quasi-static case, so the charges stored in $C_{th}$ are fewer than the case of high $dV_{GS}/dt$ with the same charges stored in $C_{pin}$. Therefore, the $V_{TH}$ of SP-HEMT under high-frequency operation is lower than the value under the quasi-static case due to the enhanced hole accumulation at the p-GaN/AlGaN interface, which is more significant at the lower rise time.

As the DUTs are turned ON fully, the gate stress bias is applied to the DUTs. The PD-HEMT and PD-HEMT will exhibit different behaviors, as shown in Figs. 5(b) and 5(c). At a gate stress bias of 3 V, electron trapping dominates the $V_{TH}$ shifts. For FD-HEMT, holes in the p-GaN layer are depleted fully, and electrons can spill over the AlGaN barrier, some electrons will be trapped by the pre-existing traps, as shown in Fig. 5(b), which can result in the ionization of acceptor traps and de-ionization of donor traps, and the net negative charge will increase. When DUTs are switched back to the recovery state, the trapped electrons cannot be released immediately, which results in extra negative charges in the gate stack, as shown in Fig. 5(c). Therefore, $V_{TH}$ increases with the stress time, and higher frequency will lead to lower $V_{TH}$ because part of the electrons cannot complete the trapping process with low-stress time in a period, as shown in Fig. 3(a). During the recovery state, the depletion region is expected to shrink; however, under high $V_{GS}$, the hole insufficiency effect becomes non-negligible, which is caused by the rectifying property of the p-GaN/AlGaN/GaN pin diode ($D_{pin}$). A shorter OFF-state time can enhance the hole insufficiency, as a result, $V_{TH}$ increases with the frequency, as shown in Figs. 3(c) and 3(d).

For the PD-HEMT, when DUTs are switched to the stress state, at a $V_{GS}$ of 3 V, the electron trapping effect is similar to FD-HEMT, which results in the positive shift of $V_{TH}$, as shown in Fig. 4(a). Nevertheless, as shown in Figs. 4(b) and 4(c), the distinct reduction of $V_{TH}$ can be observed at a $V_{GS}$ of 4 and 5 V, which cannot be explained by the hole injection and trapping, because it is widely reported that the hole injection and trapping become significant for SP-HEMT when $V_{GS}$ is above 5 V. Meanwhile, the hole trapping will be enhanced at higher $V_{GS}$ which is expected to induce the significant reduction of $V_{TH}$ at a $V_{GS}$ of 6 V; however, the measurement exhibits an opposite result, as shown in Fig. 4(d). Therefore, the distinct $V_{TH}$ behaviors related to the high $dV_{GS}/dt$ are not suitable to be explained by the hole trapping effects under the high-frequency operation. When the DUTs are turned on with high $dV_{GS}/dt$, the holes will accumulate at the p-GaN/AlGaN interface, then the accumulated holes will redistribute in the non-depleted p-GaN layer in the ON-state (stress state), as shown in Fig. 5(e), the density of accumulated holes decreases gradually, because the domination mechanism of $I_d$ changes from displacement current to electron/hole current, meanwhile, the depletion region will further extend and more electrons can be trapped in the extended depletion region. Nevertheless, the hole density cannot recover to the value of the equilibrium state during the ON-state due to the high frequency, so the holes required to shrink the depleted region can be provided by the accumulated holes at the p-GaN/AlGaN interface in the recovery state, and the excessive hole will accumulate at the p-GaN/AlGaN interface consecutively with the increase in period number. Therefore, the abnormal reduction of $V_{TH}$ will be induced when the accumulated holes are comparable to the trapped holes.
electrons, as shown in Figs. 4(b) and 4(d). However, when $V_{GS}$ is high enough (e.g., 6 V), more holes are required to shrink the depletion region when DUTs are turned off, which will induce significant hole insufficiency, and $V_{TH}$ will increase due to the increased negative charges in gate stack, as shown in Fig. 4(d). The TCAD simulation is adopted to support the proposed hole accumulation at the $p$-GaN/AlGaN interface induced by the high $dV_{GS}/dt$. As shown in Fig. 6, it can be seen that the density of the hole decreases gradually and then saturates over a relatively long time, which can also indicate that the $V_{TH}$ of SP-HEMTs under high-frequency operation is lower than the quasi-static value.

In conclusion, under high-frequency operation, the $V_{TH}$ of SP-HEMTs is lower than the quasi-static value due to the more holes charged in $C_{pin}$. For FD-HEMT, $V_{TH}$ increases with the stress time consistently, which can be attributed to the electron trapping effect. However, for PD-HEMT, hole accumulation at the $p$-GaN/AlGaN interface leads to a non-monotonic dependence of $V_{TH}$ on stress time. Notably, at high $V_{GS}$, the hole insufficiency becomes significant, resulting in a monotonic increase in $V_{TH}$. These distinct $V_{TH}$ behaviors of FD- and PD-HEMT should be considered meticulously to optimize the gate driver.

![FIG. 5. Schematic band diagram across the gate stack of FD-HEMT (a) at a $V_{GS}$ of $\sim V_{TH}$, (b) ON-state, and (c) OFF-state, and of PD-HEMT (d) at a $V_{GS}$ of $\sim V_{TH}$, (e) ON-state, and (f) OFF-state.](image)

![FIG. 6. Simulated hole density at the $p$-GaN/AlGaN interface of PD-HEMT after the $V_{GS}$ rise section.](image)
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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

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Bo Zhang: Data curation (supporting); Methodology (supporting).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

REFERENCES


