Development of high-yield and high-reliability design for high-performance ultra large scale 3DLSI processor

Hideki Kitada[1)], Osamu Moriyama[1)], Gen Oshiyama[1)], Akihiro Chiyonobu[1)], Hideaki Nabekura[1)], Takahiro Shikibu[1)], Koichi Yoshimi[1)], Shinji Tadaki[1)], Takumi Masuyama[2)], Naoaki Nakamura[2)], Norio Kainuma[2)], Seiki Sakuyama[1)], Tatsumi Nakada[1)]

1) FUJITSU LIMITED
2) FUJITSU ADVANCED TECHNOLOGIES LIMITED

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Performance Development by More than Moore

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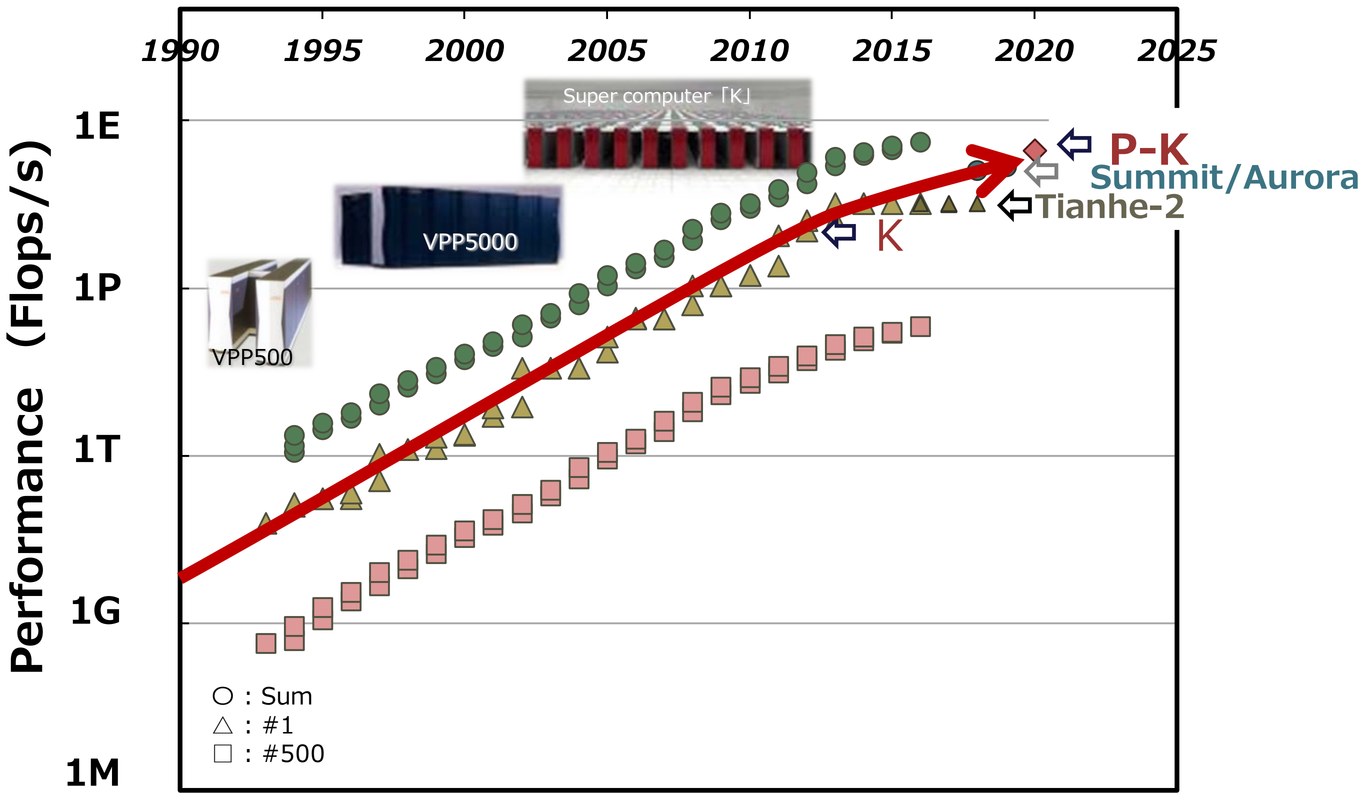
- The performance gain of super computing system has become slowdown



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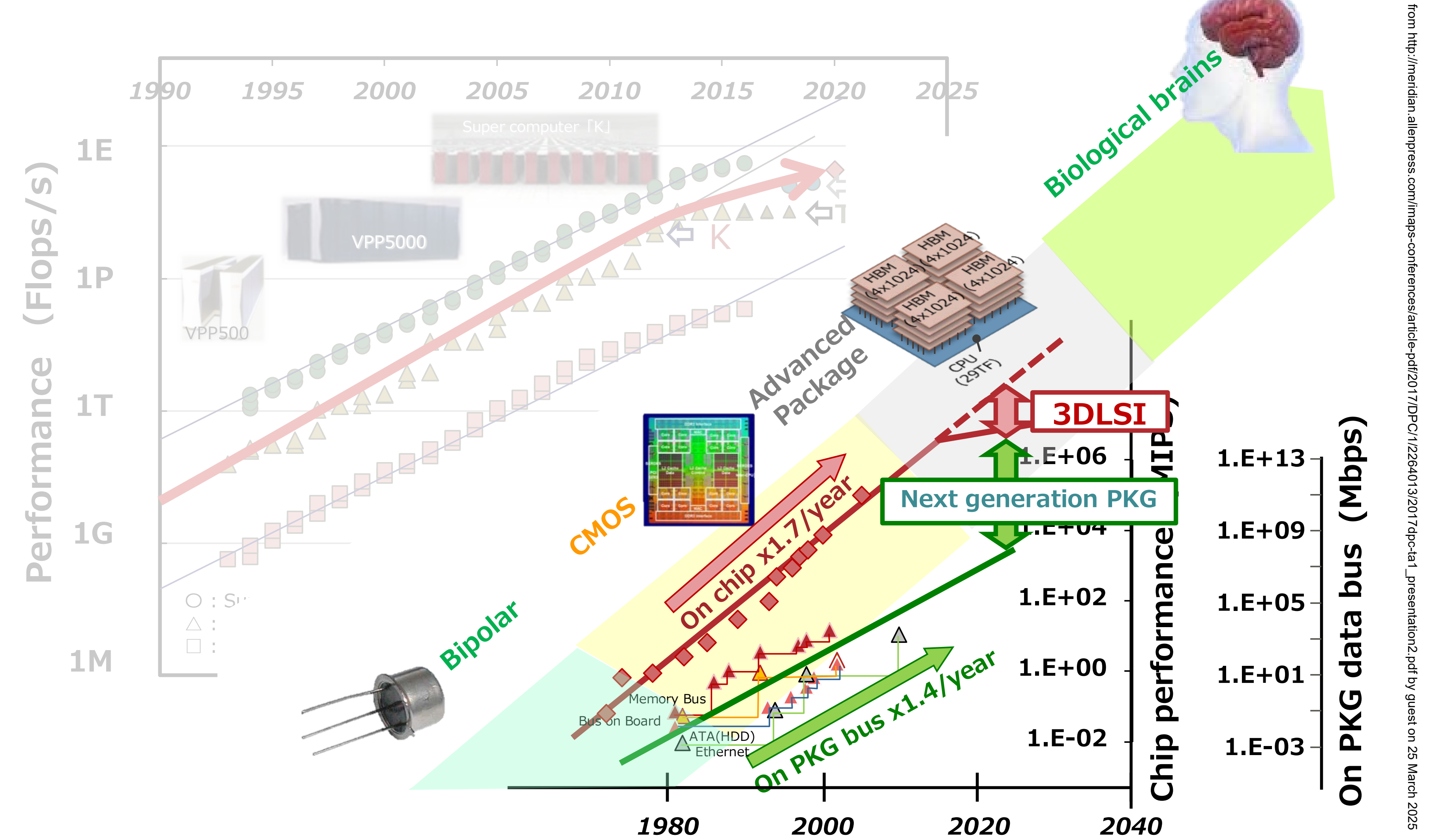

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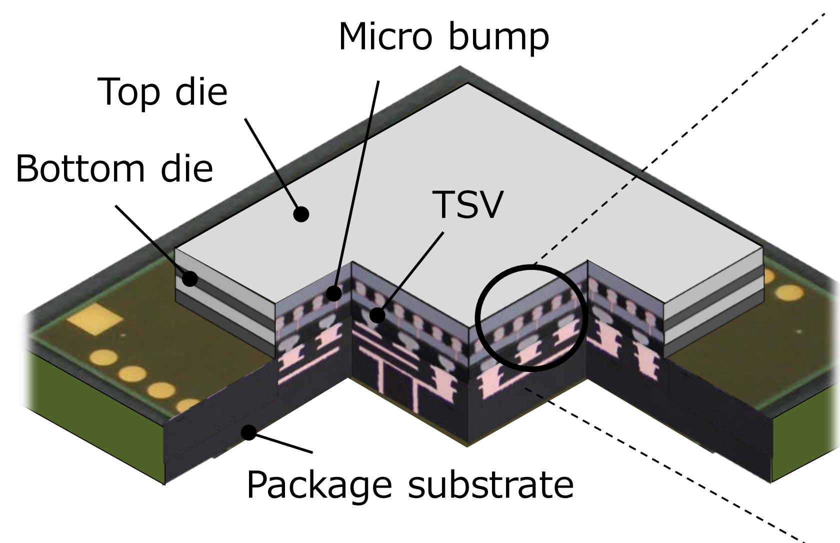
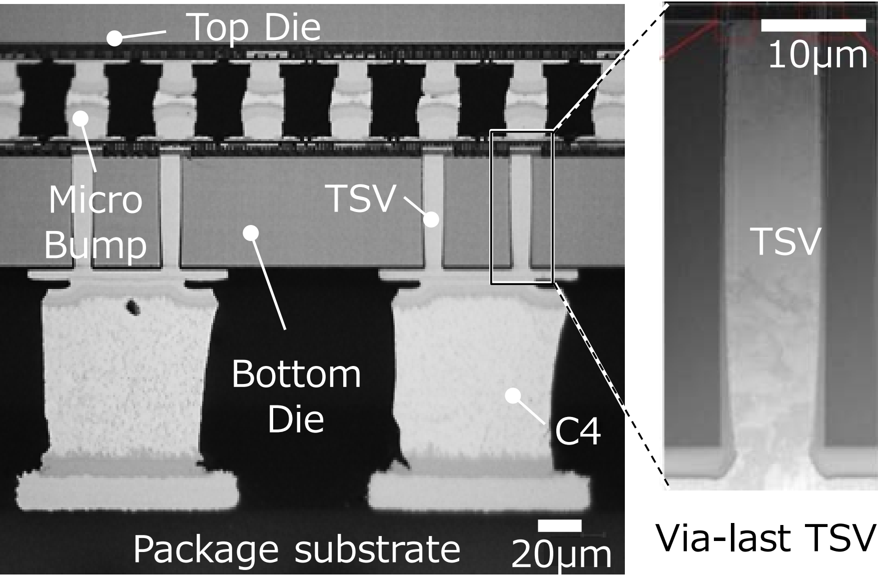
Fujitsu 3D-LSI development

- For high-end server and HPC systems

3D LSI packaging



Cross sectional image



- Development approaches

Module technology items	Comventional technology	Developed technology
TSV backside process	>300 µm: 10 x 10 mm chip	<50 µm: >23 x 23 mm chip
C4 bump tolerable current	25 mA	>100 mA
µ-bump material	<10 mA/bump: SnAg material	>50 mA/bump: IMC material
Stacked die area	100 mm^2	>500 mm^2
Number of µ-bumps	150,000	300,000
TSV transmission performance	20 GHz	40 GHz

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Basic circuit configuration of 3D processors

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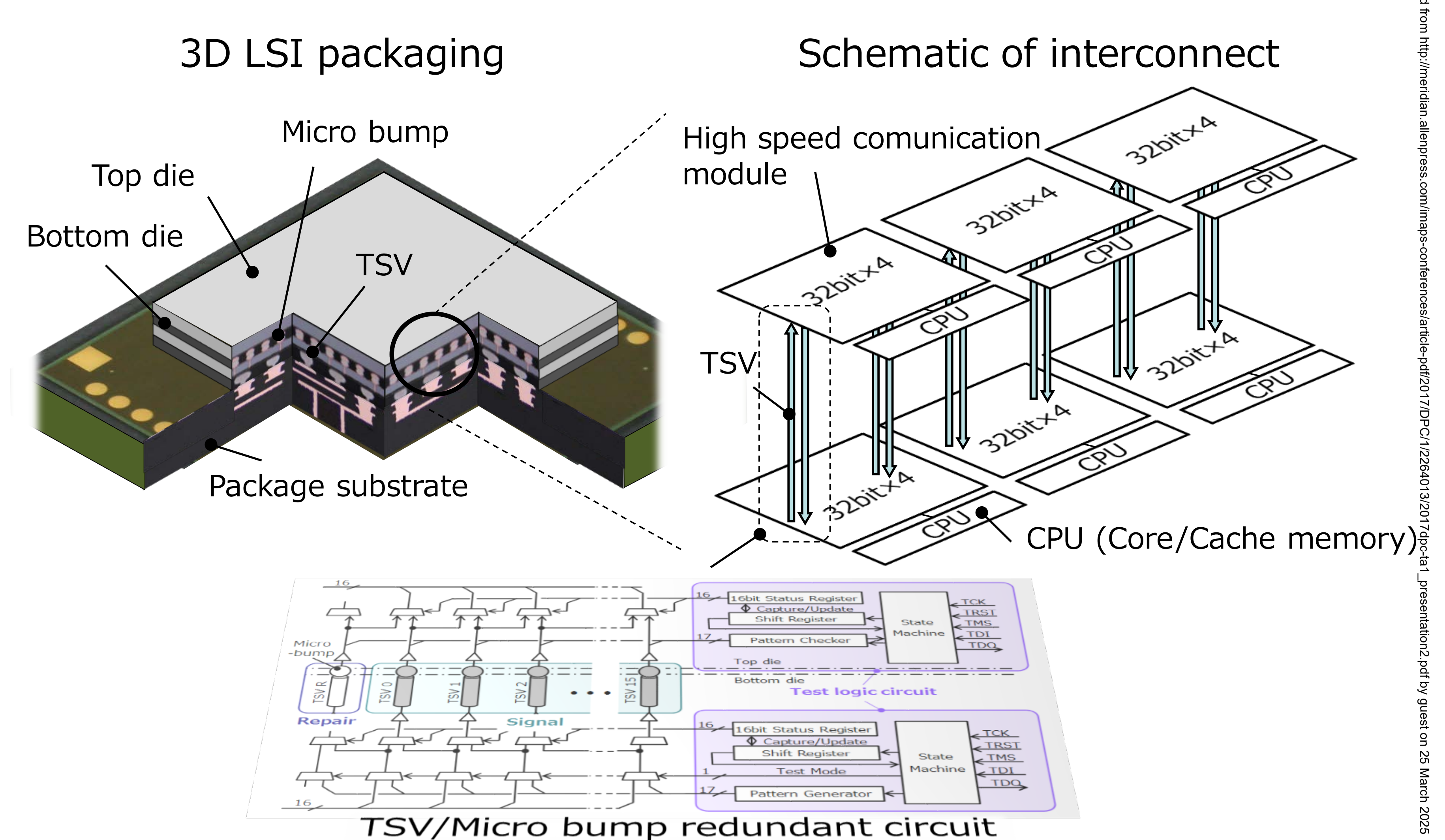
- For high-end server and HPC systems



TSV/Micro bump redundant circuit

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3DLSI development approaches

- Aims at a higher yield and reliability

- Most important point is a collaborative design with the redundant circuit which aimed at the product level reliability.

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Today's topics

- TSV yield improvement
- Micro-bump reliability of large die stacking
    - EM tolerance
    - TC life time
- Redundancy circuit configuration with reliability

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Yield improvement

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Via last TSV and back-side process flow

Bottom die formation

FEOL/BEOL
65nm Device fabrication

Si substrate

Bump formation process

Si substrate

Temporary bonding process
Wafer thinning process

Support wafer

TSV formation process

TSV

Back-side RDL formation

PI dielectric

RDL

De-bonding process
Dicing process

Support wafer

Die stack and PKG

Die stack process

Top die

Bottom die

Packaging

PKG substrate

- To investigate TSV high yield fabrication, conventional Via-last 10-µm TSV and micro-bump processes were employed.

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TSV yield improvement

- TSV thermal stability (TC)

TC: RT-400℃ anneal

Enough Ti ×1 ANL

Poor Ti

×1 ANL

×5 ANL

Probability (%)

99.99
99.9
99
90
50
10
1
.1
.01

0.1
1
10
100

Resistance increase ratio

I
V
TSV
BEOL M1 Pad

Failure analysis

TSV
Slit
M1
Low-k
M2
MN
-23MPa
880MPa

TEOS SiO2
TSV
Si
Crack
SiO_2
Cu(M1)
Low-k
600nm

SEM image after ×5 ANL

Kitada et al. ECTC2015,EPTC2016

- High TSV process yield (>99%) was achieved by using of the thermal stability examination.

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Reliability of micro-bump

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Micro-bump reliability of large die stacking

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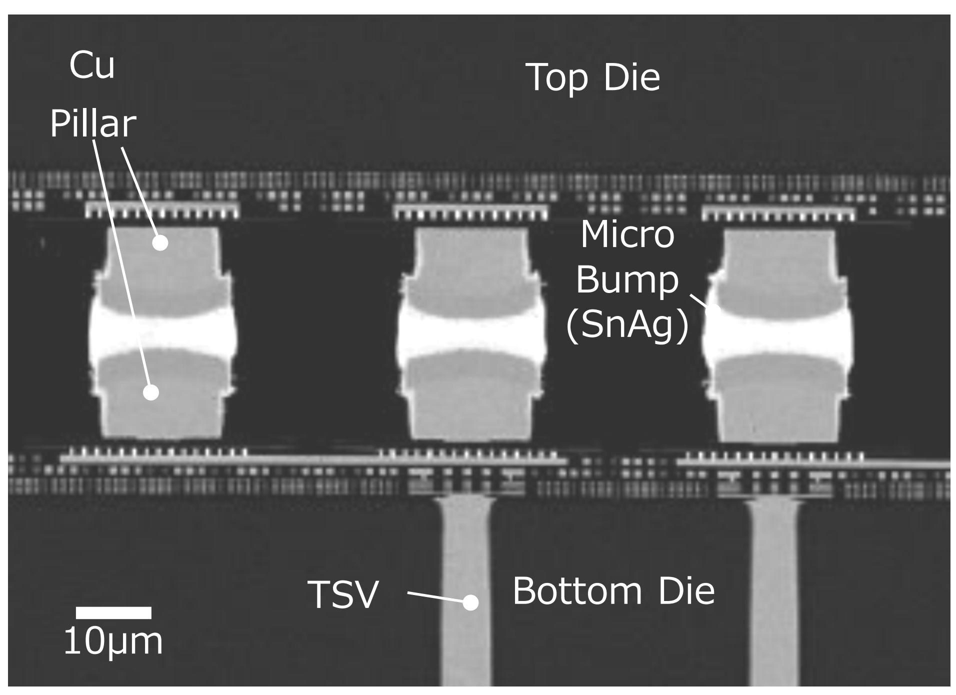
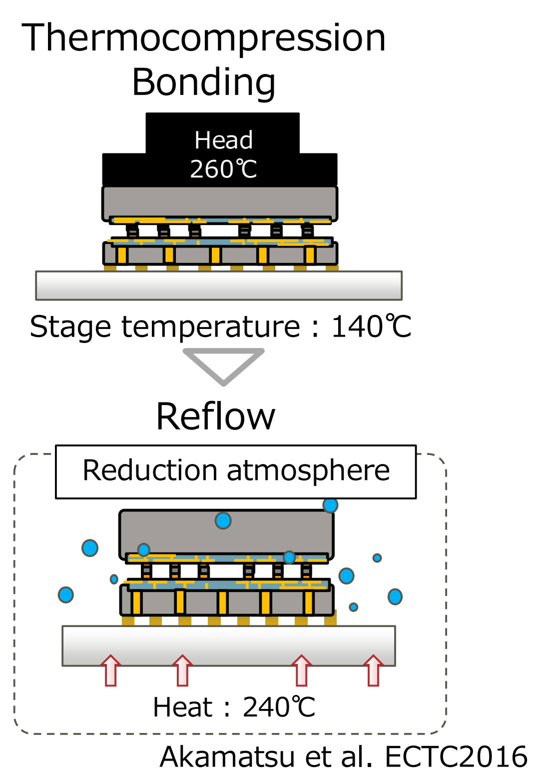
- Cross sectional SEM image and process flow in micro-bump stacking





Akamatsu et al. ECTC2016

- Flux-less reducing atmosphere in order to improve the micro bump interconnection with high accuracy.
- Micro bumps at 40 μm pitches were formed on to a 23 mm square size stacking chip, achieving an ultra-high pin junction of more than 290,000 pins.

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Micro-bump reliability – Electro migration

- Improvement of higher current tolerance with IMC material

Micro bump

Top die
Cu
Ni
e
Cu_6Sn_5
IMC
No failure
Cu_3Sn
Bottom die
Cu
10µm

Top die
e
Micro bump
40µm
Bottom die
C4 bump
80µm
PKG substrate

C4 Bump

TSV
Top die
Failure
e
Solder
Cu_6Sn_5
Ni
Substrate
Cu
10µm

EM: 600mA,2000h

- The EM tolerance of the IMC material is higher than a conventional SnAg material. It's an increase in the current density can be expected.

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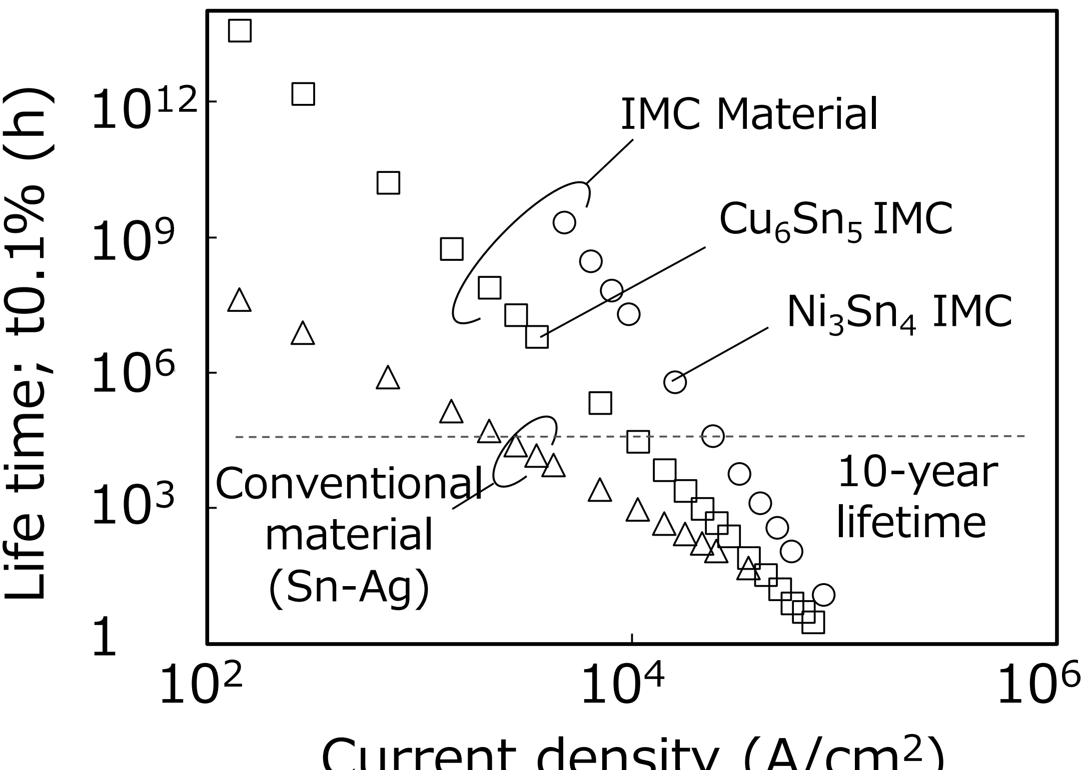
Micro-bump reliability – Electro migration

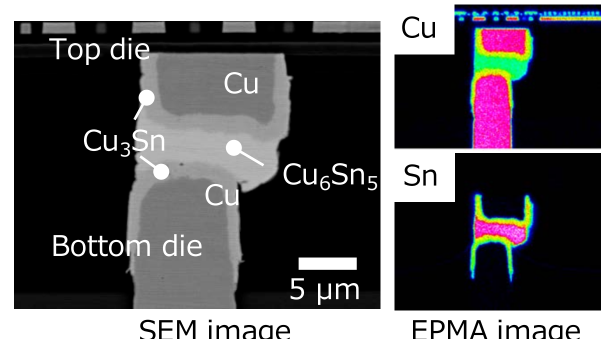
- Relation between IMC material kind and resistance of EM

EM Life time of IMC micro-bump



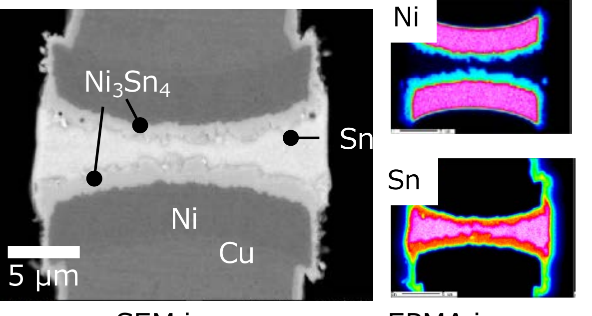
EPMA analysis image of IMC

Cu-Sn IMC



SEM image EPMA image

Ni-Sn IMC



SEM image EPMA image

- The Ni_3Sn_4 alloy demonstrated ten times high longevity.

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Thermal stability of 3D stacking structure

Thinned die deformation

TC deformation

Top die

Package substrate

Thin bottom die warpage

Si die,23mm□, 50μm thickness

Warpage: b (μm)

Equivalent film stress (MPa)

Inorganic (SiO_2)

Organic

Cylindrical

Isotropic

Target

b, b_1, b_2

structural parameters

Top die

Device side

Bottom die

Device side

C4

Package substrate

σ

Top die thickness

SiN/SiO

TEOS-SiO2

Low CTE UF material

Cu/SnAg/Cu

Organic film

SiN/SiO

Inorganic film

- Material and structural optimization that considers the influence of the thermal deformation of the PKG structure is important.

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Thermal stability of 3D stacking structure

■ Structural dependence of TC life time

TC life time

MTF (a.u.) vs. Top die thickness (μm)

Low CTE, High Modulus UF

Improved

×1.36

Conventional UF

Conventional

Top die

UF

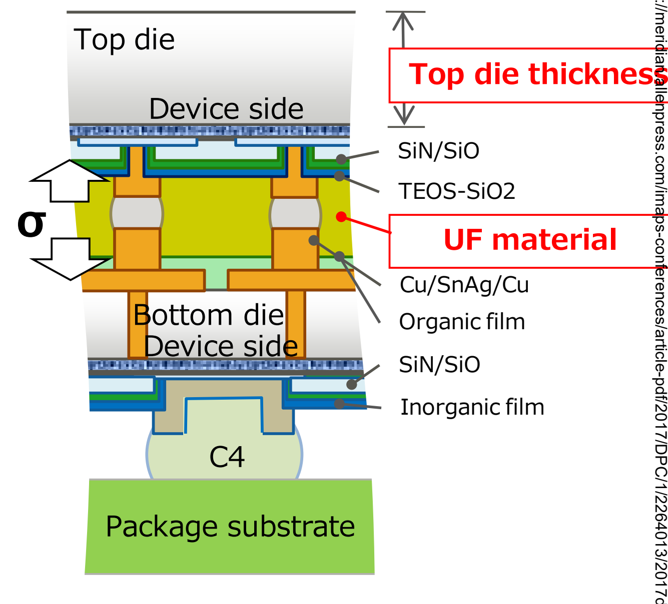
Bottom die

Package substrate

Top die thickness

TC : -55 to 125 ℃

Structural parameters



UF material properties

	CTE (ppm/℃)	E (Gpa)
Conventional	43	8.1
Improved	21	15.2

- The micro bump stress is the smaller in case of the lower total stiffness structure.

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Corroborate with redundancy circuit

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Redundant TSVs circuit

- Existing redundancy solutions

Source : Li Jiang

Switching | **Shifting** | **Crossbar** | **Router**

Die$_1$

Die$_2$

U. Kang, et al. *IEEE JSSC* 2010

A. C. Hsieh, et al. IEEE/ACM DATE 2010

Loi, et al. IEEE/ACM ICCAD 2008

L. Jiang, et al. IEEE/ACM DATE 2012

Signal TSV | Redundant TSV | Signal Pad | 1-2 Switch | Router | 1-3 Switch

- Signal-shifting solution

  - Repair efficiency of signal-shifting scheme is less than other solutions.
  - Simple structure, lower area penalty and lower cost .
  - TSV and micro-bump recovery using self- test with post die stacking.
  - Self-test sequence can be performed only once, and a reduction in the test time.

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Our approach for redundant TSVs circuit

Schematics of shifter redundant TSVs/Micro-bump

16
16bit Status Register
Capture/Update
Shift Register
State Machine
17
Pattern Checker
TCK
TRST
TMS
TDI
TDO
Top die
Micro -bump
TSV R
TSV 0
TSV 1
TSV 2
TSV 15
Bottom die
Test logic circuit
Repair
Signal
16
16bit Status Register
Capture/Update
Shift Register
State Machine
1
Test Mode
17
Pattern Generator
TCK
TRST
TMS
TDI
TDO
Vdd, Signal
16

- TSV and micro-bump recovery using self- test with post die stacking
- Self-test sequence can be performed only once, and a reduction in the test time

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Our approach for redundant TSVs circuit

- Redundant TSV self test

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Our approach for redundant TSVs circuit

- Fault free mode

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Our approach for redundant TSVs circuit

- TSV/Micro-bump repair mode

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Considering of redundancy for reliability

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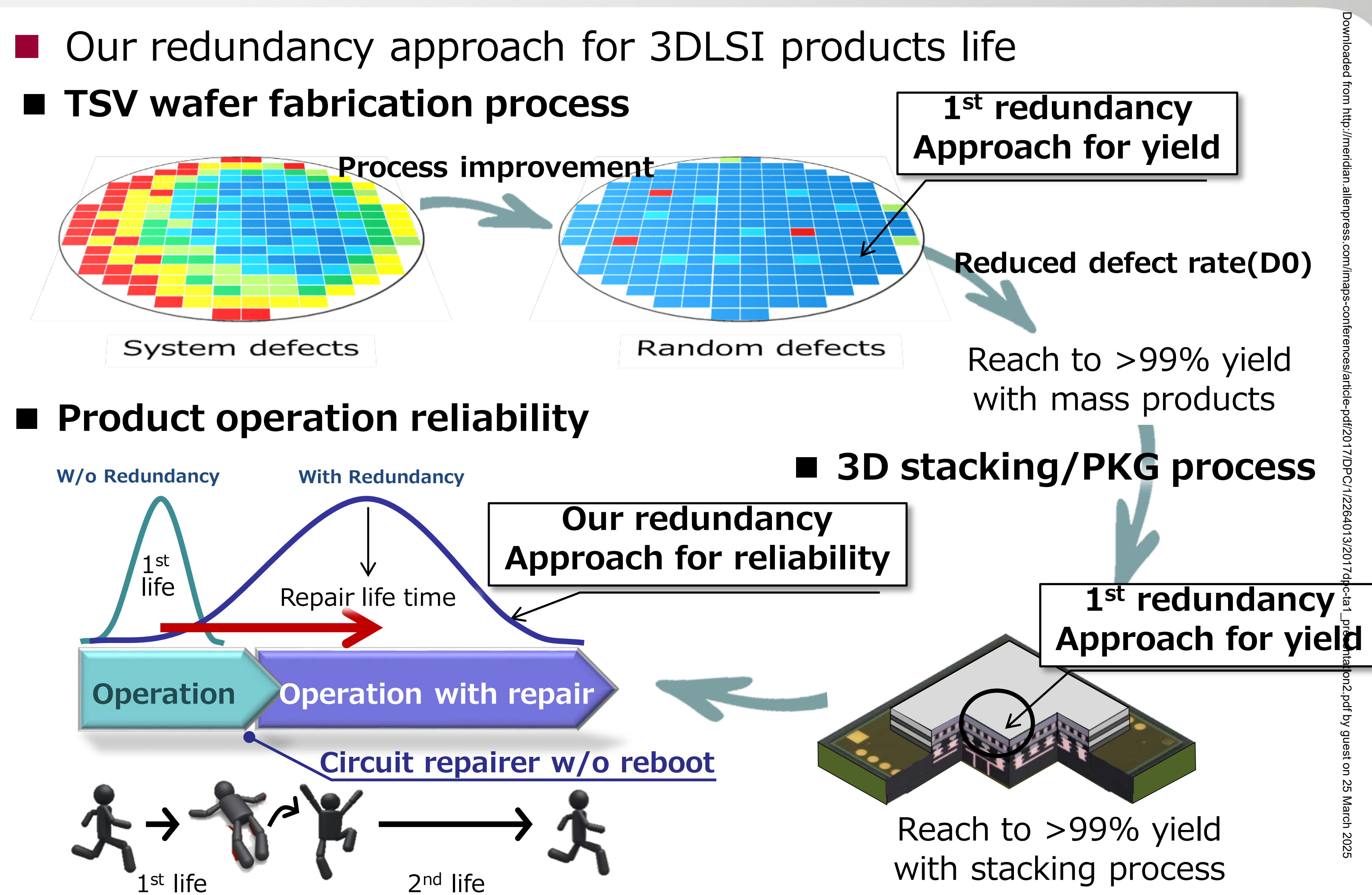

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TSV/Micro-bump life time with Redundancy

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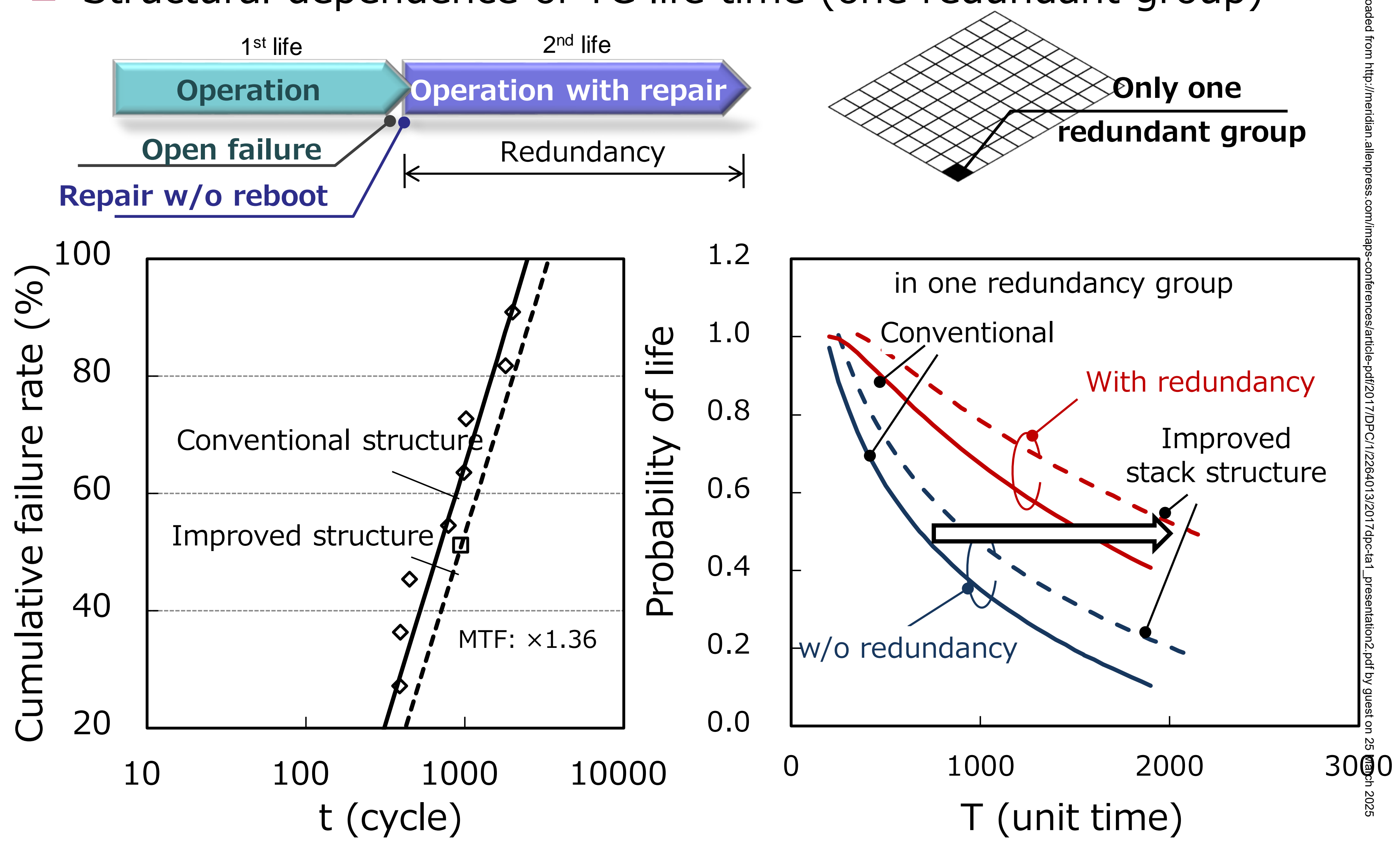
- Structural dependence of TC life time (one redundant group)



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TSV/Micro-bump life time with Redundancy

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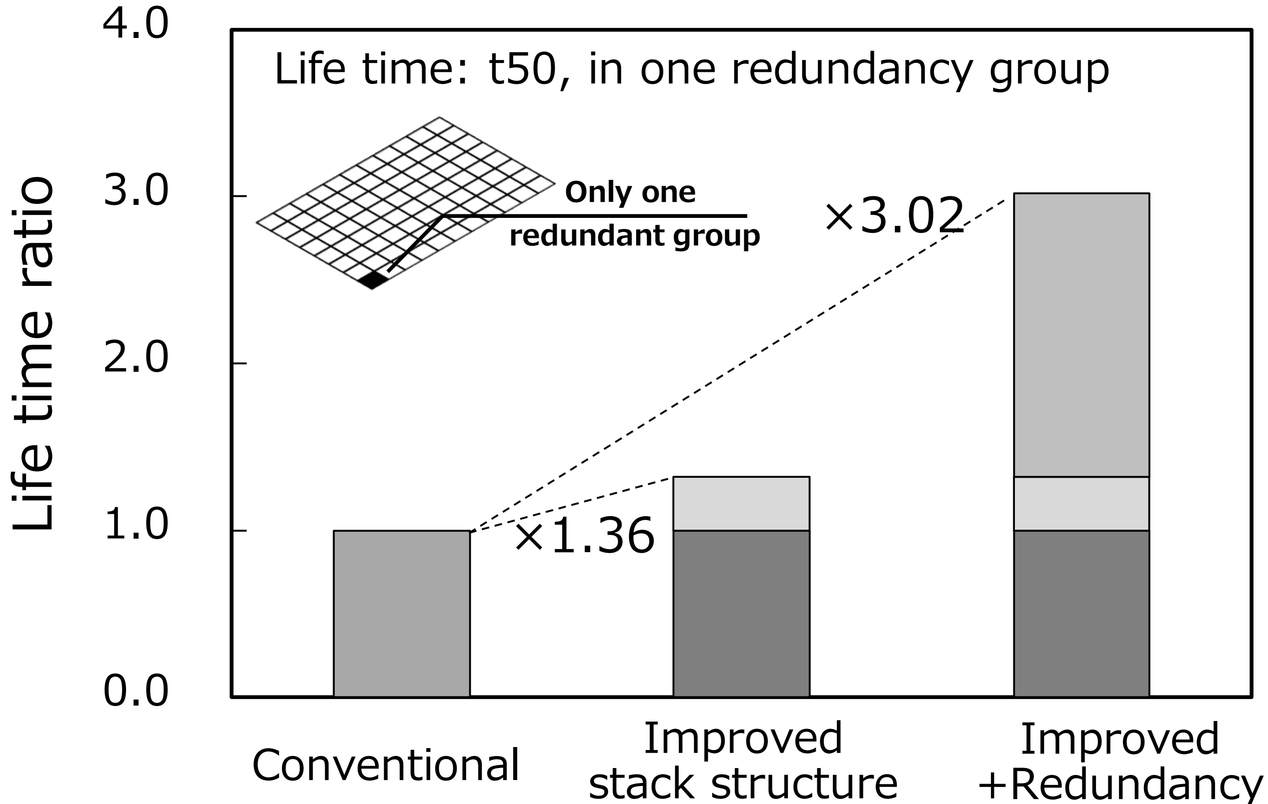
- Operation life time with optimized structure and redundancy



- When the redundancy is included by 1.36 times in the improvement structure, about three times further the lifetime improvement are possible.

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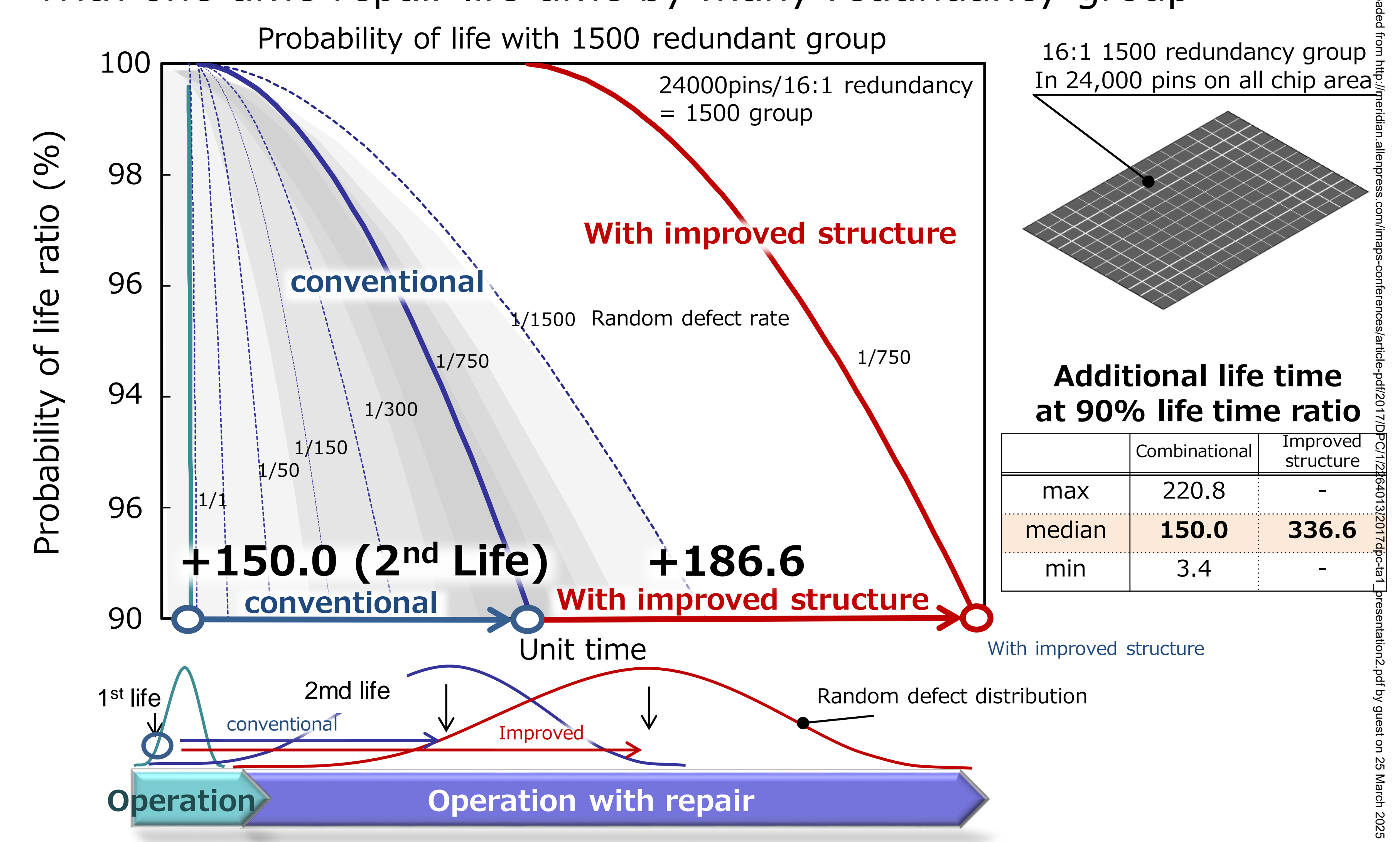
TSV/Micro-bump life time with Redundancy

- With one time repair life time by many redundancy group



Additional life time at 90% life time ratio

	Combinational	Improved structure
max	220.8	-
median	**150.0**	**336.6**
min	3.4	-

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TSV/Micro-bump life time with Redundancy

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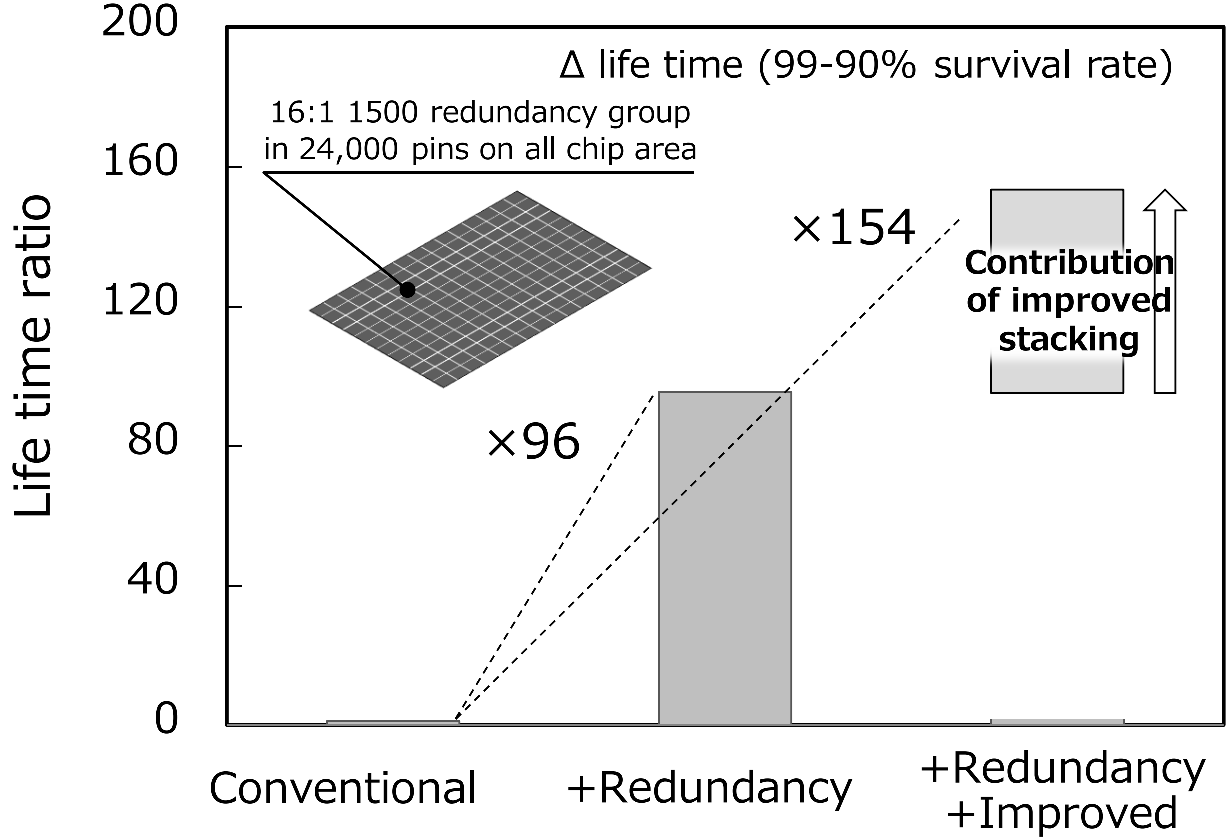
- Operation life time with optimized structure and redundancy



	Conventional	Redundancy	**Improved + Redundancy**
Δlife time (99-90%)	0.44	42.0	**67.6**
Ratio	1	95.5	**153.5**

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Total improvement with process and design

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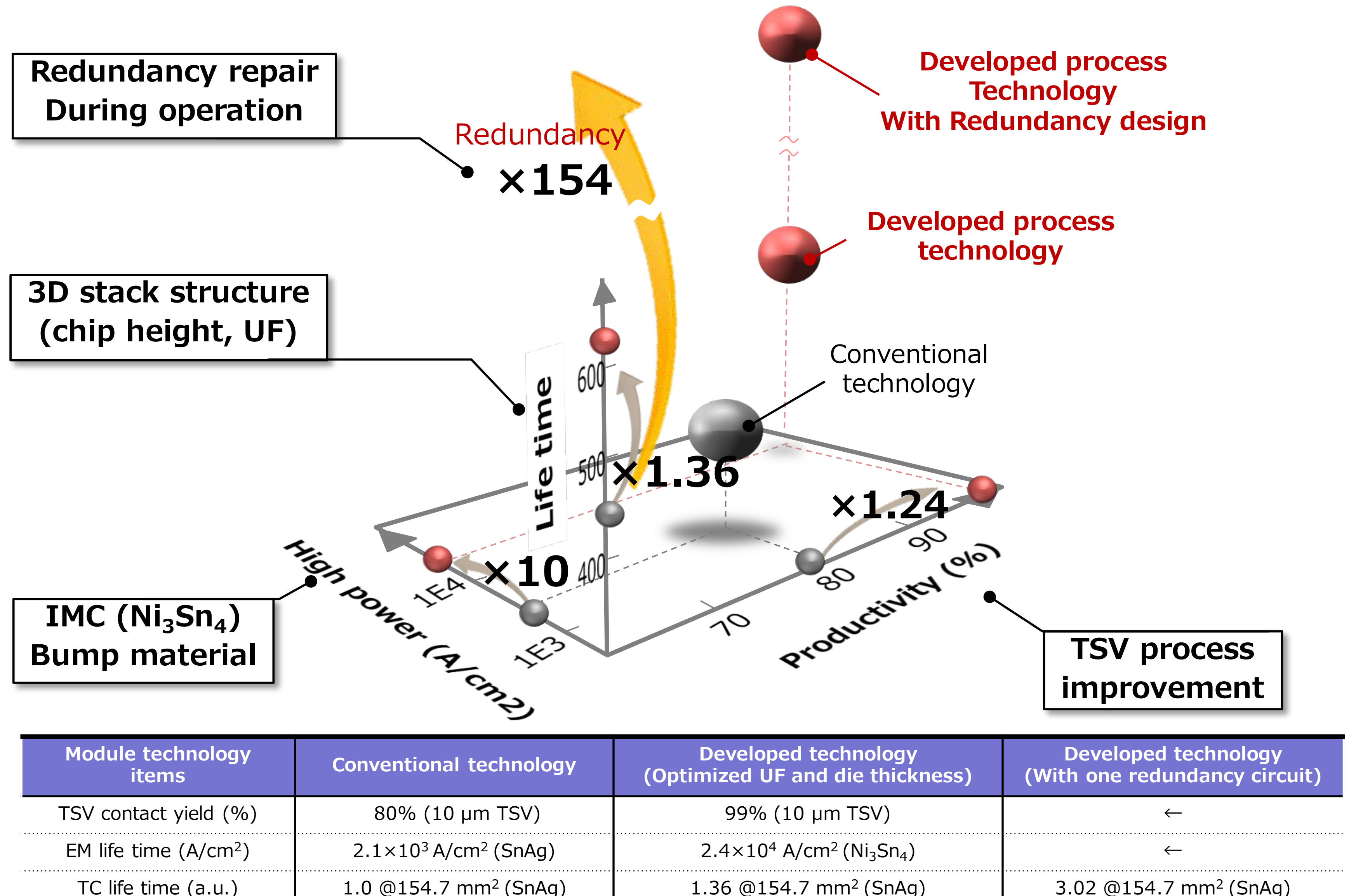

Module technology items	Conventional technology	Developed technology (Optimized UF and die thickness)	Developed technology (With one redundancy circuit)
TSV contact yield (%)	80% (10 μm TSV)	99% (10 μm TSV)	←
EM life time (A/cm^2)	2.1×10^3 A/cm^2 (SnAg)	2.4×10^4 A/cm^2 (Ni_3Sn_4)	←
TC life time (a.u.)	1.0 @154.7 mm^2 (SnAg)	1.36 @154.7 mm^2 (SnAg)	3.02 @154.7 mm^2 (SnAg)

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Summary

1. We developed
   - the integration of redundancy TSV/Micro bump design method
   - micro-bump material technologies

   for in 3D high-performance logic large scale processors.

2. We achieved high yield, high reliability and high power to use
   - intermetallic compound (IMC) alloy joining
   - High yield TSV process
   - Redundancy circuit

3. 3DI technologies will be able to about 154 time longer life time with real product operation.

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THE POSSIBILITIES ARE INFINITE

This work was carried out in the “Next Generation Smart Device Development Project” in conjunction with the New Energy and Industrial Technology Development Organization (NEDO).

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Uniform design

Based on co-design with reliability

Recommendation of redundant circuit design unified to occurrence frequency of defect

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