The effect of underfill on thermal stresses on logic ASIC and its electrical performance

Babak Talebanpour, Doug Link

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Outlines

- **Introduction**
  - ➢ **Thermo-mechanical stresses on logic ASIC and its effects**
- **Finite element analysis of stresses**
- **Experimental observations**
- **Summary**

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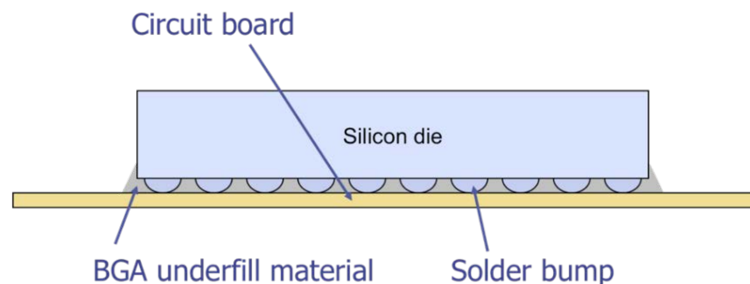
Thermo-mechanical stresses on flip chip assembly



Component	Material	CTE ppm/oC
Die	Si	2.6
Micro bumps	Sn-3%Ag-0.5%Cu	21.6
Underfill	UF1	41-120
Flex PCB	Polyimide	35

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Effect of Thermo-mechanical stresses on logic ASIC

Observations:

- **Nominal clock for an Starkey logic die is set at 10.24 MHz**
- **Maximum allowable clock shift ±0.25 %**
- **FC on flex circuits consistently show clock shift of above 1%, when exposed to heat events (solder reflow).**
- **1 week wait from fabrication to clock calibration reduces the shift significantly.**

Goals:

- **The cause(s) of clock shift,**
- **Minimize the clock shift.**
  - **Quick solutions.**
  - **Permanent solution for next gen products.**

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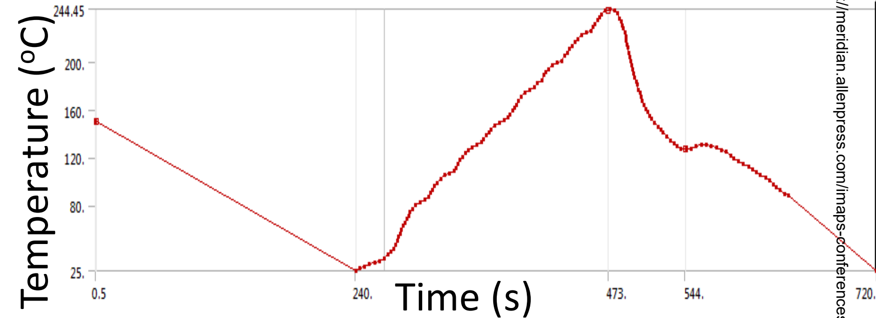
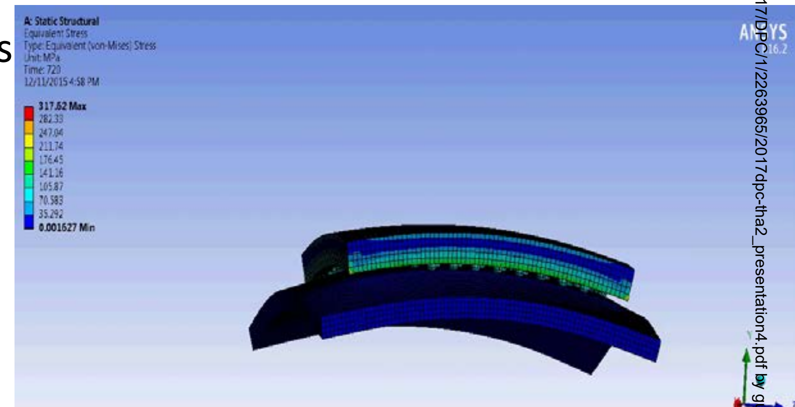
FE analysis

- Assumptions:

1. Perfect bonding for all contact surfaces,
2. The assembly is stress free at 150 ^{o}C (UF cure temperature),
3. No temperature gradient between components.
4. FE analysis/real life experiments on flip chip assemblies have shown the most important component of stress that adversely affects the clock is the normal (y) component.





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Effect of no underfill

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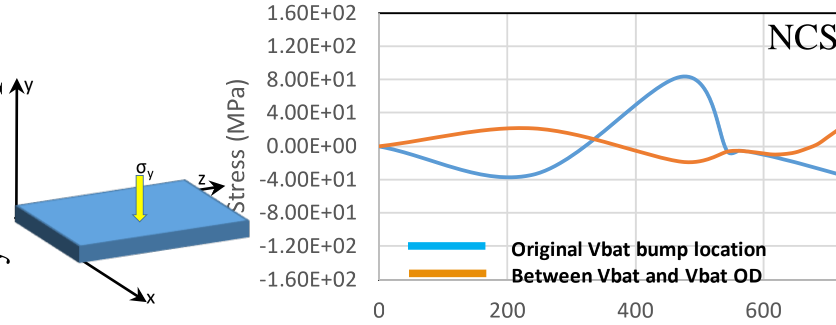
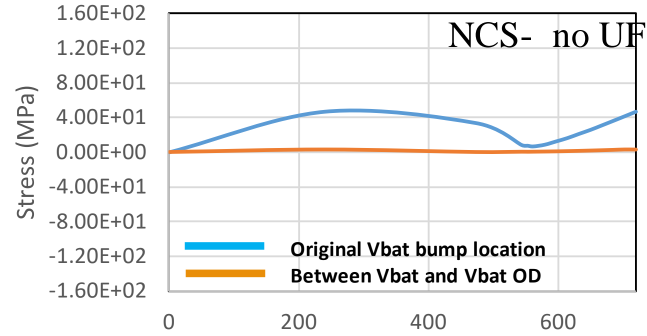
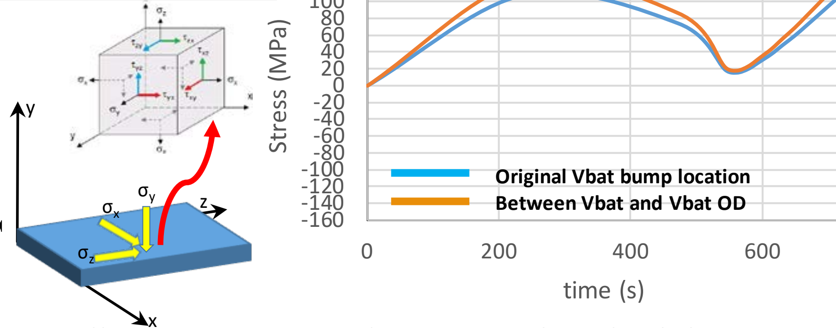
σ_y (out of plane)

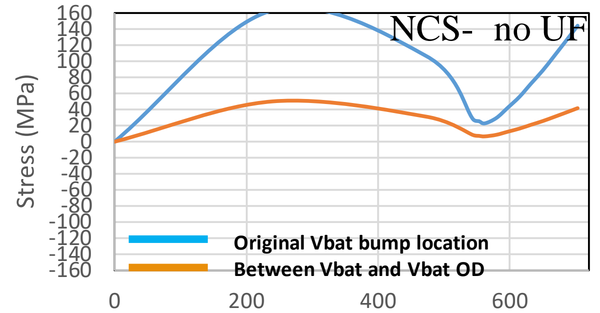




$$\sigma_{vM} = \sqrt{0.5\left[(\sigma_x-\sigma_y)^2+(\sigma_y-\sigma_z)^2+(\sigma_z-\sigma_x)^2\right] + 3(\sigma_{xy}^2+\sigma_{yz}^2+\sigma_{zx}^2)}$$

Equivalent





- smaller stresses on the die at the clock location, when UF is eliminated.
- UF reduces equivalent stress on the die, due to providing support against lateral loads on bump.

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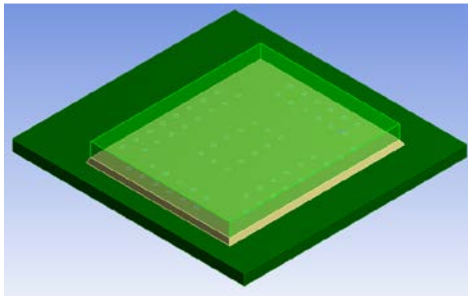
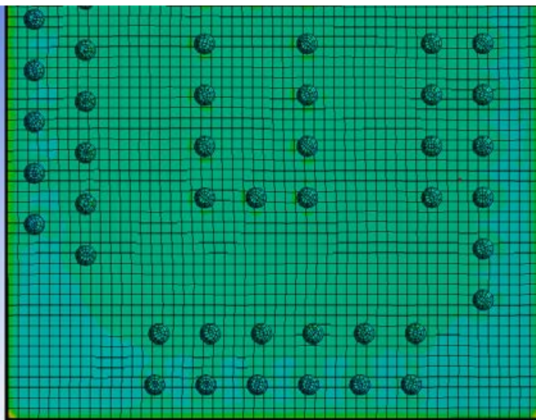
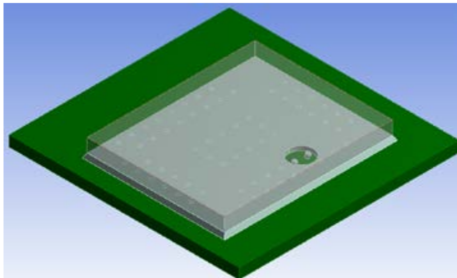
Evaluating the effect of voids

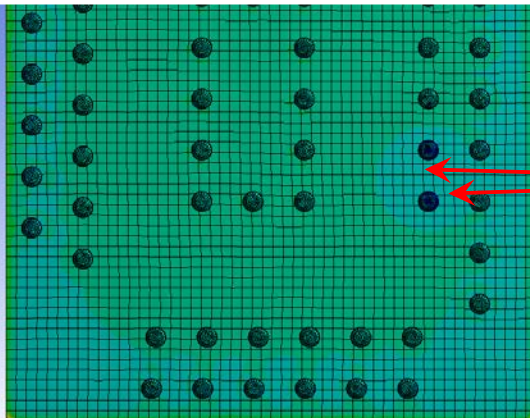
Underfill covers the whole die active layer side





UF with a void 450 microns in diameter around Vbat and Vbat O/D bumps.





Much lower stress levels on V bat and V bat O/D as well as the surrounding area.

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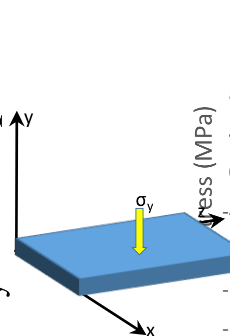
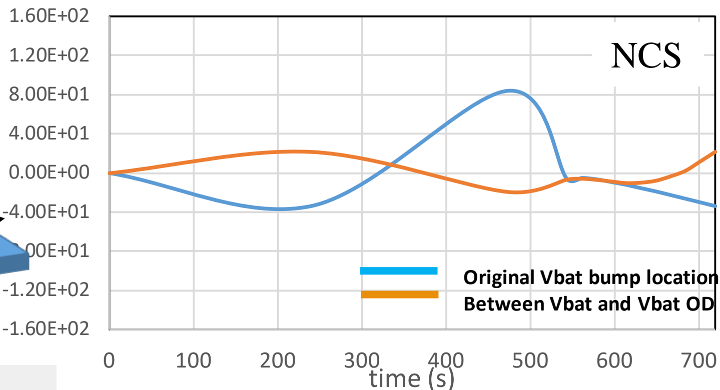
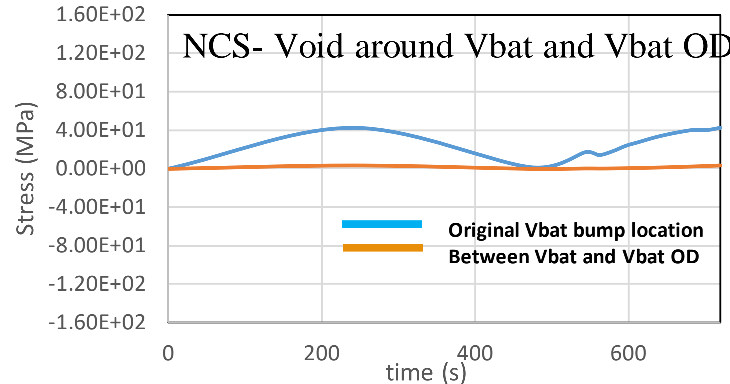
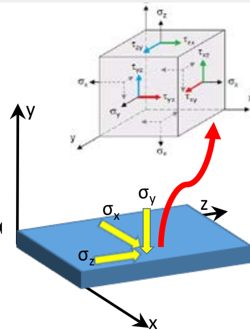
Effect of UF void on stress

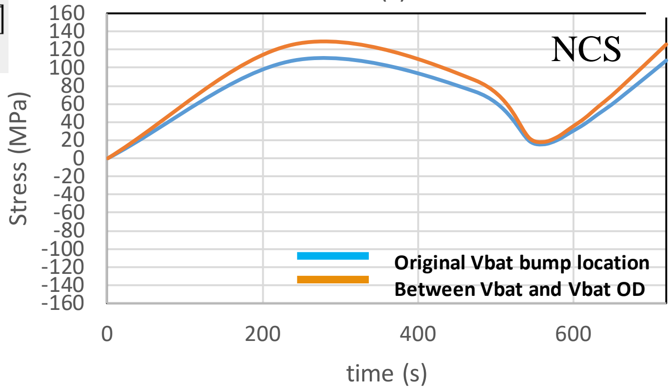


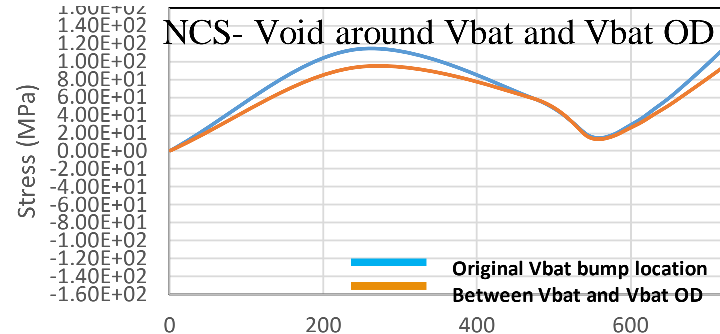




$$\sigma_{vM} = \sqrt{0.5\left[(\sigma_x-\sigma_y)^2+(\sigma_y-\sigma_z)^2+(\sigma_z-\sigma_x)^2\right] + 3(\sigma_{xy}^2+\sigma_{yz}^2+\sigma_{zx}^2)}$$







- much smaller stresses on the die at the original Vbat bump location or half way between Vbat and Vbat OD, when void exists around the clock circuit.
- Equivalent stresses are comparable.

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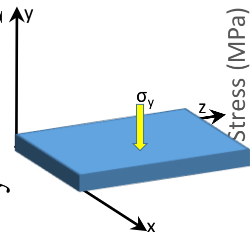
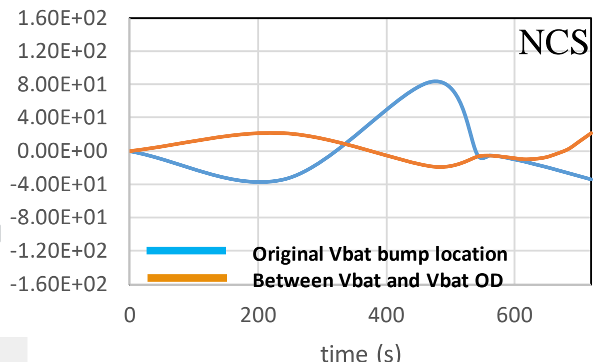
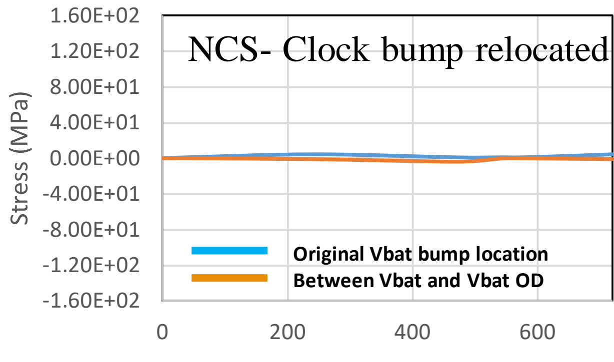
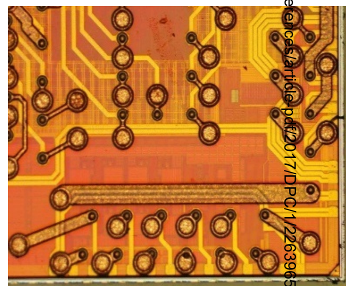
Effect of relocation of bumps

σ_y (out of plane)



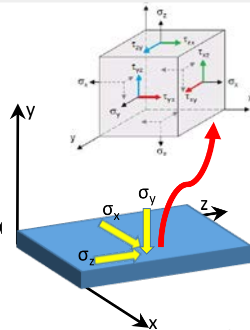


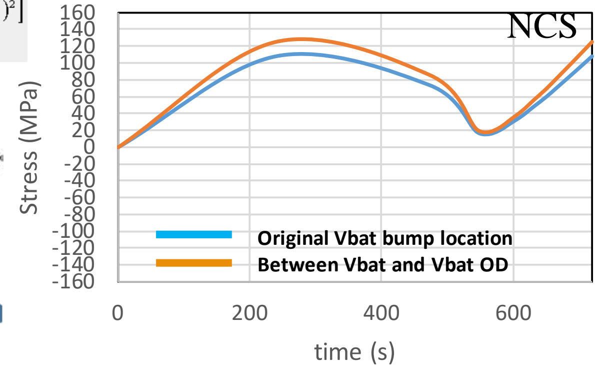


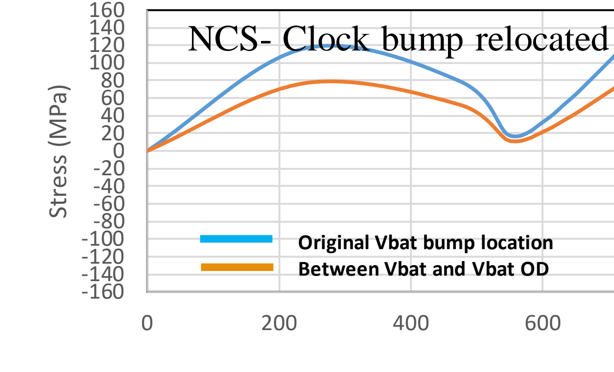


$$\sigma_{vM} = \sqrt{0.5\left[(\sigma_x - \sigma_y)^2 + (\sigma_y - \sigma_z)^2 + (\sigma_z - \sigma_x)^2\right] + 3\left(\sigma_{xy}^2 + \sigma_{yz}^2 + \sigma_{zx}^2\right)}$$

Equivalent







- Stress is probed at the original V bat location as well half way between Vbat and Vbat OD. Smaller stresses at both locations when Vbat is relocated according to NP5-S layout.
- Comparable values of equivalent stress.

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Effect of collapsing the bumps from 80 to 66µm

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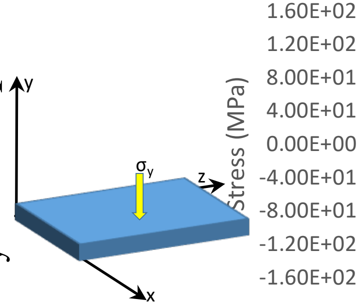
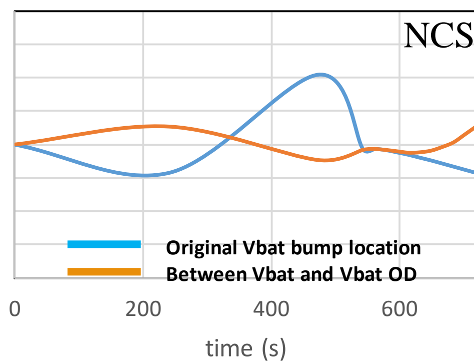
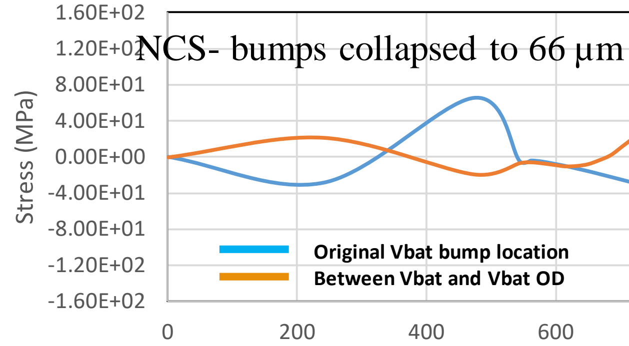
σ_y (out of plane)

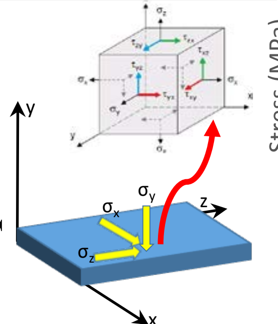


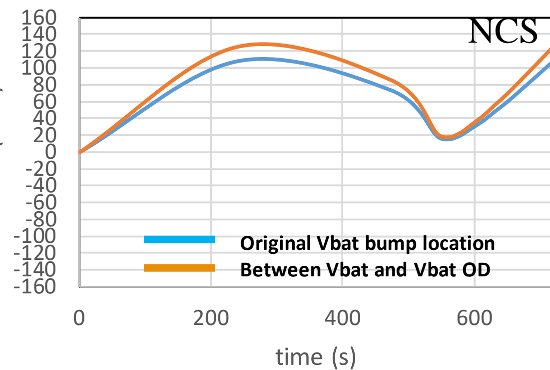


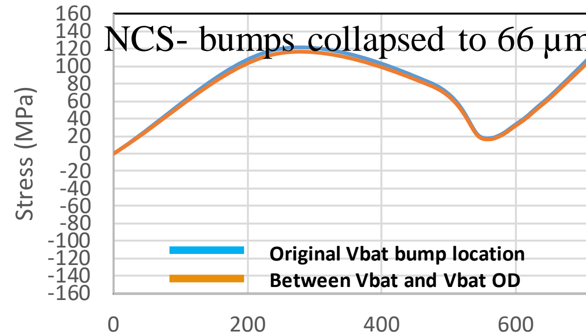


$$\sigma_{vM} = \sqrt{0.5\left[(\sigma_x-\sigma_y)^2+(\sigma_y-\sigma_z)^2+(\sigma_z-\sigma_x)^2\right] + 3(\sigma_{xy}^2+\sigma_{yz}^2+\sigma_{zx}^2)}$$

Equivalent







- Minimal decrease of stress when bumps are collapse 18 % of their height.
- Comparable values of equivalent stress.

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The effect of thickness

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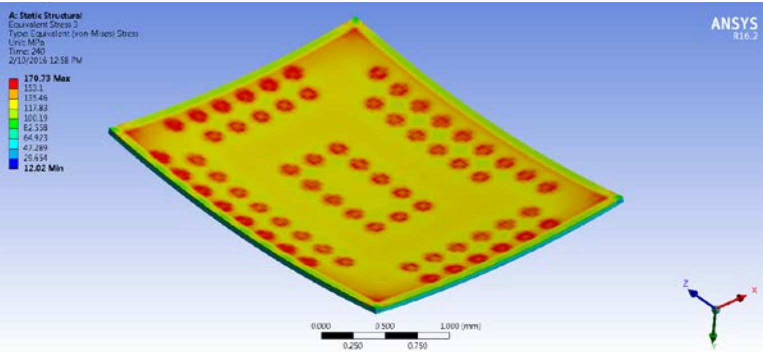

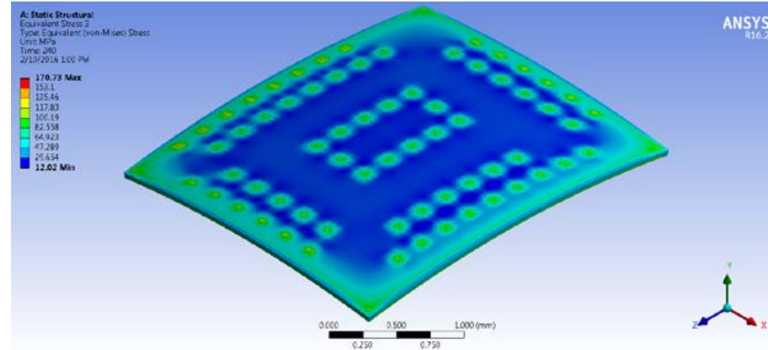

Eq Stress (MPa)

	254 µm thick die	100 µm thick die	50 µm thick die	Trend with decreasing thickness
Stress (Mpa)	317.62	225.63	170.73	↓
Deformation (mm)	0.020537	0.049953	0.06751	↑

- Thinner dies will carry less stress, but allow more deformation (more flexible).
- The stress and strain is more localized near the bump in thinner dies.

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FE analysis

- UF reduces equivalent stress on the die! But produces a large normal-to-the-die stress.
- Relocated bump significantly reduces stress at the clock location.
- A void around Vbat and Vbat OD bumps significantly reduces the normal stresses both at Vbat location and between Vbat and Vbat OD.
- Smaller bump height has little effect on the stresses.
- Thinner dies have more flexibility and less susceptible to stress build up.

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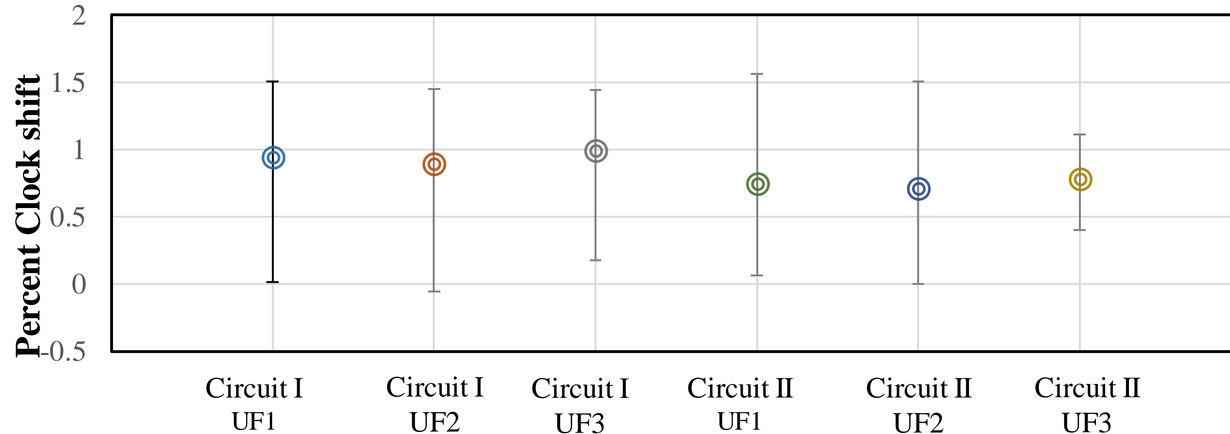
Experiments:

The effect of Underfill Material

- **3 different Ufs, tested on 2 circuits (with the same ASIC)**



- No significant difference between different materials or different circuits.

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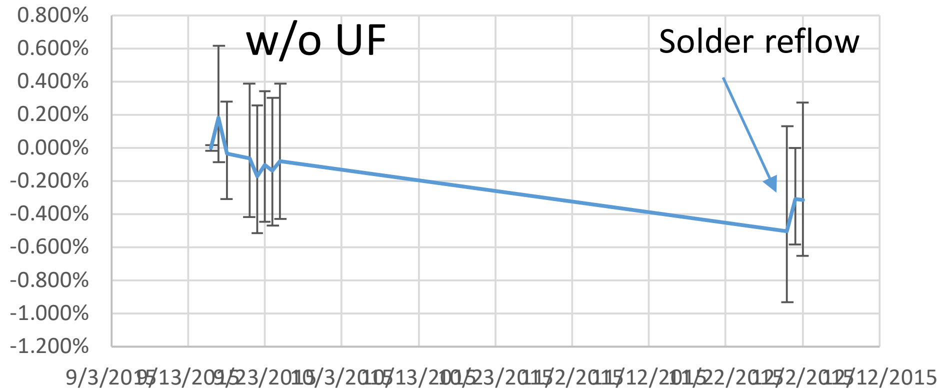
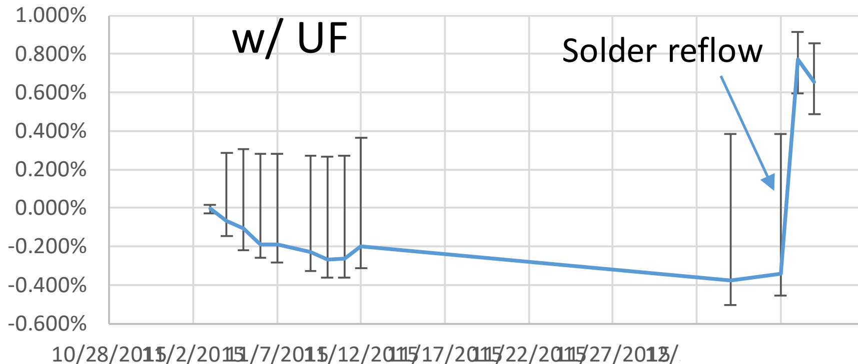
Experiments:

Underfill/no-underfill

- **Panels tested with and without UF**





- Large thermal stresses due to CTE mistmatch between Die-Solder-UF-substrate and high stiffness of UF

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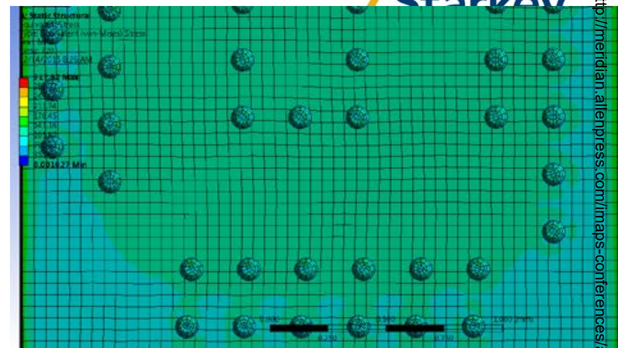
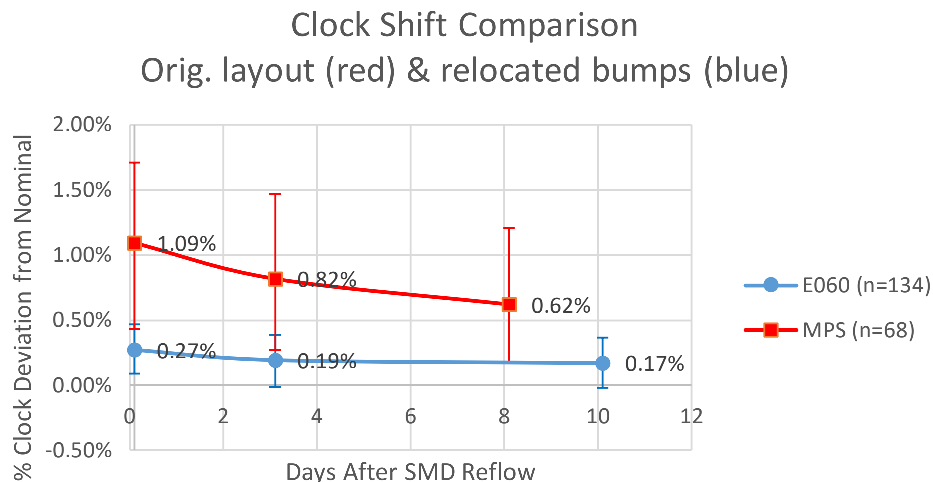
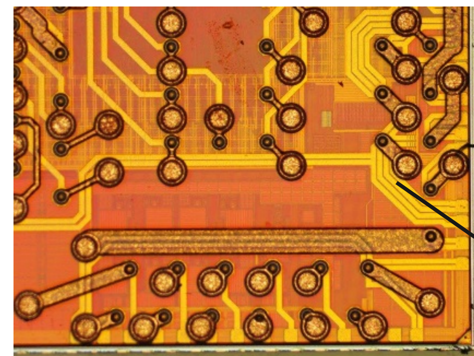
Experiments:

Effect of relocation of bumps



NP5 in Chip on Flex





NP5 relocated bumps (NP5 S-F)

Vbat shifted 180 μm

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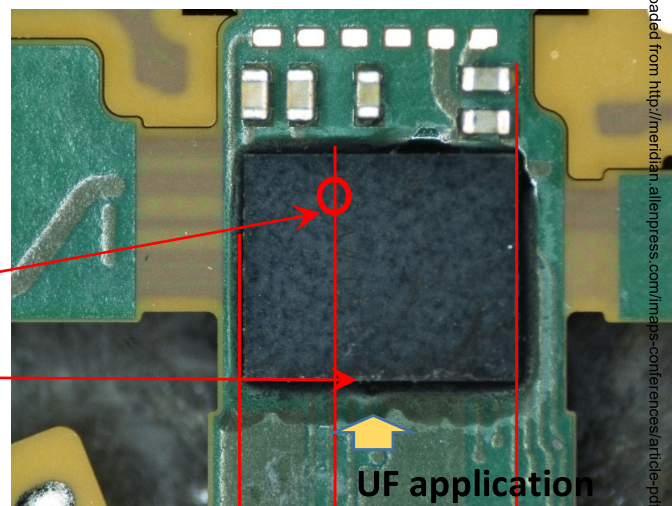
Experiments:

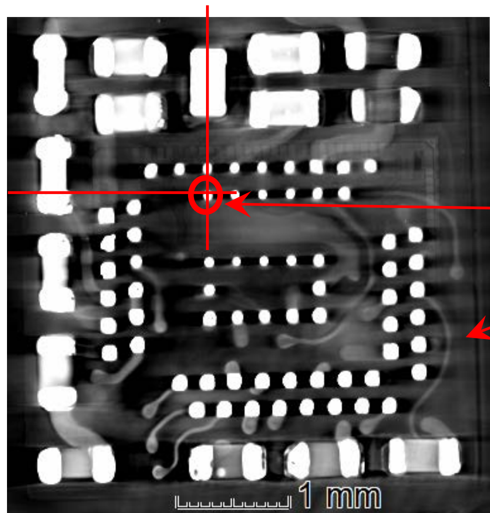
Creating voids in UF

JMBN

V bat

UF application edge

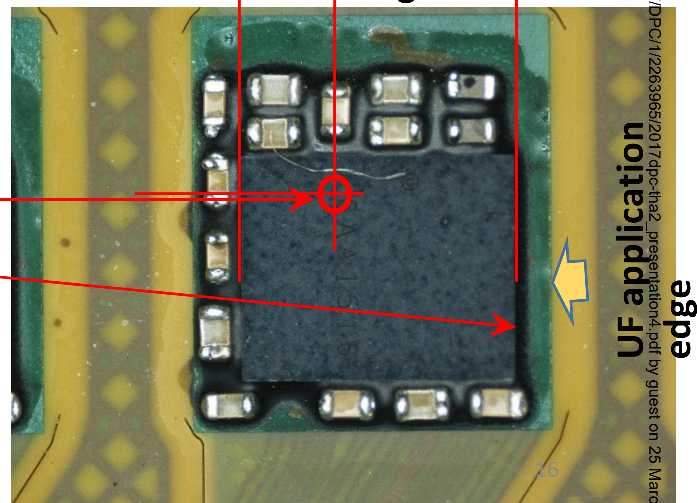




NCS

V bat

UF application edge



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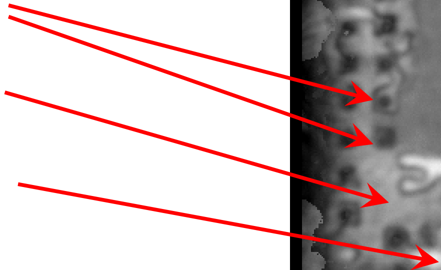
Experiments:

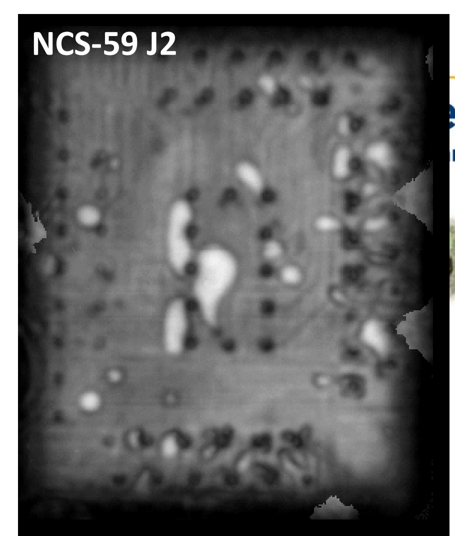
CSAM images

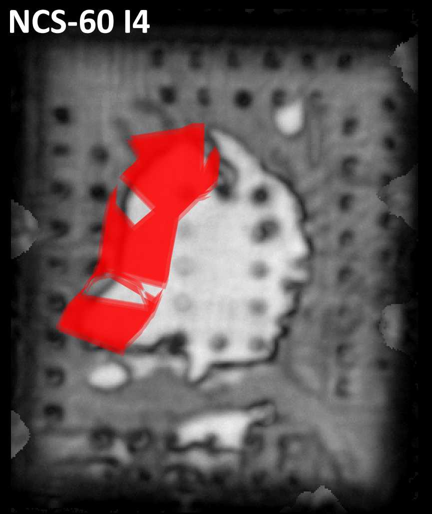
V bat & V bat OD bumps

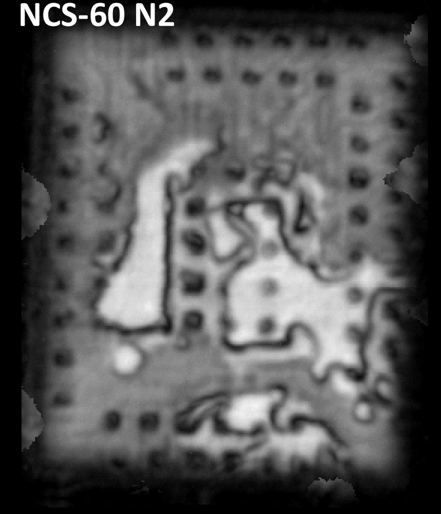
Underfill

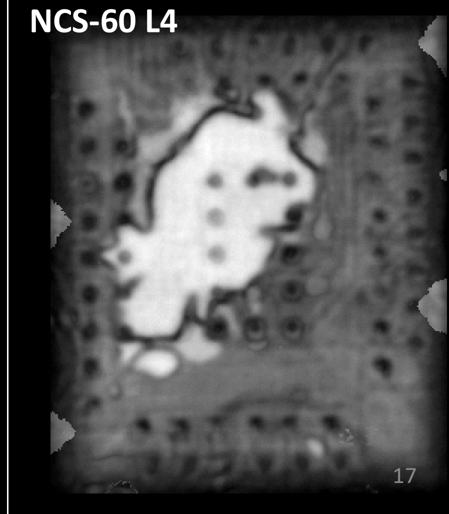
Void/delamination











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Experiments: Voids in UF vs clock shift

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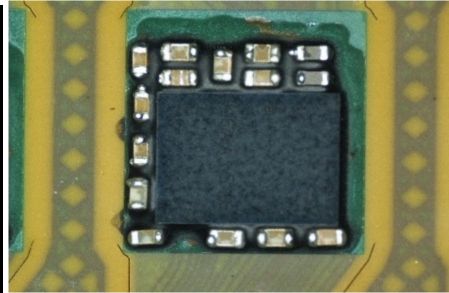
iMAPS

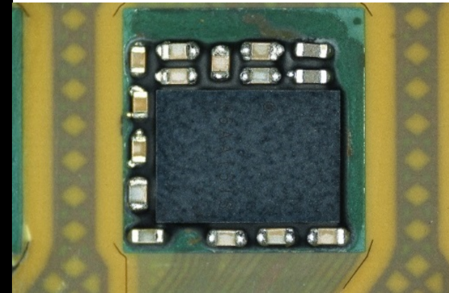
NCS-59 L1



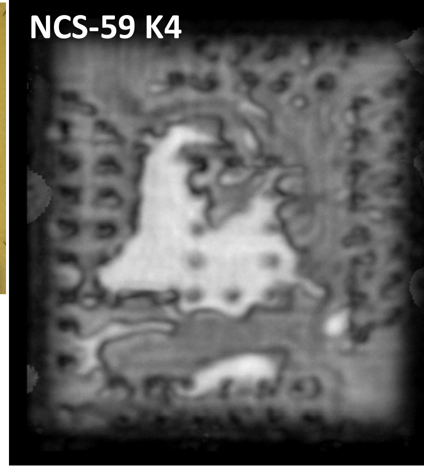
1% clock shift during reflow

Large clock shift
+1.1% shift during reflow

NCS-60 I4



+0.3% shift during reflow



Very little clock shift
-0.05% shift during reflow

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Summary

- The UF material does not improve the stress problem on the die.
  - ➢ Higher fiber content reduces CTE mismatch, however, at the same time makes UF stiffer and builds up stress with less thermal expansion.
- The normal stress is the component the affects the performance of the clock.
  - ➢ UF reduces equivalent stress on the die! But produces a large normal-to-the-die stress.
- Sometimes lower quality UF (with voids) might help with state of stress on the die.
  - ➢ A void around Vbat and Vbat OD bumps significantly reduces the normal and equivalent stresses both at Vbat location and between Vbat and Vbat OD.
- Thinner dies have more flexibility and less susceptible to stress build up. They can be a good area to explore.
- Relocated bump significantly reduces stress at the clock location.
  - ➢ An exclusion zone about the same size as the bumps pitch is recommended.

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Thank you

Questions …?

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