



IMAPS

13th International Conference and Exhibition on
Device Packaging, March 2017

Technology Review of System-in-Package

Presented

by

Yashashree Wase



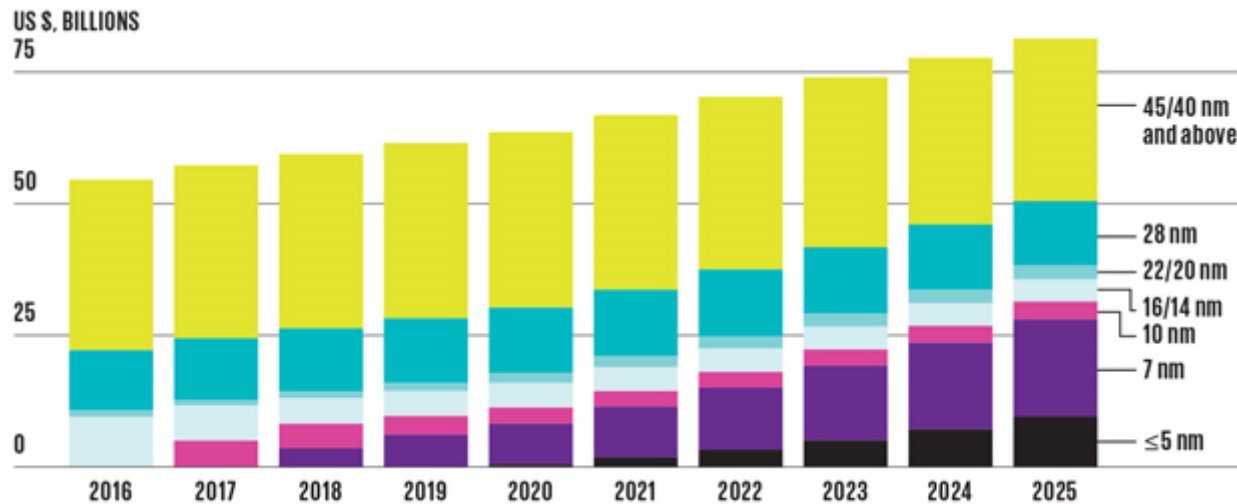
Overview

- Moore's Law – “More Moore” and “More than Moore”
- System-in-Package (SiP) definition
- Comparison of advanced packaging technologies
- Brief history of SiP
- SiP opportunities, challenges and solutions
- Market for SiP and main players
- Inside the devices
- Summary



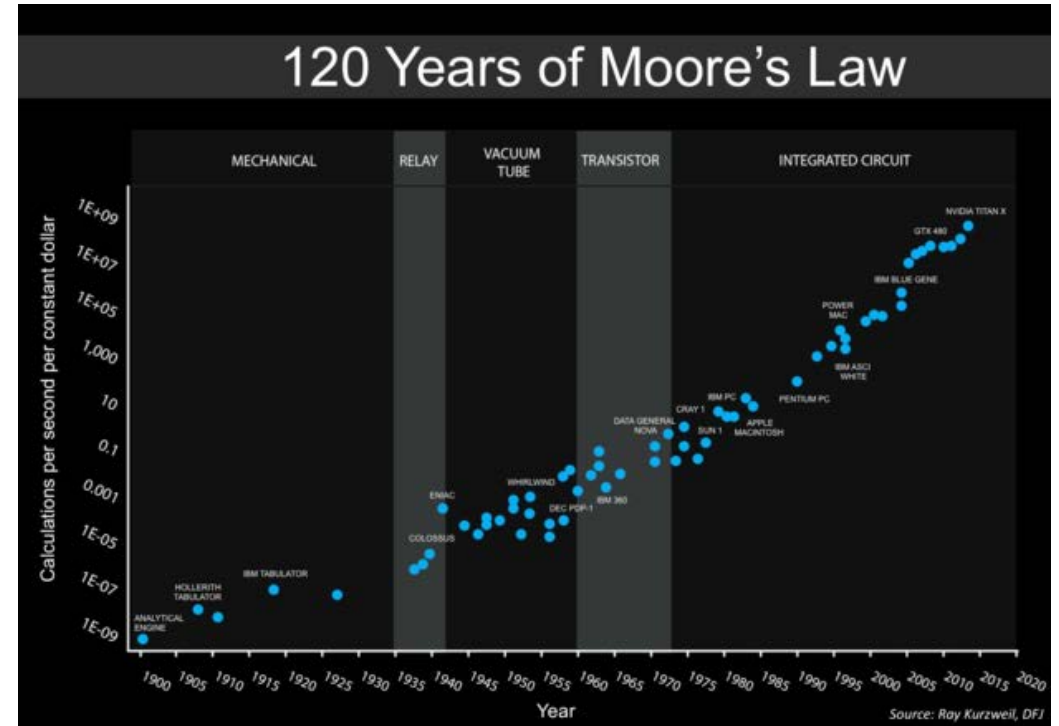
Moore's Law

- Is it dead? – No!
- It has slowed down
- Cost is increasing
- “More Moore” or “More than Moore” ?



Source: IBS

College of Engineering
March 14, 2017



Source: Ray Kurzweil, DFJ

University of Idaho

System-in-Package

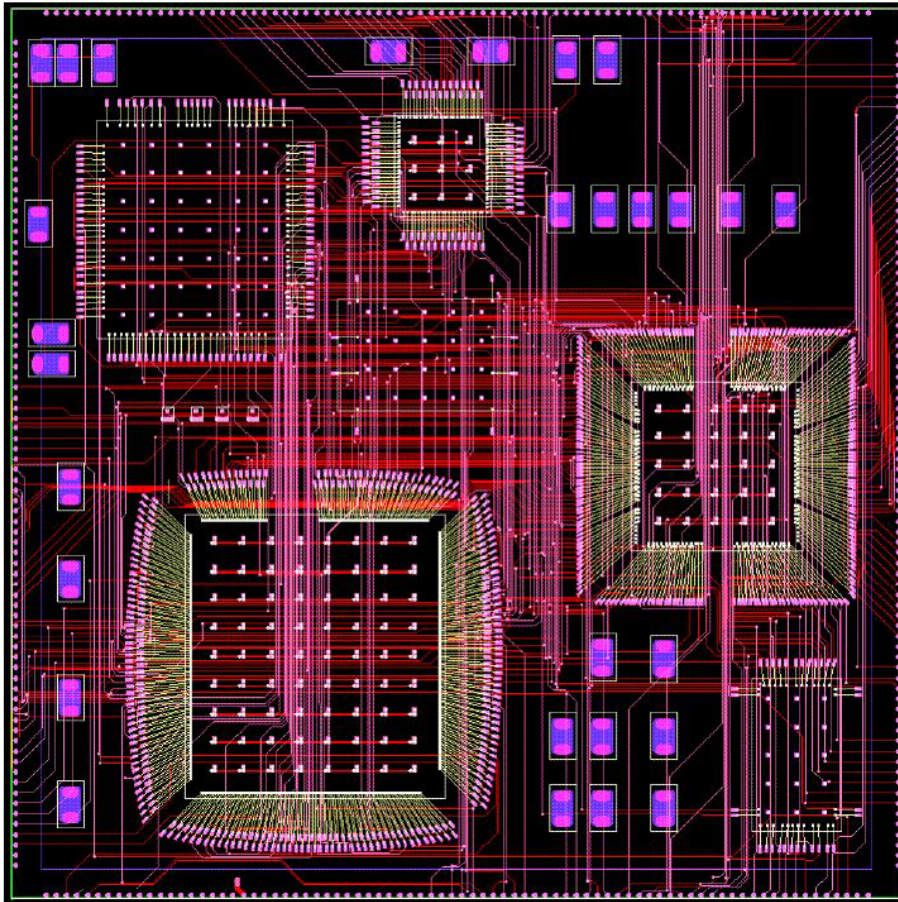


Fig. 1 Complete Pentium Computer in a System-in-Package(SiP) design: CPU, RAM and graphics [1]

- Number of ICs enclosed in a single module
- Integration of ICs, passives, active components, devices like MEMS or optical components
- Components that provide Multiple functions associated with a system
- SiP is used in mobile devices, medical devices ,IoT ,wearables, etc.

Comparison of Packages

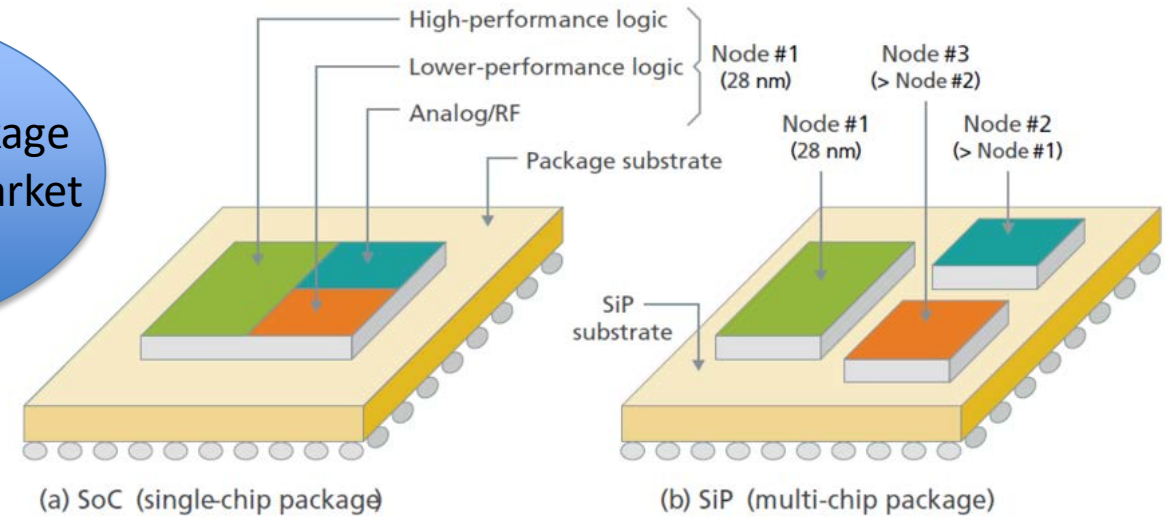
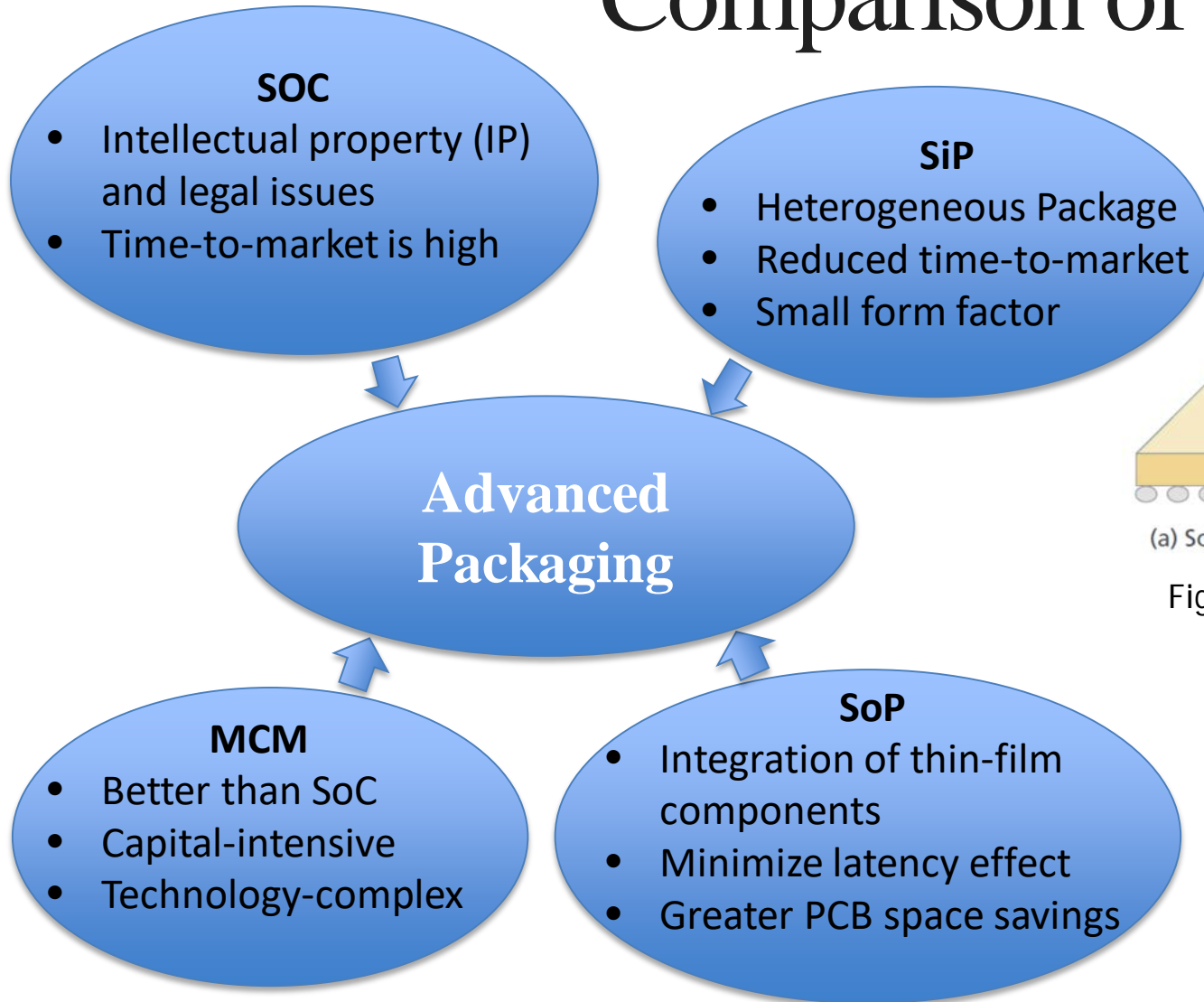


Fig. 2 System-on-chip (SoC) compared to System-in-Package (SiP)

History of SiP

- An insightful reading of “Historical Perspective of System in Package (SiP)” by Dr. Dai
- Profound contributions by Prof. Ernest Kuh
- The term “System-in-Package” was promoted in 2000
- SiP design, analytical methods, and CAD tools
- Solder bumping and FC assembly platforms for SiP
- Wafer level package (WLP) – Advanced packaging



Why SiP?



- More than Moore
- System Integration
- Cost reduction
- Performance Boost
- Functionality Boost

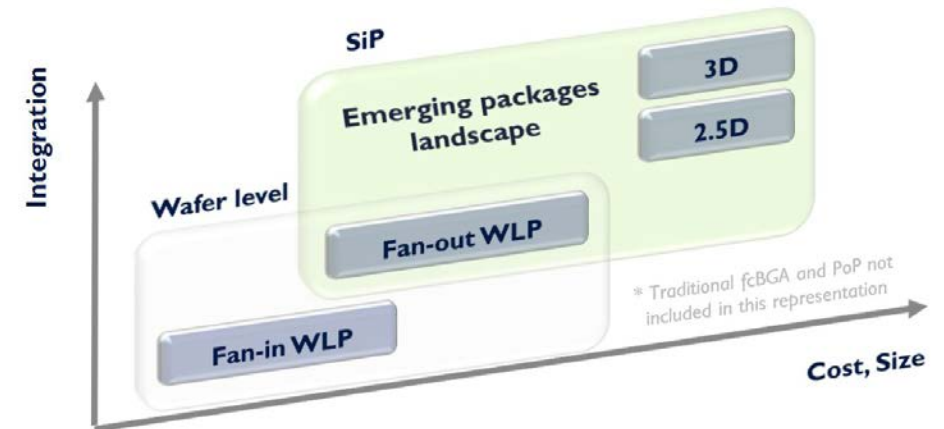


Fig. 3 Growth of advanced packaging [2]

Mobile sector is driving production and growing, however, a new market driver – IoT is on the horizon and is expected to have a significant impact on the packaging industry as a whole – Yole Development

Opportunities

“Smaller, faster, cheaper”

- Reduced time-to-market
- The modules and main system assembly can be developed concurrently
- Compatibility with die design and integration of various die technologies
- Reduced system board space and complexity and layer count by moving to SiP solution



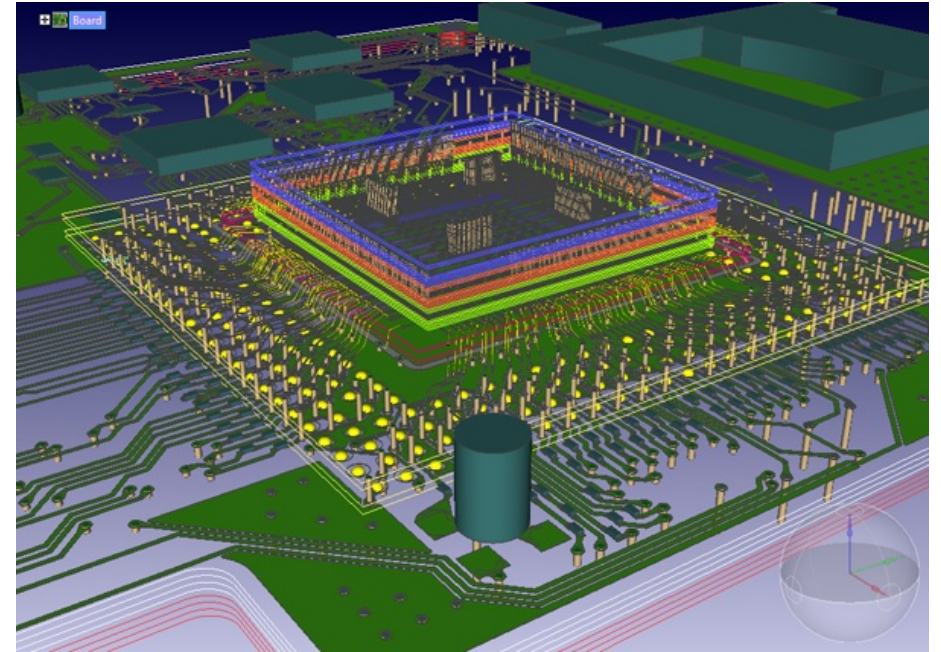
Challenges

- Managing substrate complexity
- Design Challenges
- Known-good-die (KGD) issue
- Interconnect Challenges
- Thermal Management
- Test Challenges



SiP Design Challenges

- Several optimization problems:
 - System I/O requirements
 - Thermal and signal integrity constraints
 - Die placement and orientation
 - Stacking configurations
 - Package substrate and interposer design
 - interconnect design
- Floor-planning
- Design tools



Thermal and Test Challenges

- Need of Thermal Solutions
- ITRS Roadmap
- Thermal Solutions by Amkor
- Test Cost
- Time-to-market



SiP Solutions

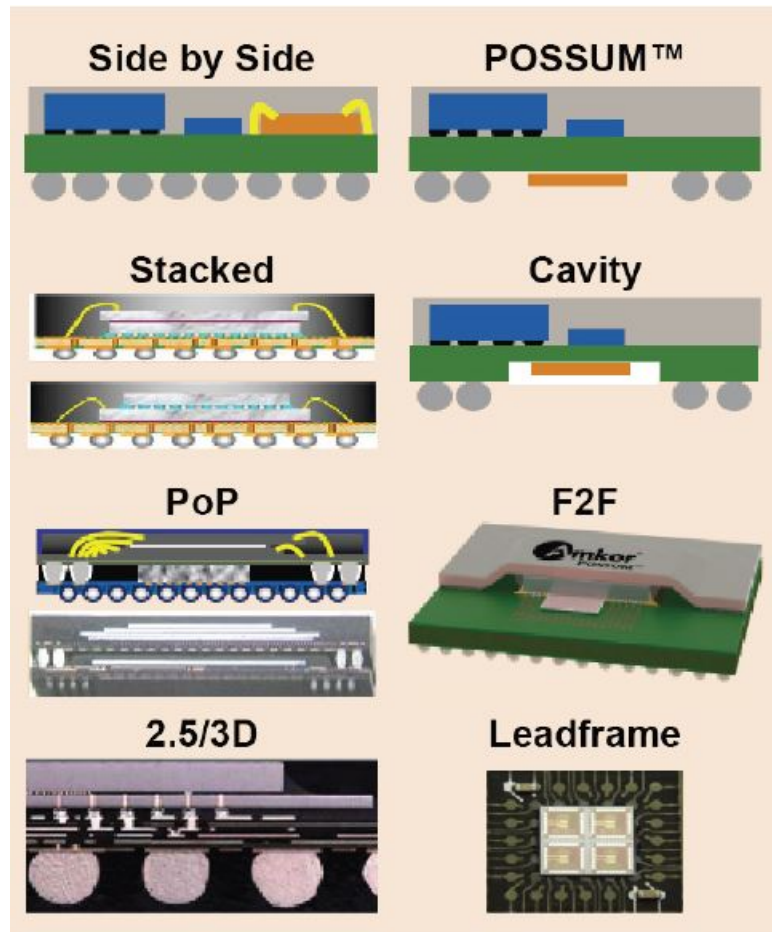


Fig. 4 SiP module design options [3]

- Surface mount discrete passive
- Integrated passive devices (IPD), either glass or silicon (Si) type
- Passives embedded inside or patterned on the substrate
- Die embedded in the package substrate
- Surface acoustic wave (SAW)/bulk acoustic wave (BAW) filters, crystals, oscillators, antennas
- Sputtering conformal shielding and compartmental conformal shielding
- Core and coreless substrate
- Recessed and cavity substrate
- Doubled side mold
- Double-sided assembly (POSSUM™)
- Strip grinding fine pitch ultra-thin package
- Different ICs integrations (Silicon, GaAs, SiGe)
- Pre-packaged ICs
- Connectors
- Mechanical parts

Market for System-in-Package



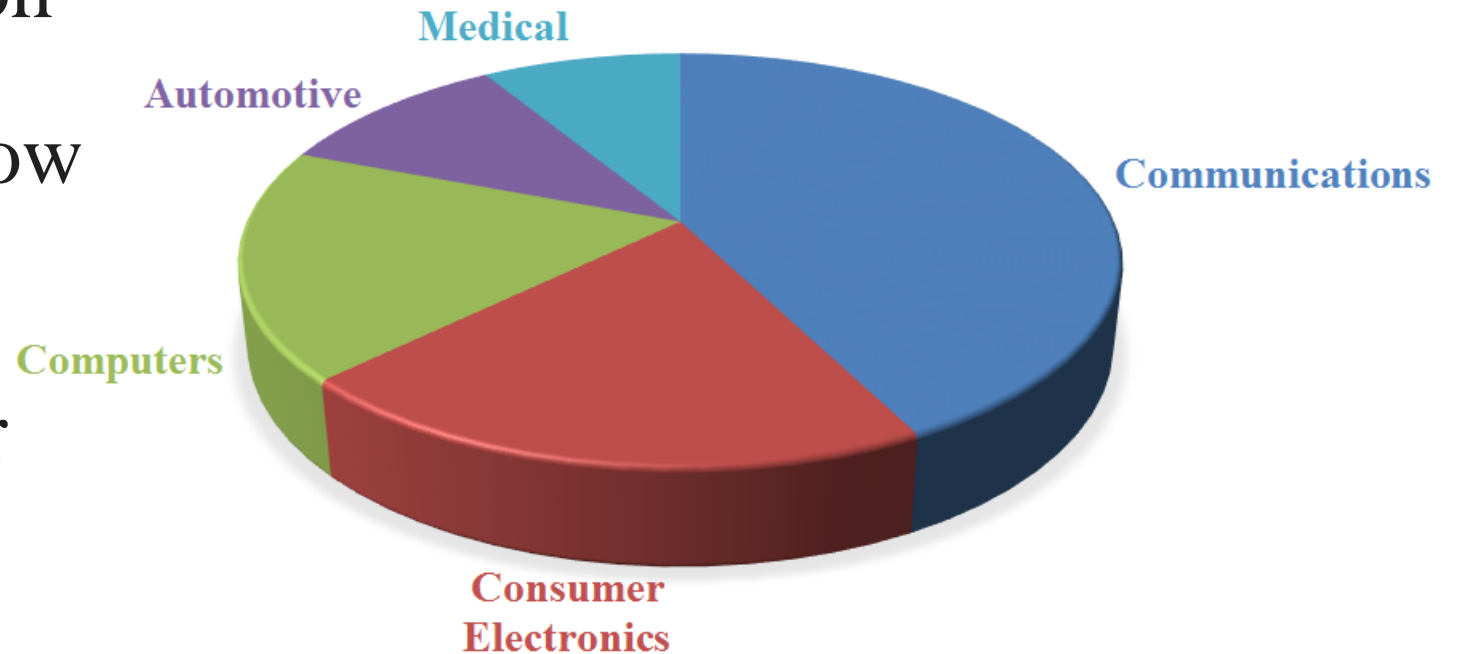
- RF and wireless devices
 - Power amplifiers, front end module, antenna switch, GPS/GNSS modules, cellular handset and cellular infrastructure, Bluetooth® solutions
- Solid-state drives (SSDs)
 - Storage for tablets, net books and computing applications where typical SSDs include controller ASIC, NAND, DDR, logic and power circuits
- Automotive applications
 - Under-hood electronic control unit (ECU), sensory modules and infotainment
- IoT for wearable and machine to machine (M2M) products
 - Connectivity, MEMS, sensors, microcontroller, power management and other mixed-signal devices
- Power modules
 - DC/DC converter, LDO, PMIC, battery management and others



Market Report

- SiP market by application
- Global SiP market to grow at a CAGR > 10 %
- Major application sector

Global SiP market share by application 2015



Market Players

- Amkor Technology
- ASE
- Jiangsu Changjiang Electronics Technology (JCET)
- Siliconware Precision Industries (SPIL)
- United Test and Assembly Center (UTAC)



3D TSV System-in-Package for Aerospace application

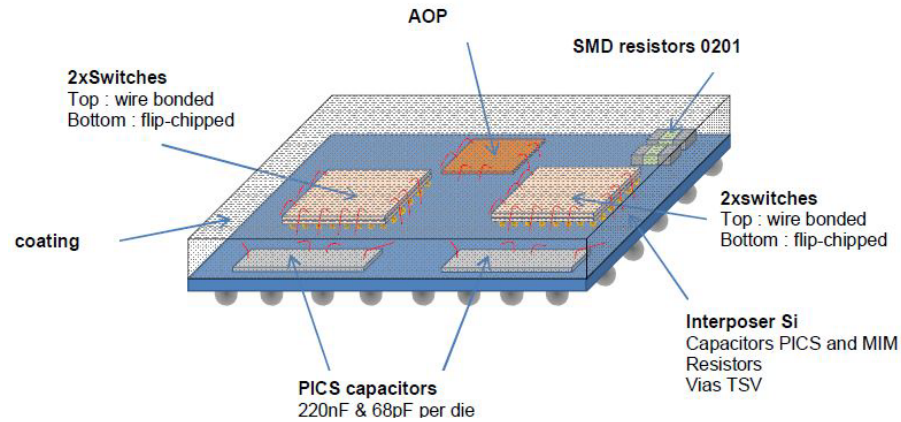


Fig. 5 Schematic view of 3D SiP [4]

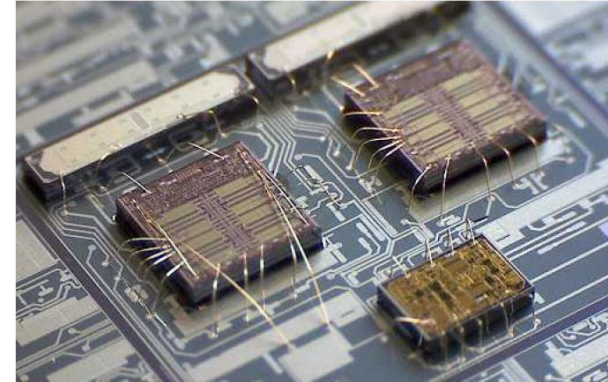


Fig. 6 Overview of an SiP [4]

Intel's 3D System-in-Package Technology

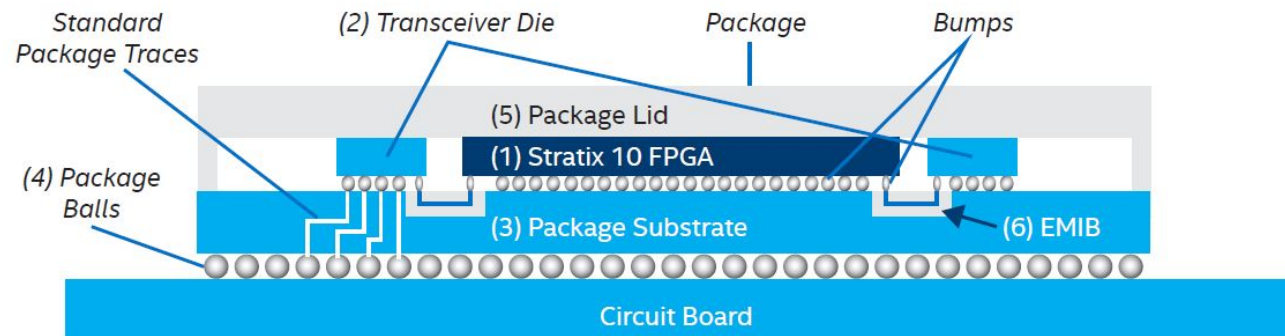


Fig. 7 Heterogeneous Integration using EMIB Technology [5]

Miniaturization of System-in-Package for wearables

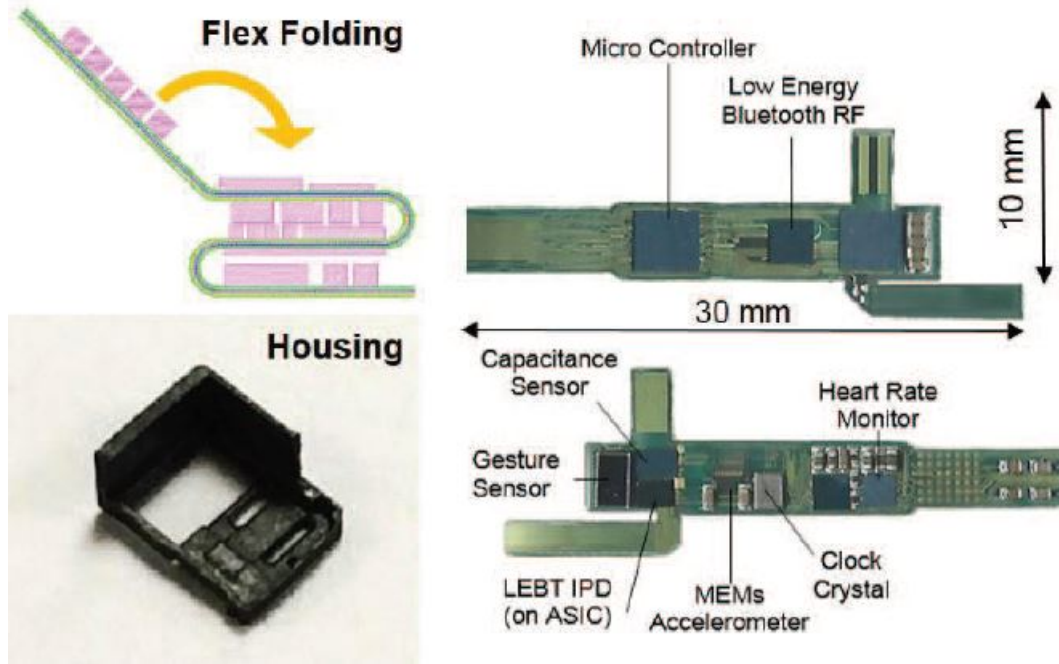


Fig. 8 Health monitoring module using Cu pillar solder flip chip with size reduction from 30 x 10mm to 6 x 4 x 2.6mm after folding the flex to the septum [6]

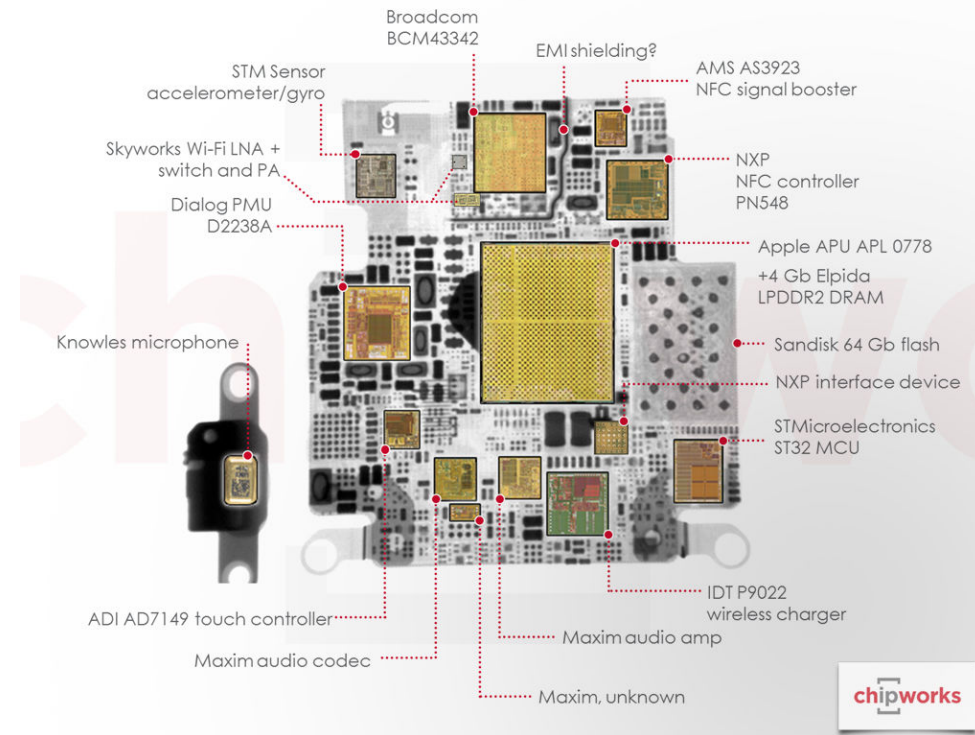


Fig. 9 Apple watch S1 System-in-Package

Summary

- System-in-Package remains a viable interim solution to the inevitability of SoC manufacturing
- Shorter time-to-market and reduced production cost are the key considerations of SiP
- The main advanced packaging technology drivers and innovation: Increased integration, small form factor and low cost
- Reviewed SiP solutions, market, and application



References

- [1] A. Fontanelli, "System-in-Package Technology: Opportunities and Challenges," *9th International Symposium on Quality Electronic Design (isqed 2008)*, San Jose, CA, 2008, pp. 589-593.
- [2] A. Ivankovic, T. Buisson, S. Kumar, A. Pizzagalli and R. Beica, "Status of the Advanced packaging Industry-From technologies to market: 2015" Yole Developpement, *IMAPS Journal of Microelectronics and Electronic Packaging*, November 2015.
- [3] Technology Solutions by Amkor Technologies, <http://www.amkor.com/go/SiP>
- [4] J. C. Riou, E. Bailly, C. Bunel, L. Lenoir and M. Pommier, "3D TSV system in package (SiP) for aerospace applications," *2013 European Microelectronics Packaging Conference (EMPC)*, Grenoble, 2013, pp. 1-7.
- [5] Intel White paper: Enabling next-generation platforms using Intel's 3D System-in-Package technology, Manish Deo, Senior Product Marketing Manager and Intel Programmable Solutions group
- [6] K. Pun, A. Singh and M. N. Islam, "Miniaturization of system in package for wearable devices using copper pillar solder flip chip interconnects," *2016 China Semiconductor Technology International Conference (CSTIC)*, Shanghai, 2016, pp. 1-8.
- [7] Miettinen J., Mantysalo M., Kaija K. & Ristolainen E. O., "System design issues for 3D system-in-package (SiP)," *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 2004, pp. 610-615 Vol.1
- [8] Xi J., Lin K., Xiao F. & Sun X., "Studies on reliability of a 3D system-in-package device," *Electronic Packaging Technology (ICEPT), 2013 14th International Conference on*, Dalian, 2013, pp. 1033-1036
- [9] James D., "3D ICs in the real world," *25th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC 2014)*, Saratoga Springs, NY, 2014, pp. 113-119



Thank
You!

