Silicon Wafer Integrated Fan-out Technology

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IMAPS DPC Mar 2017

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Outline

- SWIFT™ (HDFO) Technology Introduction
- Product Drivers and Market Forecast
- SWIFT™ Value Proposition
- Process Flow and Structure
- Key Enablers and Challenges
- Electrical, Thermal and Warpage
- Conclusions

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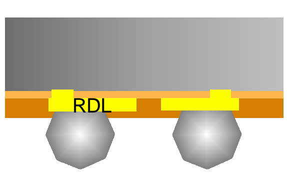
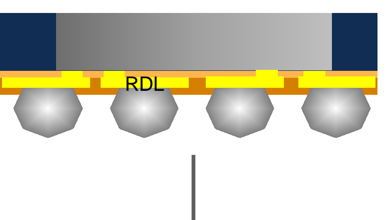
WLP & Flip Chip Migration to Fan-Out Package

WLP (Fan-in)

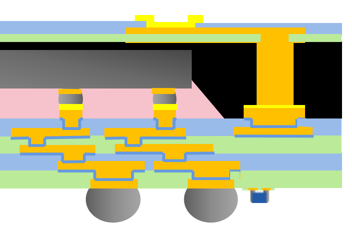


- More real estate for I/O required for increased chip functionality
- Enable 3D, SiP and MCM through mold
- Known good die process
- Si side protection

Fan-Out WLP

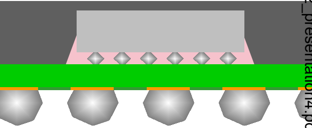


High Density Fan-Out WLP



- Thinner profile (no substrate and wafer level thinning)
- Improved electrical/ thermal performance
- Finer routing available
- As a low cost alternative to 2.5D TSV MCM

Flip Chip Package



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Target Segments – SWIFT™ Packaging Technology

Mid-High End | Low-Mid End

Mobility

- Phones
- Tablets
- Thin clients

IoT

- Consumer
- Industrial

Automotive

- ADAS
- Infotainment

HPC

- Networking
- AI
- GPU
- Server

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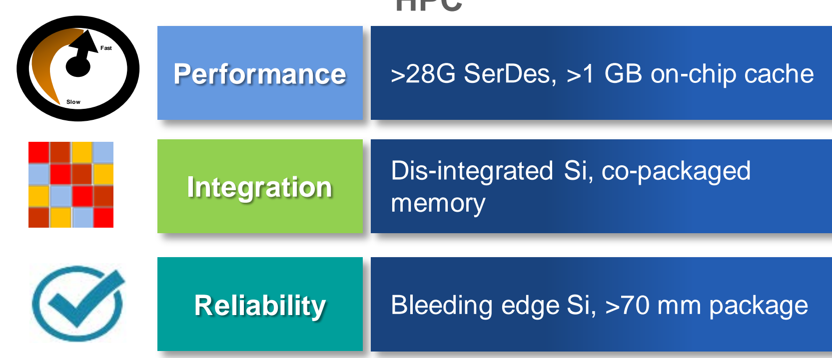
Mobility & HPC Market: Key Drivers/Inflections

Mobility

Size	Miniaturization, Lower weight
Integration	AP, BB, PMIC, Wi-Fi, BT, GPS etc.
Cost	Lower cost per I/O

- Premium smartphones driving AP Z height to 0.6 mm
- Package I/O count and pitch scaling driven by premium and high end smartphone market
- Integrated AP+BB solutions will likely migrate to disaggregated solutions at 7 nm node for AP
- Wafer level SiP solutions for integration of AP with memory and/or PMIC



- AI driving package size, bandwidth, component count per package
- Data center and 5G infrastructure driving the need for overall package size migration to 70 mm and higher
- Die-disintegration (especially SerDes from ASIC) seen as key enabler for faster time to market
- Off-chip data rate migration to 56G and 112G SerDes drive the need for TSV less solutions

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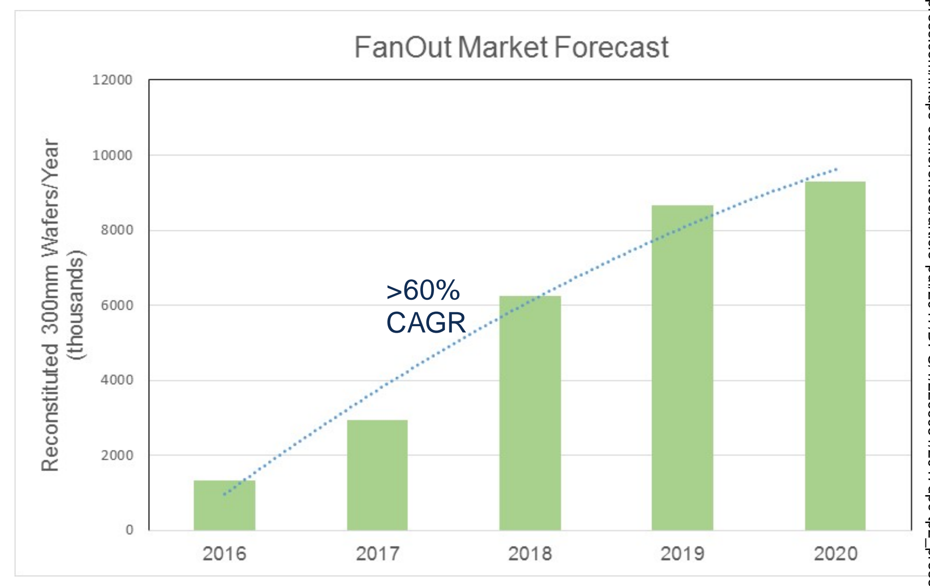
Fan-Out Market Projections

- Device – RF transceiver and switch, PMIC, CODEC, automotive radar, connectivity (IoT) modules, Apple's application processors made by TSMC and application processors from other companies in the future
- Future memory for top PoP
- HDFO (SWIFT, others)- >70% of Fan-out market



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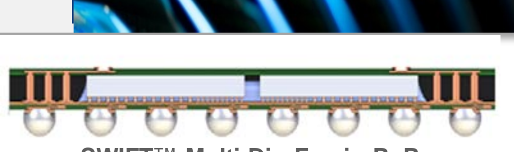
Features and Value Proposition SWIFT™

Process	▪ RDL first ▪ Chip attach last
Cycle time & yield	▪ Shorter cycle time ▪ RDL wafer pre-build ▪ Known good RDL wafer
Flexibility & scalability	▪ Package variants – 3D, SiP etc. ▪ Multi-die, passives ▪ Flexible thickness
Performance	▪ Thermal ▪ Electrical ▪ Reliable



SWIFT™ Multi-Die SiP Overmold

SWIFT™ Multi-Die Fan-in PoP

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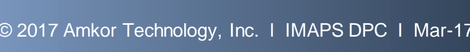

Advanced Fan Out Comparison

Key Attributes	Fan Out SWIFT™	fcCSP Exp Die PoP	fcCSP Fan-in PoP	SWIFT™ Benefits
Package Thickness	0.40 mm	0.45 mm	0.630mm	➢ 11% reduction ➢ 37% reduction
Layer Count	3 or 4	3	5	
Construction	3 layers on bottom + 1 layer on top (for fan in)	3 layer substrate on bottom	3 layer substrate on bottom + 2 layer substrate on top	➢ Same as exposed die ➢ Fewer layers
Electrical	Reduced signal width allows flexibility in routing/ impedance control	Predetermined location at edge of package	Fixed signal widths and difficulty in impedance control	➢ Flexibility, reduced trace length, reduced DC resistance & AC loss
Interposer Interconnect to Package Edge	50 µm	200 µm	200 µm	➢ 75% Reduction

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High Density Interconnection Method

SWIFT™
Cu RDL

Die
μ-bump
RDL
BGA

Inner Layer : No of Possible Signal Routes per MM of Die Length

SLIM™
Cu Damascene

Die
μ-bump
BEOL
RDL
BGA

Routing capability comparison

SLIM™ > 3x SWIFT™ > 3x flip chip

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Wafer Level Packages in High-End Smart Phones

- WLCSP % as function of total BOM increasing in all smartphone categories
- PMICs and audio codec driving pitch reduction

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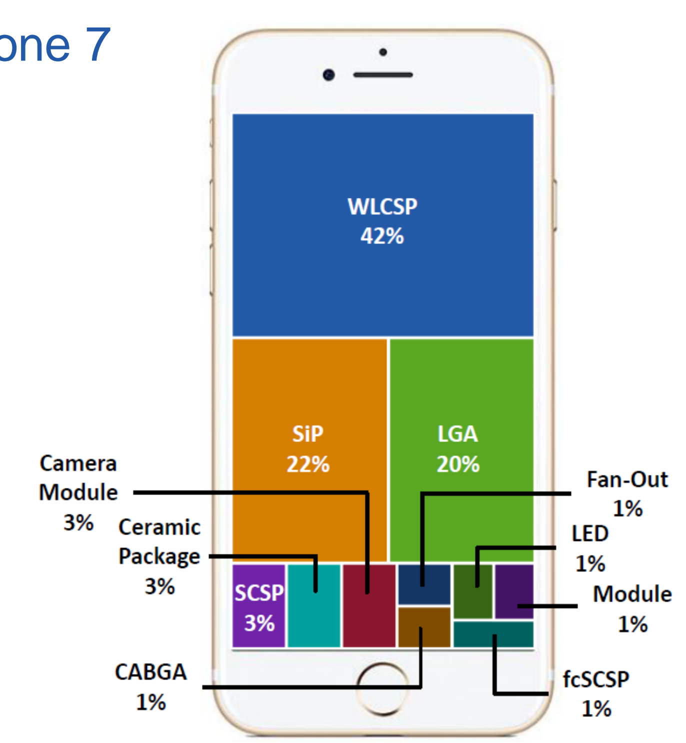
Packages Used in High End Smart Phones

Apple iPhone 7



- Miniaturization
- Integration
- Performance
- Wafer level
- Multi-die and passives

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High Density Fan-Out Evolution

I/O: 5000, 3000, 2000, 1500, 1000, 500, 300, 100

Body Size: 2 x 2, 3 x 3, 4 x 4, 5 x 5, 6 x 6 mm, 8 x 8 mm, 10 x 10 mm, 12 x 12 mm, 15 x 15 mm

WLCSP

Conventional FO-WLP

- Limited scalability & platform extension to MCM, SiP and 3D structure at finer feature size

(L/S: > 8 µm/8 µm)

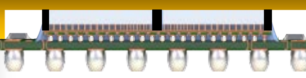
High Density FO-WLP

- Better scalability, 3D compatible process and extended platform to SiP and MCM at finer feature
- Chip last and chip first

(L/S: >= 2 µm/2 µm)

High Density FO for 2.5D

- ≤2 µm L/S for multi-die interconnect
- Fan-out module attach to substrate as low cost alternative to TSI 2.5D



(L/S: <= 2 µm/2 µm)

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SWIFT™ Package Assembly Flow

POP Pillars
200 µm Pitch

RDL for Memory Interface

40 µm Pitch

< 0.40 mm
Total Height

SWIFT™

Carrier Remove

Top Side Routing
For Memory Interface

Carrier

Carrier

RDL & Copper Pillar
Bump (3D Only)

Chip Attach & UF

Wafer Mold

POP Pillars
200 µm Pitch

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Key Process Technologies & Challenges

3D PoP

SiP

Package Stacking
- Solder joint
- Gap filling
- PoP reliability
- Mold side RDL

Mold & Mold Grind
- Warpage
- TTV
- Surface condition

Through Mold Interface
- ≤0.3 mm pitch & 0.2 mm tall
- Throughput
- Uniformity

Multi Layer RDL
- High metal density
- Fine L/S and uniformity
- Via contact
- RDL-polymer integrity

Chip Attach & UF
- Fine pitch μ-bump joint
- Thin die attach
- Underfill flow
- Reliability

Land Side Cap
- Low profile component

MUF
- Gap filling
- Warpage
- Reliability

EMI Shield
- Adhesion
- Thickness uniformity
- Side coverage
- Shielding performance

Package Singulation
- Exposed RDL
- Mold-RDL-polymer adhesion

Passive Integration
- Ability to assemble various finish type
- Adhesion to MUF

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DDR4: Signal Integrity Comparison

Key Attributes	Fan Out SWIFT™	fcCSP Exposed Die PoP	SWIFT™ Benefits
Eye Diagram DDR4 @ 6 Gbps			
Eye Amplitude	548 mV	451 mV	3.0x Improvement
Eye Height	481 mV	339 mV	1.4x Improvement
Eye Width	164 ps	158 ps	4.0x Improvement
Pk-Pk Jitter	3.7 ps	9.8 ps	2.2x Improvement
Rise/Fall Time	64 ps	75 ps	1.2x Improvement

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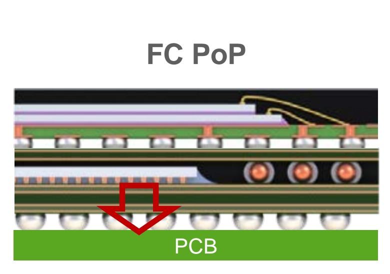
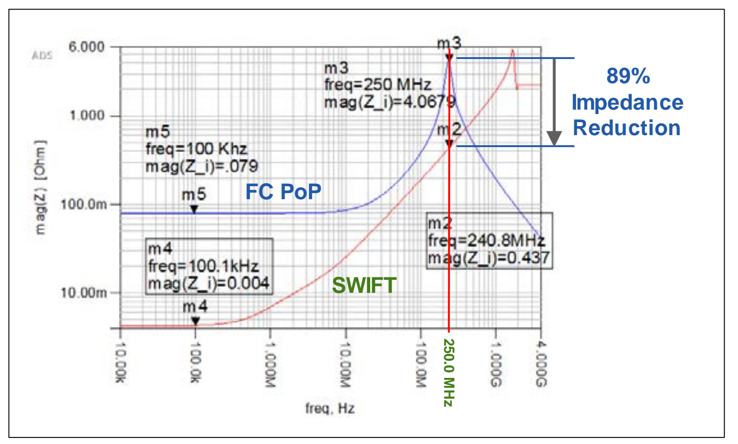
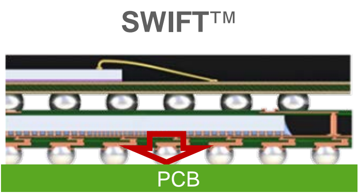
Power Integrity: Lower PDN Impedance







- PDN Impedance: Improved by 11% vs FC PoP (at 250 MHz)
  - SWIFT™: Substrate eliminated – resulting in reduced pad-BGA wiring length
  - Low PDN Impedance → High power integrity

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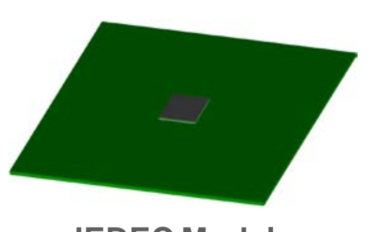
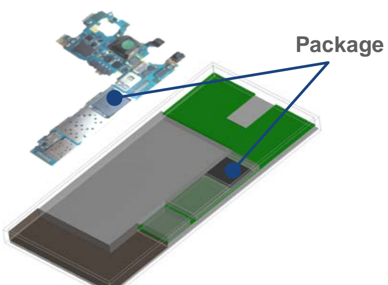
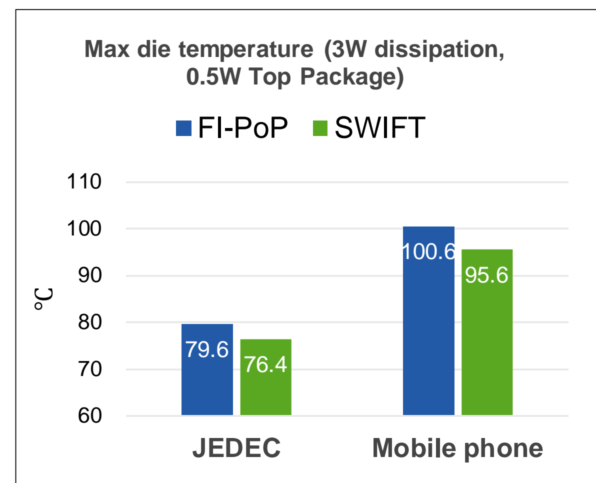
SWIFT™ vs FC PoP Thermal Simulation

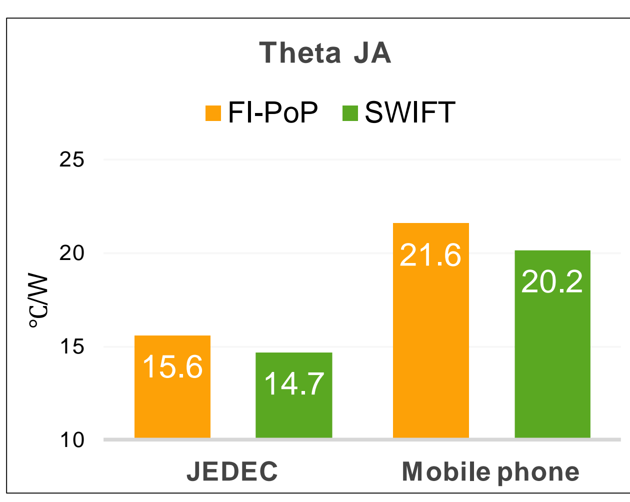
Steady State Analysis


JEDEC Model



Mobile Phone Model





Max Temp (3W) °C	FC PoP	SWIFT	Delta	Delta %
JEDEC	79.6	76.4	-3.2	-4%
Mobile Phone	100.6	95.6	-5.0	-5%

Theta JA °C/W	FC PoP	SWIFT	Delta	Delta %
JEDEC	15.6	14.7	-0.9	-6%
Mobile Phone	21.6	20.2	-1.4	-6%

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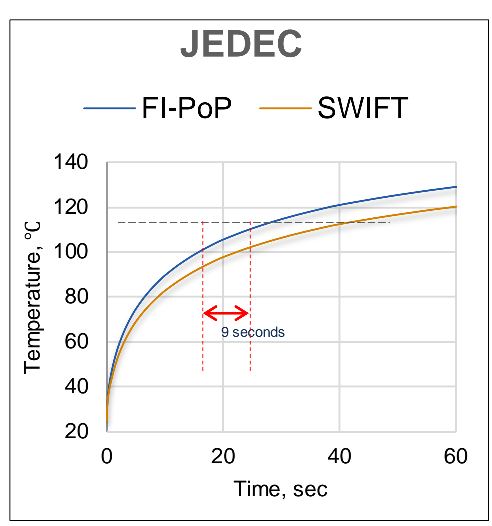
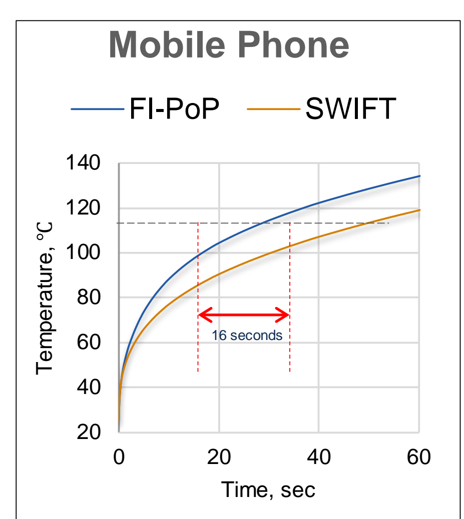
SWIFT™ vs FC PoP Thermal Simulation

Transient Analysis





Time for die temp to reach 105°C (9W power dissipation)

	JEDEC	Mobile Phone
fcPoP	19.5 sec	20.5 sec
SWIFT	28.2 sec	36.8 sec
Gain	**8.7 sec**	**16.3 sec**
	45%	**80%**

- Time to reach the allowable max die temperature when a 9 watt duty cycle is applied
- The assumed allowable max die temperature is 105°C
- SWIFT extends the time to reach 105°C by approximately 9 and 16 seconds as compared to conventional substrate FC PoP

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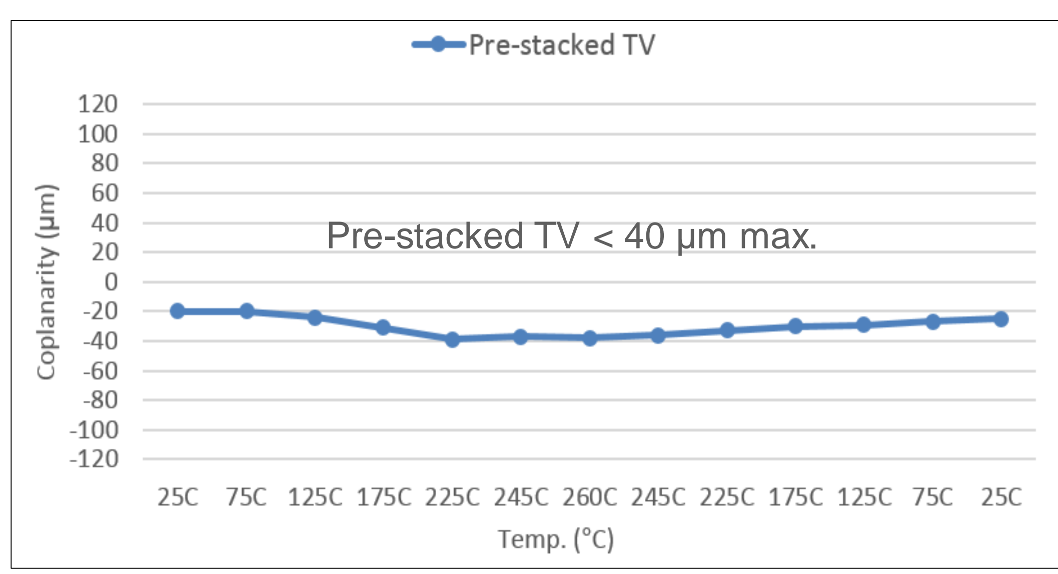
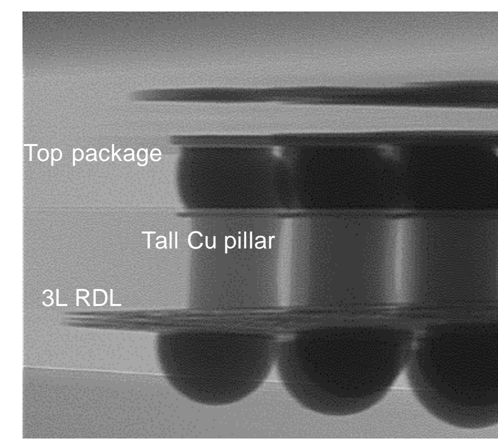
HD-FO Unit Warpage

Unit warpage (shadow moiré)
15 x 15 mm Body, (2x) 5 x 10 mm die





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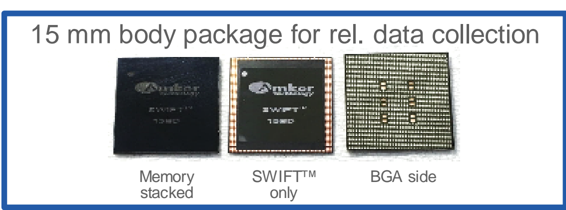
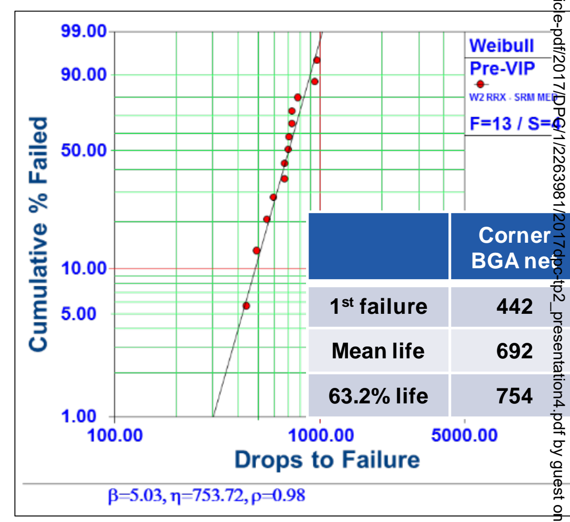
SWIFT™ Package Reliability

- Package level
  - Passed MSL L3/260°C
  - Passed MSL3 + uHAST 96 hrs
  - Passed MSL3 + TCB 1000 cycles
- BLR (w/board UF)
  - Passed TC 2000 cycles
    - JEDEC condition G in JESD22-A104
  - Passed 2000 drops
    - JEDEC condition B in JESD22-B111
- BLR (wo/board UF)
  - Passed TC 2000 cycles
    - JEDEC condition G in JESD22-A104
  - Completed 1000 drops (See chart to right)
    - JEDEC condition B in JESD22-B111



w/o Board UF
Drop Test Weibull Analysis



	Corner BGA net
1st failure	442
Mean life	692
63.2% life	754

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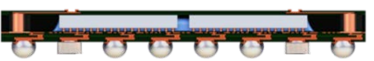
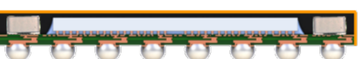
SWIFT™ (Chip Last) Package Roadmap

Available	2017	2018

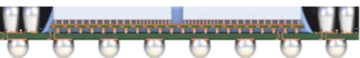
Single Die SWIFT™ (2D)



Multi-Die SWIFT™
- 3D tall Cu interconnect
- Land side cap
- Fan-in RDL



SiP SWIFT™
- Active and passive components
- Sputtered EMI shield



SWIFT™ on Substrate
- Split logic
- 3D Interconnect
- Land-side cap

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Conclusions

- SWIFT™ – bridges the gap between TSV (high end) and traditional substrate and wafer fan-out packaging (low end)
- SWIFT is uniquely suited:
  - To improve product performance
  - To handle multiple die from different functional blocks (analog, mixed-signal, digital)
  - To enable very small form factors
- Enables the creation of advanced 3D structures that address the need for increased IC integration in emerging mobile and networking applications
- Improved signal integrity and power distribution networking due to fine line/space and thin film dielectric capabilities

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