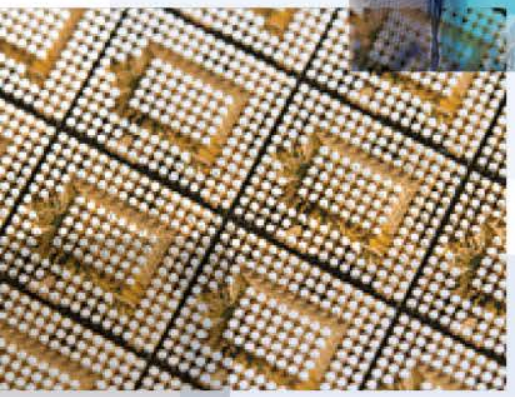
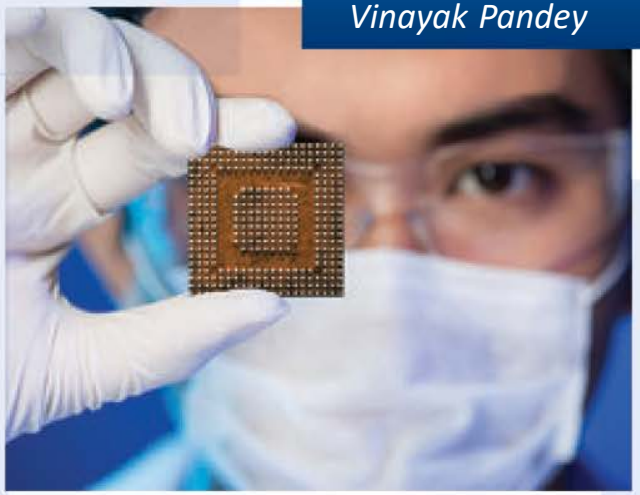
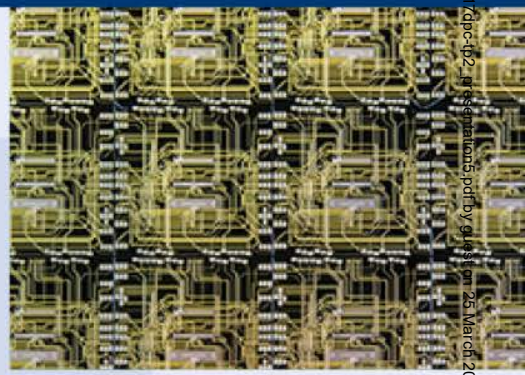


Advanced 3D eWLB-SiP (embedded Wafer Level Ball Grid Array – System in Package) Technology

Chen Kang and Seung Wook Yoon
Vinayak Pandey

07 March 2017





Innovative Integration Solutions

Outline

1. SiP and the need for integration
2. eWLB FOWLP : Value proposition of SiP
3. 3D eWLB-SiP Study
4. Cost considerations with panel scalability
5. Summary

Drivers for Integration

- **Heterogeneous integration for optimized system solution**
- **Differentiation & specialization**

Miniaturization

Higher performance

Heterogeneous integration

Si partitioning in advanced nodes

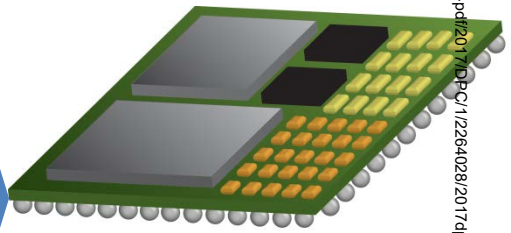
Customization, platform re-usability & re-configurability

Modularization – Final assembly simplification

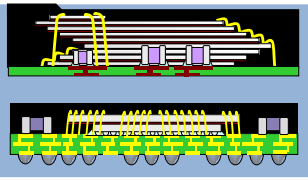
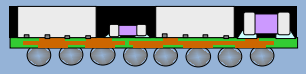
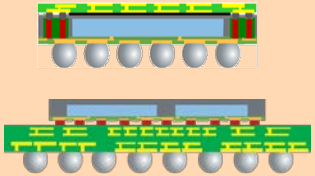
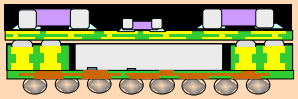
Design flexibility & Time-to-market

Lower system level cost

SiP / Module



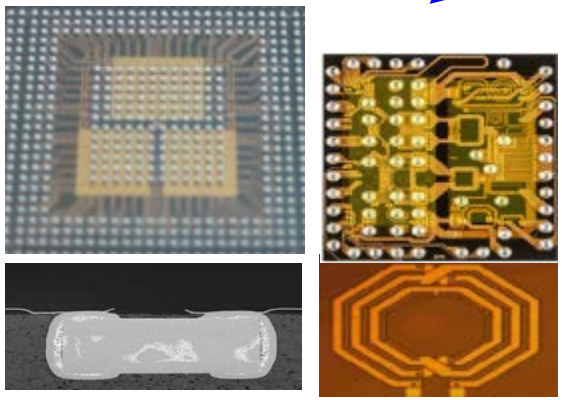
SiP Modules and Applications

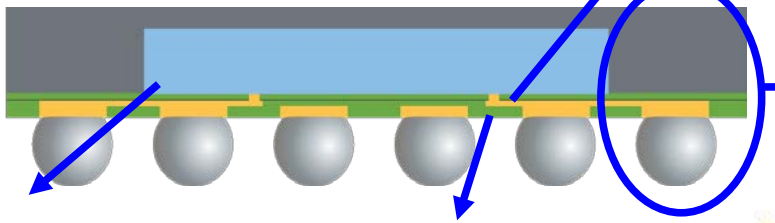
SiP Package Types		Features	Target Applications
Stacked Die Module		• LGA/BGA • Thin Stacked Die • Passives	• SSD (Removable & Embedded) • BB/AP Processors (WE)
Substrate Module		• LGA/BGA • Bare Die or Over-Mold • IPDs, Passives • Cu OSP + LF Solder	• Filters • PA Modules • Connectivity Combo Modules
fcFBGA SiP		• Passives, WLCSP, Packaged Components • Coreless or cored substrates	• Controller Modules • PA/PAD Modules • RF FEM
Hybrid (FC+WB) SiP			
FOWLP (eWLB) SiP		• Multi-die embedded • 10/10 → 5/5, 2/2um L/S • Passives Integration • 5x5~ 16x16mm Body Size	• Connectivity • PMIC, CODEC • PA Modules • AP processor+ Memory • RF MEMS
eWLB-PoP & 2.5D SiP		• eWLB-PoP (eBAR) • 0.4 → 0.2mm stacking pitch • Ultra thin package (<0.3mm)	• High-end AP Processors • CPU/GPU • High bandwidth

Integrated Packaging Platform

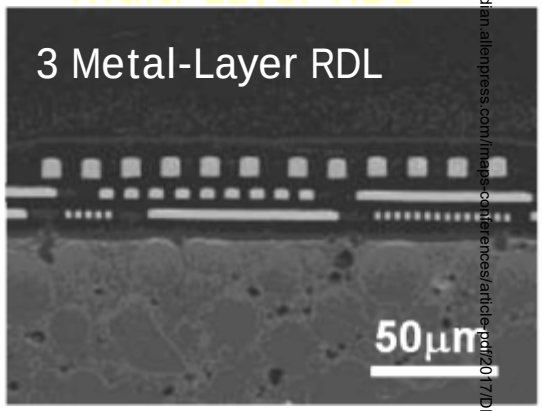
- **Thinner and smaller form factor**
- Enhanced performance
- **Integration – multi-Die, 3D PoP & SiP**
- Cost effective solution with scalability
- Manufacturing proven solutions (HVM from 2009)

Integration with multi-die, embedded discrete and RDL inductor



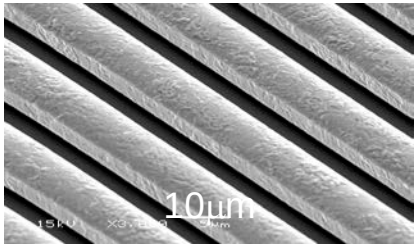


Multi-Layer RDL



Ultra thin package
~0.3mm with solder ball

Fine Cu Plated RDL
5/5um → *2/2um* LW/LS



eWLB Value Proposition for SiP Modules

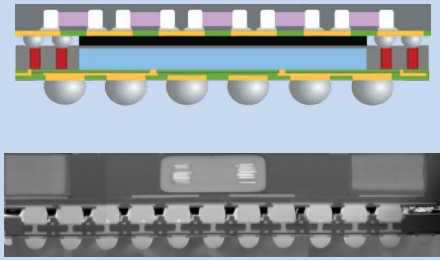
1.Size Reduction
- X/Y & Z

2.Enhanced Reliability
- Fewer interfaces

3.Integration Capability
- Heterogeneous die, passives, etc

4.Performance Improvement
- Better RLC and thermal

3D eWLB



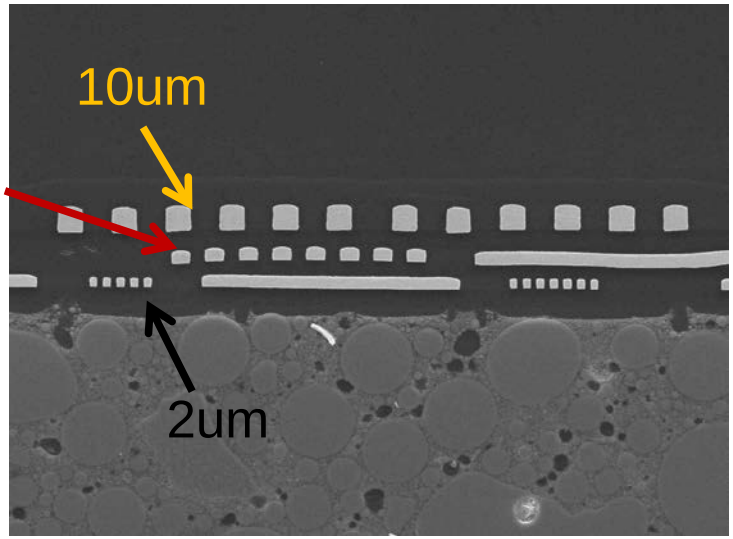
Innovative Integration Platform

Significant X/Y Size Reduction

Ultrafine line/space ground rules down to 2/2um in a 3 RDL format enables improved routability and tighter component placement

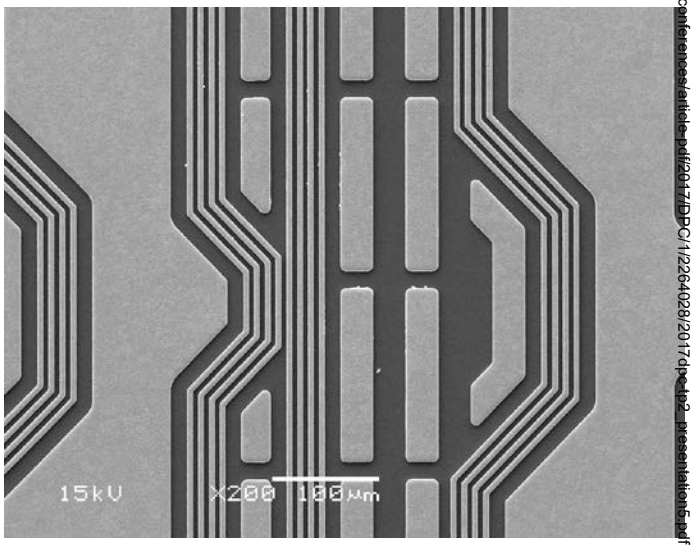
X-Y Size Reduction

SEM micrographs of 3-layer RDL eWLB



3rd Layer – 10/10um LW/LS
2nd Layer – 5/5um LW/LS
1st Layer – 2/2um LW/LS

SEM micrograph of 2/2um LW/LS RDL

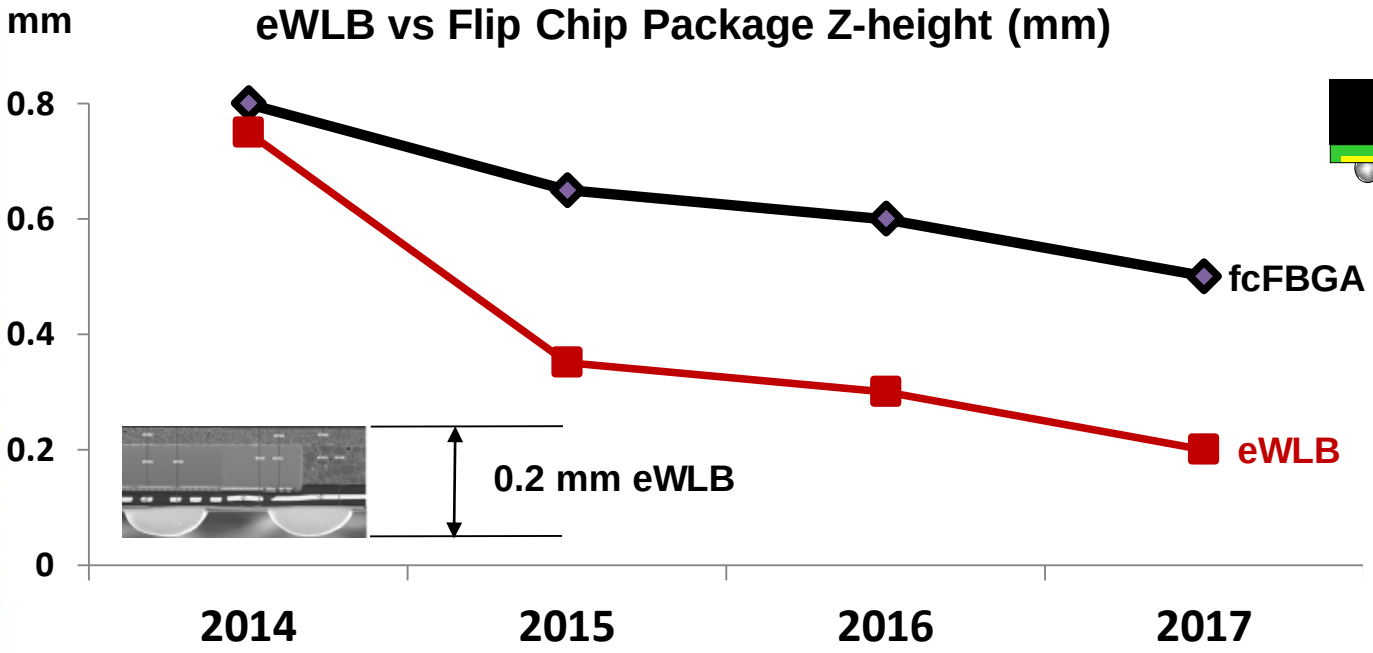


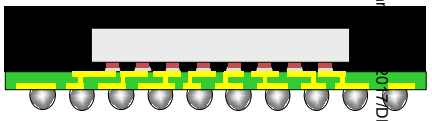
Source: Joint paper with Qualcomm published on Oct 29 2015, iMAPS2015 Orlando, US

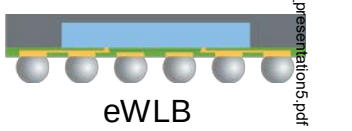
Z-height Size Reduction

eWLB eliminates the use of a substrate reducing the overall package thickness by up to 50% down to 0.2 mm in 2017 (HVM)

Z Size Reduction

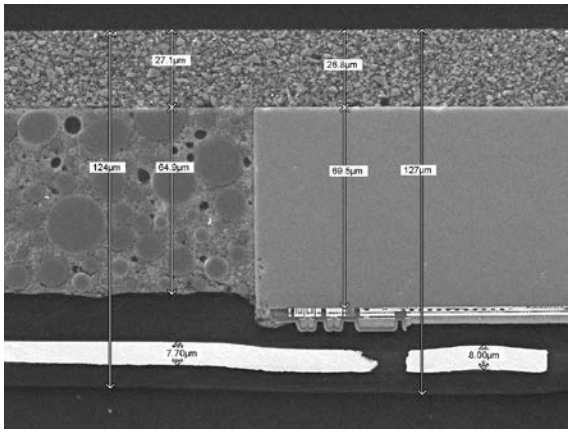






Ultra Thin Package Height (0.2mm)

Characteristic	Specification
PKG Size	6.2x7.0mm
Die Size	4x4mm
IO	400
Ball pitch	0.225mm
PKG Thickness	125 um
Si Die Thickness	65 um
RDL Thickness	25 um
BSP Thickness	25 um
Bump Height	75um
Total PKG Height	200um

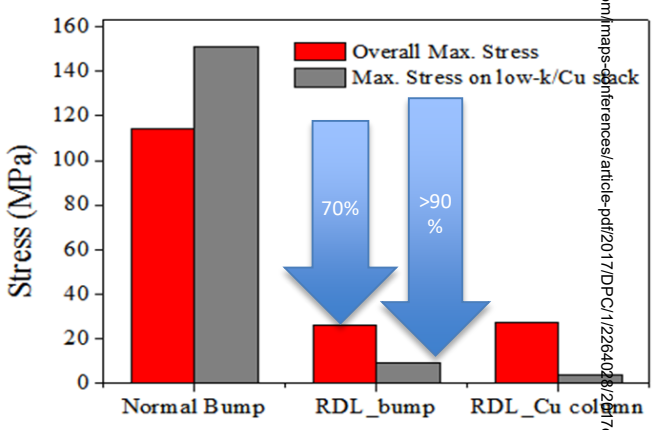


- Package height is ~0.2mm
- 75um bump height with microball drop
- Status: Completed feasibility study

Enhanced Reliability

Elimination of the substrate reduces one set of interfaces plus less stress on ELK by RDL, Both generally improving reliability

Enhanced Reliability

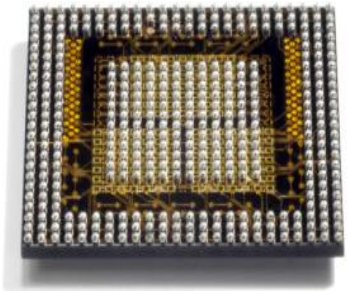


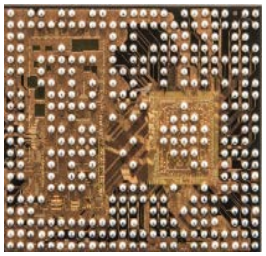
With RDL interconnects, bump stress does not directly affect ELK ILD/IMD stack layers, therefore, more mechanically reliable and robust.

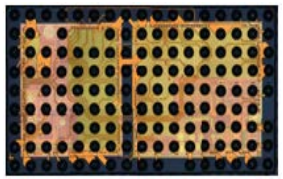
- Proven reliability for mobile/consumer products from 2009
- Currently HVM with 28nm products, Qualified with 20nm devices
- Qualified for Automotive AEC Q100 Grade-1

Integration Capabilities

Multi-die, passives, crystals, IPD, MLCC

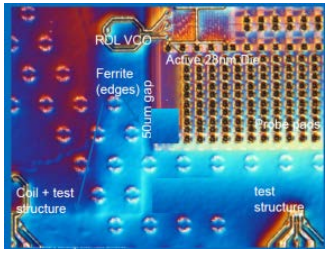


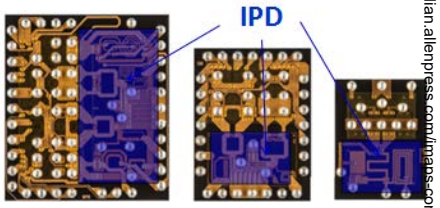




Side-by-Side: Multi-die & SiP applications

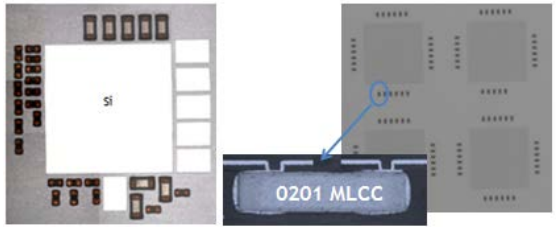
- Analog + Logic Package level integration (HVM from 2012)
- Functional partitioning
- Large-scale Side-by-Side Multichip
- Alternative solution of 2.5D Interposer
- 2/2um LW/LS with 3-L RDL





Crystal / IPD embedding

- Ferrite embedding for high Q performance of RF performance
- IPD for matching Functional partitioning

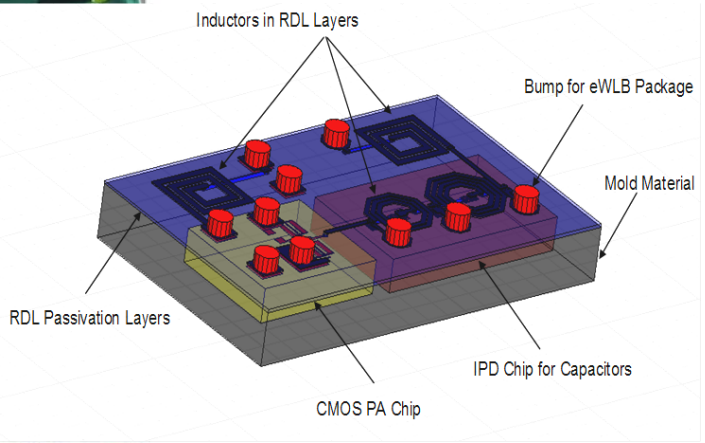


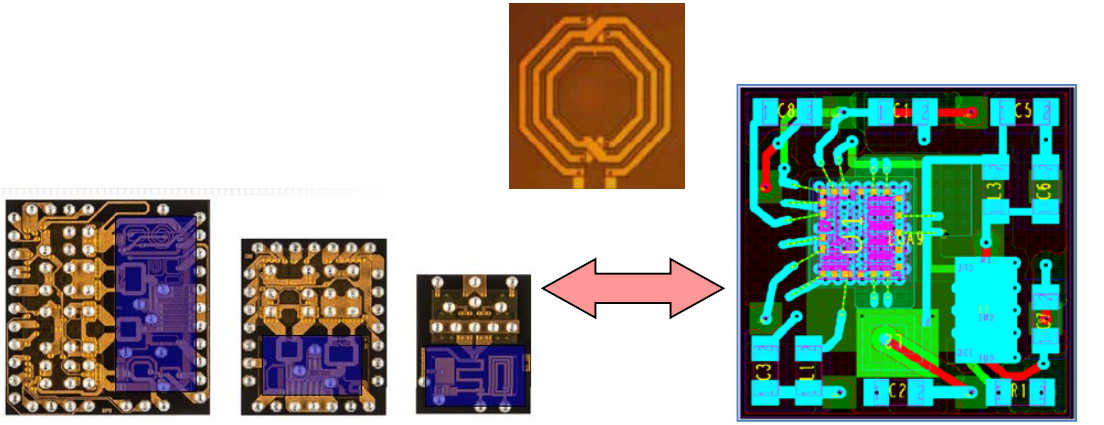
Discrete RLC embedding

- Qualified with 0201 MLCC
- MLCC with Cu metal finish

SiP Integration with IPD & RDL Inductor

eWLB helps enable high-integration with high-performance



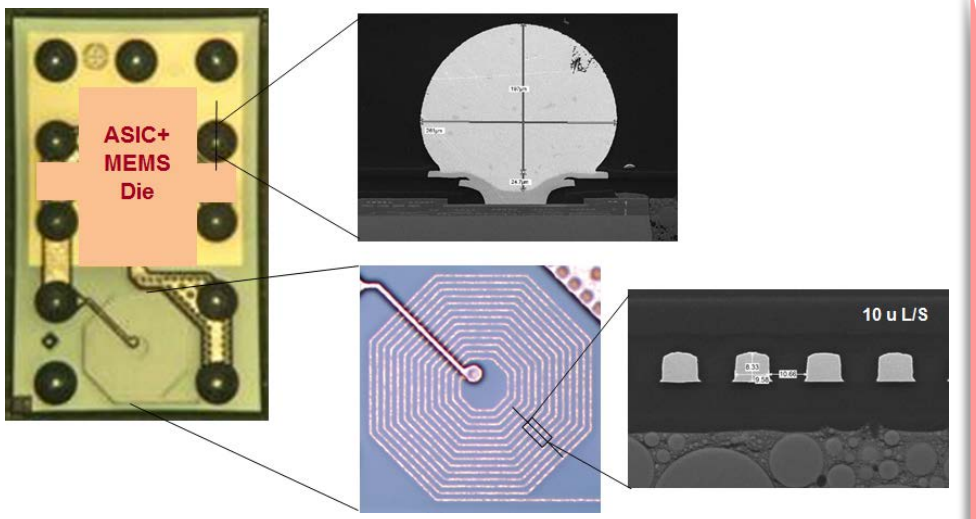


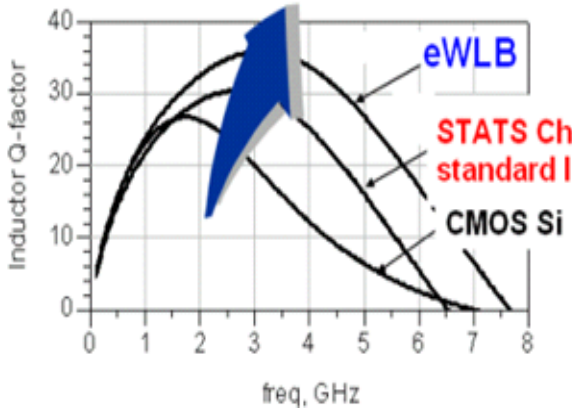
PA Module (eWLB version) **PA Module (SiP version)**

- Inductors can be made in RDL process using eWLB mold compound as supporting substrate for best Q
- CMOS chip (PA, for example) is embedded in the eWLB process and connected through RDL and bumps
- IPDs (capacitors, for example) can also be embedded in the eWLB process and connected through RDL and bumps

Improved Performance

Through features like thick Cu-RDL, embedded inductors, and IPD integration, eWLB provides flexible options to meet RF performance requirements (L, Q-factor etc.)

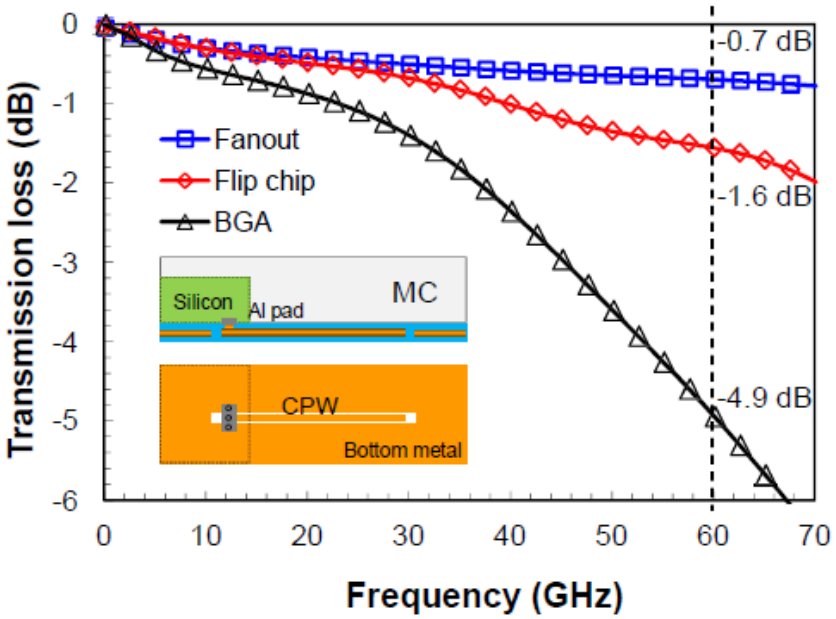


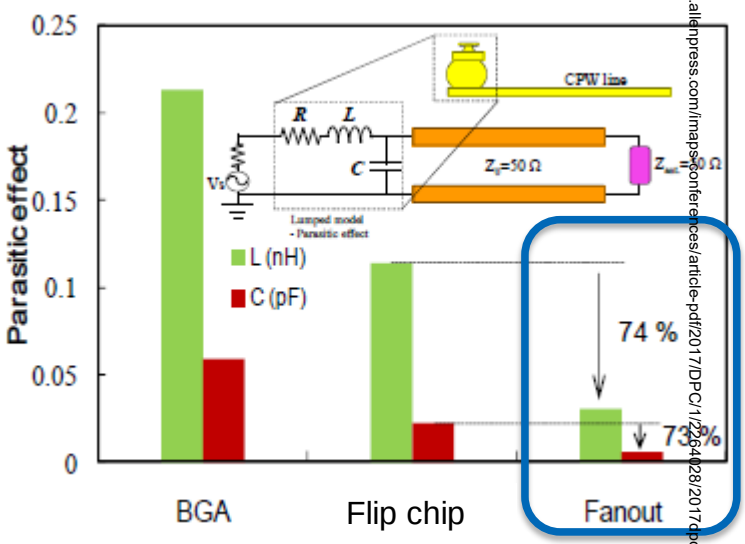


- Inductor Coil for RF with Cu RDL in eWLB
- High Q factor (>20) of Thick Cu RDL Inductor on EMC area
- RF MEMS Applications
  - Effective tuning ratio is doubled for eWLB vs WLCSP package.
  - High Q factor sustains performance while the low band antenna tunability improves.

High Frequency Performance

eWLB FOWLP for AiP, Antenna in Package @ mmWave High Frequency



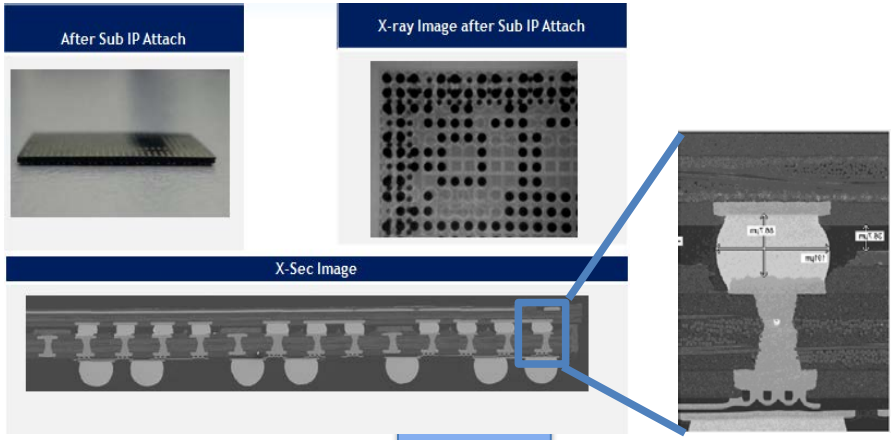


	FOWLP	Flipchip
Interconnect loss (dB)	0.7	1.6
Required power for PA output (mW)	11.7	14.5
Power saving (%)	**19%**	

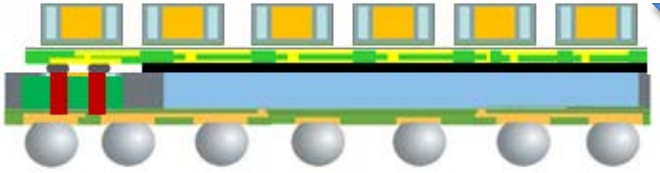
(source : TSMC, IEMD2013)

3D eWLB PoP : Interposer Type

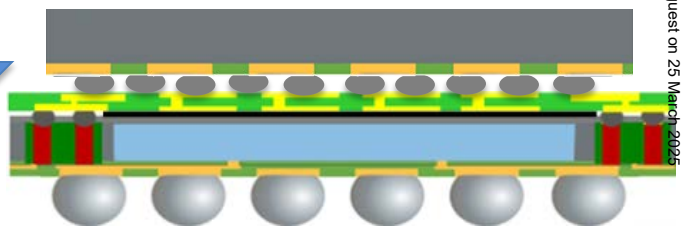
Interposer can support array type or customized memory ball out



Discrete SMT

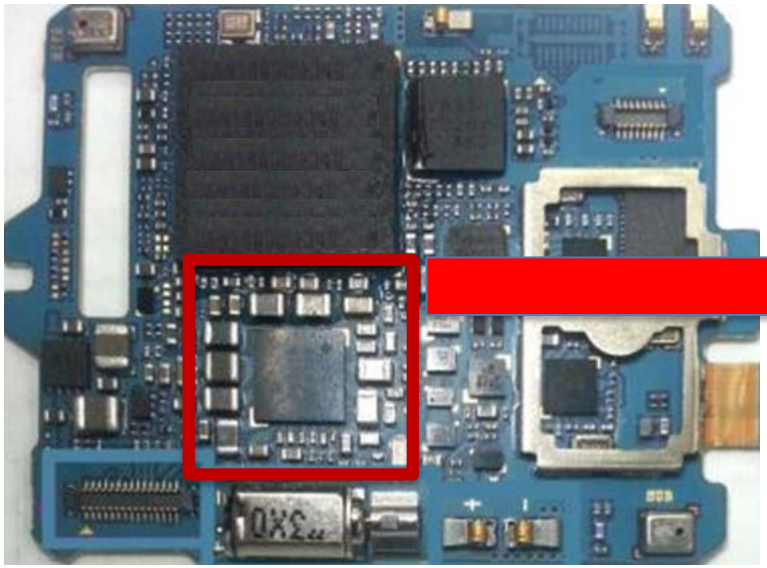


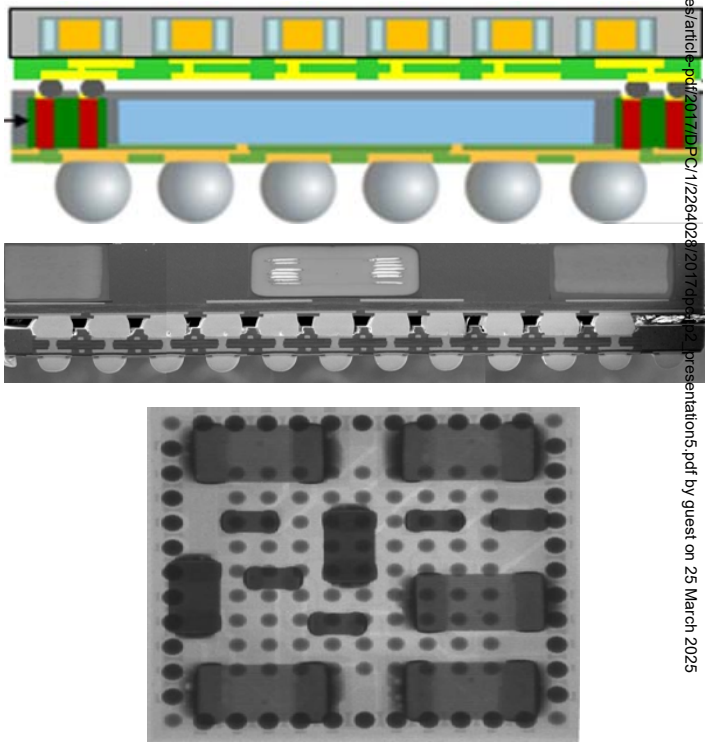
Array Type Memory PKG



eWLB SiP for Mobile/Wearable

- PCB real-estate is key concern for portable applications, especially for wearable electronics
- Discrete has occupied most of area in PCB
- Integration of discrete into package or embedded passive or IPD would be solution to save more PCB area
- Still total package height is critical

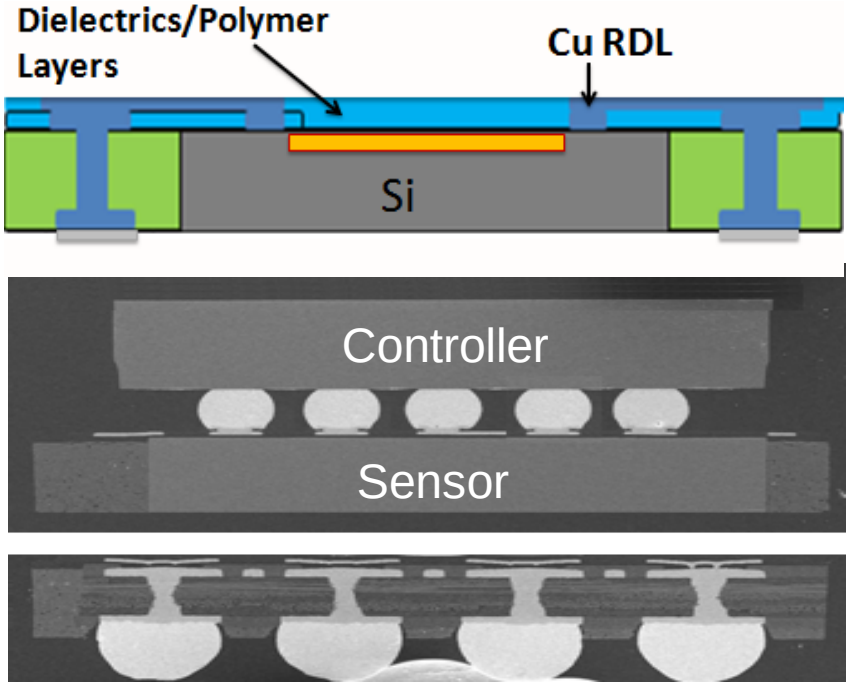




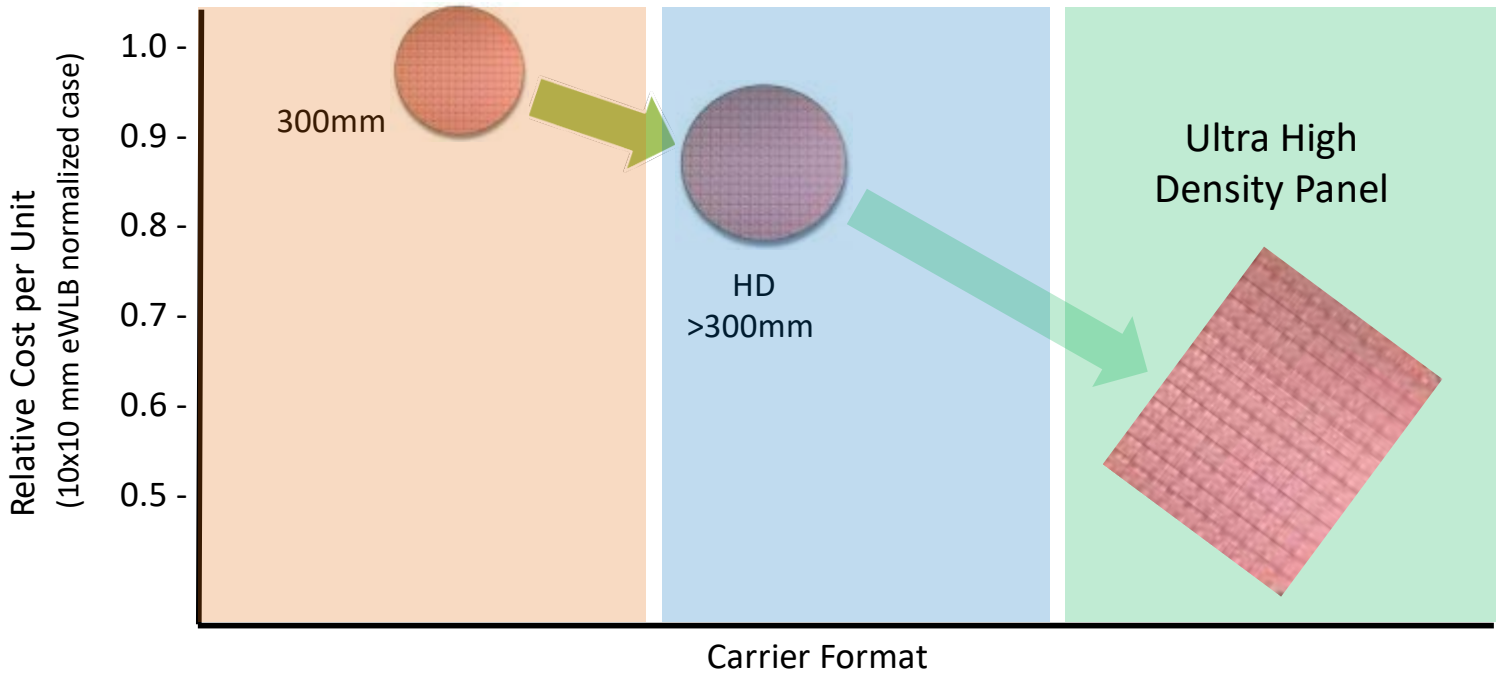
SmartWatch MotherBoard

Integrated Sensor/MEMS eWLB/ FOWLP

- Cost-effective Alternative solution of 3D TSV
- Thinner PKG Profile with 3D stacking
- Ideal for lower IO sensor of cost-sensitive
- Functionality and Reliability proven for functional sensor/MEMS devices



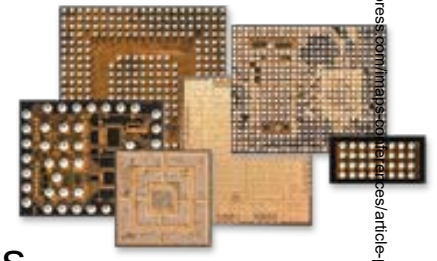
Cost Scaling with Larger Carrier Sizes



- FOWLP manufacturing lends itself to the use of larger carrier formats which has a direct impact on capital intensity and cost
- HD carrier formats have been qualified in volume production line since 2016
- Panel level processing is the most sensible for larger body sizes above 10x10mm

eWLB as an Innovative Integration Platform - Summary

- Advanced low profile and integrated 3D eWLB-PoP and eWLB SiP was developed using eWLB (FO-WLP) technology.
- Versatile platform for 2D, 2.5D and 3D integration that delivers product advantages in terms of higher I/O and thinner profiles in a reliable, cost effective package
- Advanced 3D eWLB-PoP / eWLB SiP technology provides a smaller form factor, increased performance value add and is proving to be a new 3D or SiP packaging platform that can expand its application range to various types of emerging mobile, IoT and WE including sensors/MEMS or automotive applicationse
- WLB has an aggressive cost reduction path from an already competitive cost structure. (300mm → HD →UHD)



Thank You

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Innovative Integration Solutions