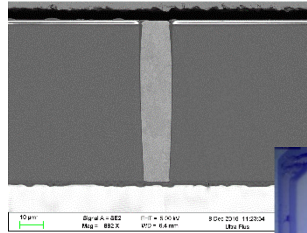
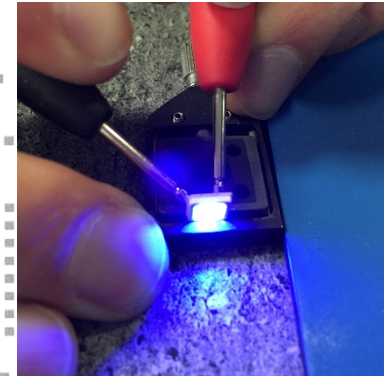
IMAPS 13th International Conference and Exhibition on Device Packaging
Phoenix, AZ, March 6-9 2017





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NEW WAFER LEVEL PACKAGING CONCEPT FOR POWER LEDS

Volpert Marion | 7/03/2017

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SOMMAIRE

1 Introduction: LED market and technology

2 The wafer level packaging approach

3 WLP fabrication process and characterizations

4 Device packaging development

5 Conclusion

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INTRODUCTION : THE LED MARKET

- **The invention of the high brightness blue LED and the phosphor implementation was a turning point for the development of white LEDs**

- **Rapid development of the LED industry in many applications:**
  - Displays
  - General lighting
  - Street lamps, traffic lights
  - Automotive lighting
  - Lighting for horticulture

- **More development with smart lighting yet to come (Li-Fi …)**

- **However :**
  - The reliability of the LEDs is generally limited by packaging issues
  - Packaging costs may represents up to 60% of the LED production cost

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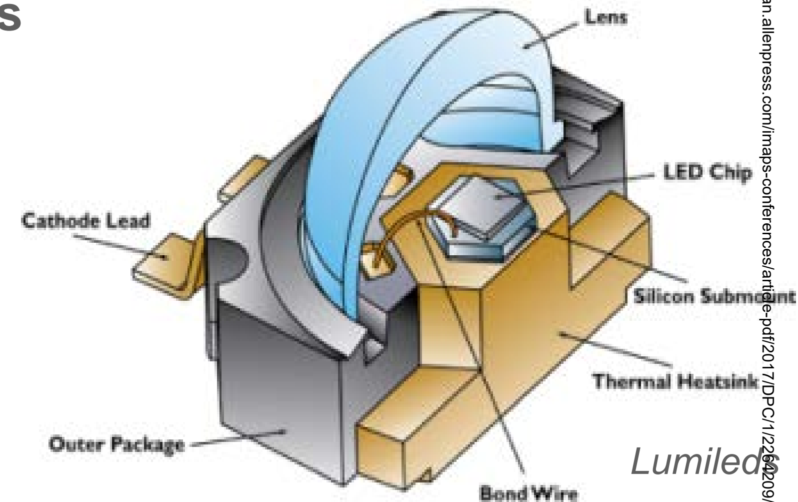
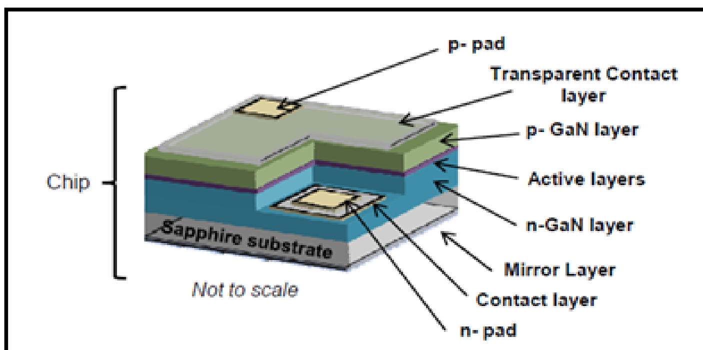
INTRODUCTION: THE LED PACKAGE

- **Lighting industry must deal with new semiconductor technology and thermal cooling via heat conduction**
- **Standard packages : SMT and COB devices**
  - Bond wires connections
  - Thermal heatsink
  - Encapsulation & lenses for light extraction, color conversion phosphors integration and beam shaping

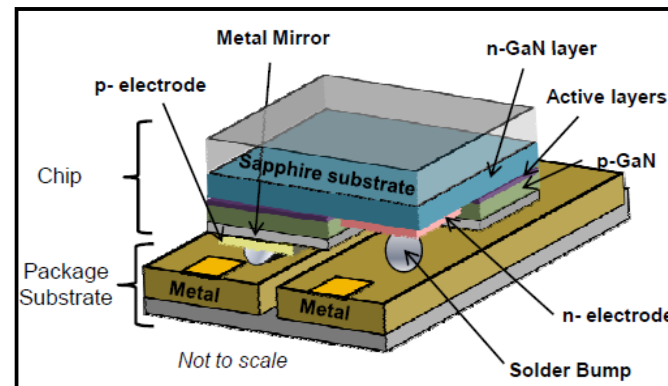


Lumileds

Example of LED chip (conventional)



Example of LED chip (Flip chip)



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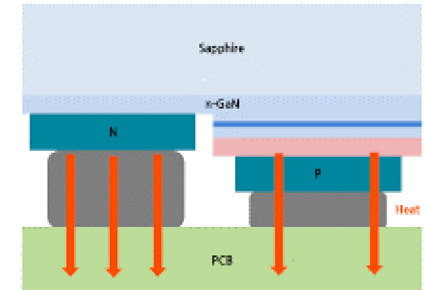
INTRODUCTION: WLP LED TREND (SOURCE SEOUL SC)

[WICOP]

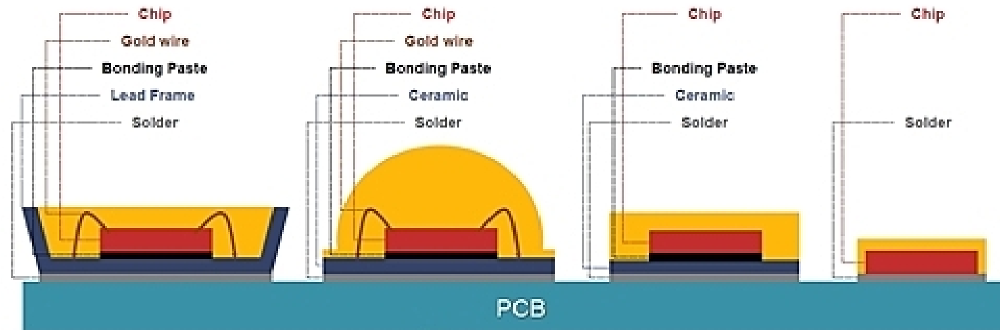
No Frame, No Gold wire, No Substrate, No Paste

=>Direct connection between Chip and PCB, Chip size=PKG size



WICOP2 ≠ CSP

Conventional PKG | CSP | Wicop2



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INTRODUCTION: ISSUES AND TREND

- **Main Issues:**
  - Wire bonding for VTF and CC structures : reduce the current capabilities
  - Large footprints
  - Light color conversion and mounting achieved mostly on singulated chips

- **Market trend:**
  - More functions
  - Smaller and thinner package
  - More power, more robust
  - User friendly
  - Cost reduction

Tendency to go towards:
- Flip chip LED
- Compatibility with 3DIC Integration

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INTRODUCTION: LED TECHNOLOGY

- **Standard LED technology is based on epitaxial growth of GaN on sapphire or SiC**
- **Requires technological challenges to transfer the LEDs to a silicon substrate for Vertical Thin Film configuration**
- **No true wafer level packaging solutions exist for :**
  - Bumping and RDL
  - Encapsulation and light conversion (only on Chip to wafer)

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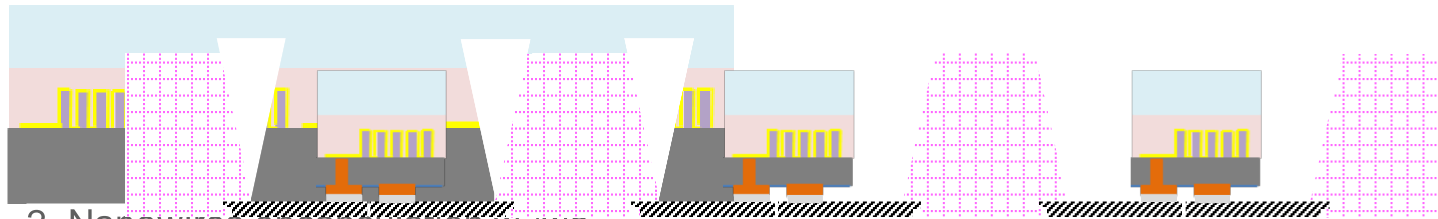
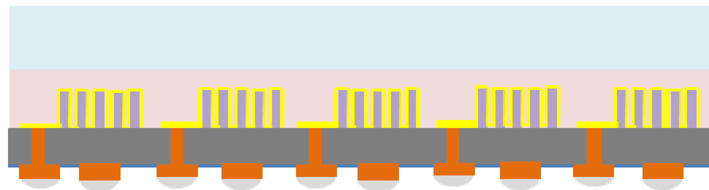
THE WAFER LEVEL PACKAGING CONCEPT AT A GLANCE

1. Fabrication of the GaN wireLED on doped Si

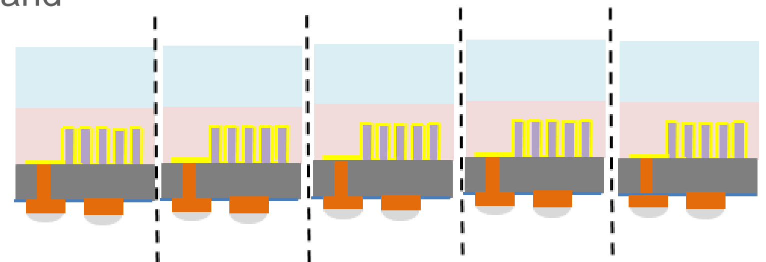


2. Nanowires encapsulation w /wo phosphors and glass ca

5. QFN mounting: collective reflow



3. Back side process : TSV, RDL and bump or pads fabrications



4. Dicing the SMT LEDs

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OUR WAFER LEVEL PACKAGING APPROACH

- **Fully compatible with semi conductor fabrication process**
- **P and N contact on the backside for SMT ready integration**
- **Batch process for LED color conversion and encapsulation**
- **Specific lead-frame to address high power LEDs**
  - Thermal management (spreading issues)
  - Collective reflow

Miniaturization

Electrical performances

Cost

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MAIN TECHNOLOGICAL PROCESS STEPS

- LED Fabrication : GaN nanowire epitaxial growth
- Front End processing and N,P patterning
- LED encapsulation

- Handler bonding (permanent or temporary)
- Wafer thinning
- TSV-Last fabrication
- Back side metallization
- Testing
- Dicing
- Lead frame assembly

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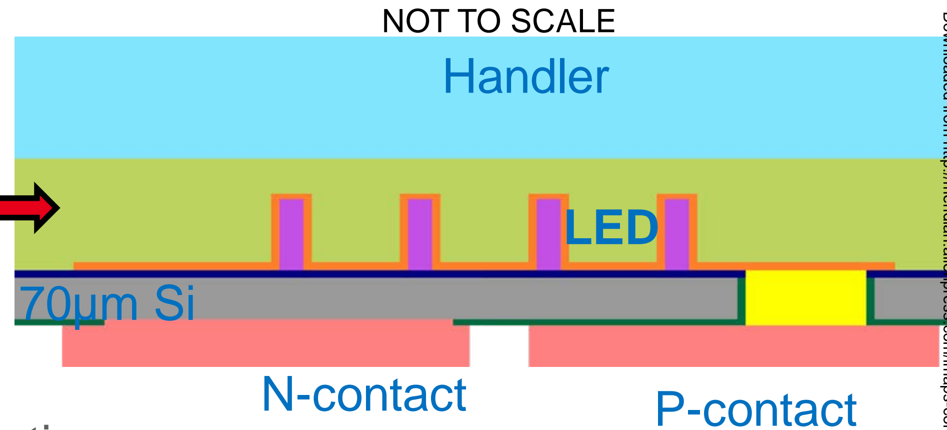
MAIN ISSUES



- **Polymer bonding :**
  - Compatibility with lighting application
  - Insure low TTV (<5µm) over the whole wafer
  - Low temperature (<200°C) compliant process
- **Wafer thinning:**
  - Stress induced process
  - Damaged Si zone must be removed
- **TSV-Last with high A/R (5 compared to a standard of 2)**
  - Destructive cross section characterization
  - Low temperature dielectric liner deposition

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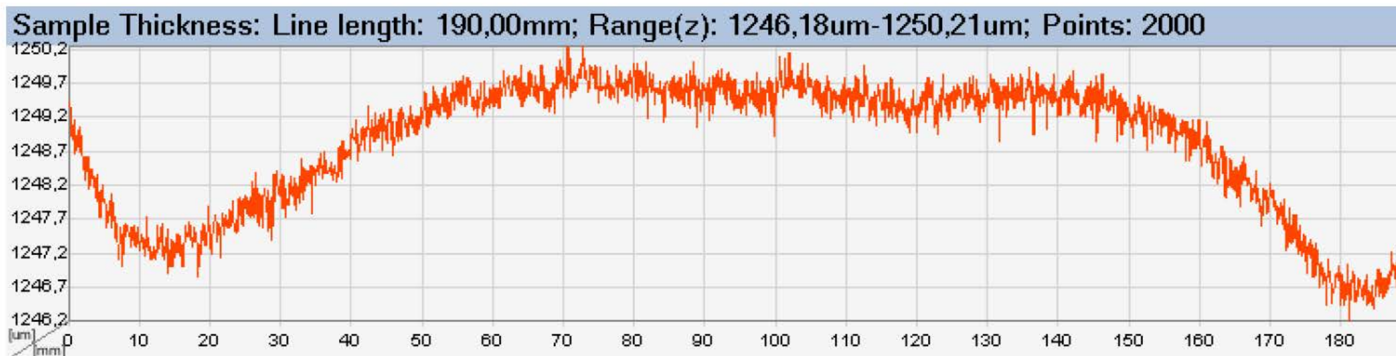
BONDING AND THINNING PROCESS

- **TTV after bonding : 5µm avg**
- **Bow after bonding : 120µm**
- **Bow during thinning :**
  - After coarse grinding down to 200µm : Maximum at 480µm
  - After thin grinding down to 150µm : 240µm avg
- **Bow after thinning and throughout the whole process <150µm**

Measurement done on FRT: Thickness after bonding



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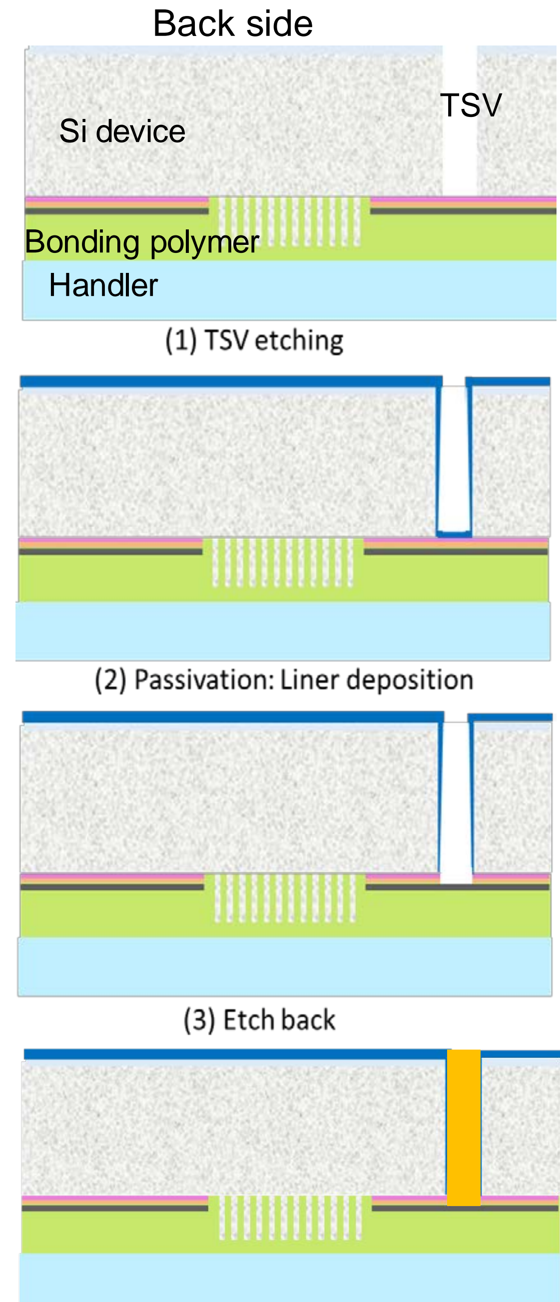
TSV FABRICATION

- **High AR (~5) with low opening ratio:**
  - Si Etching time to be assessed
  - Dielectric liner conformity to be evaluated
  - Etch back time to be assessed
  - Copper filling to be developed

Destructive characterization



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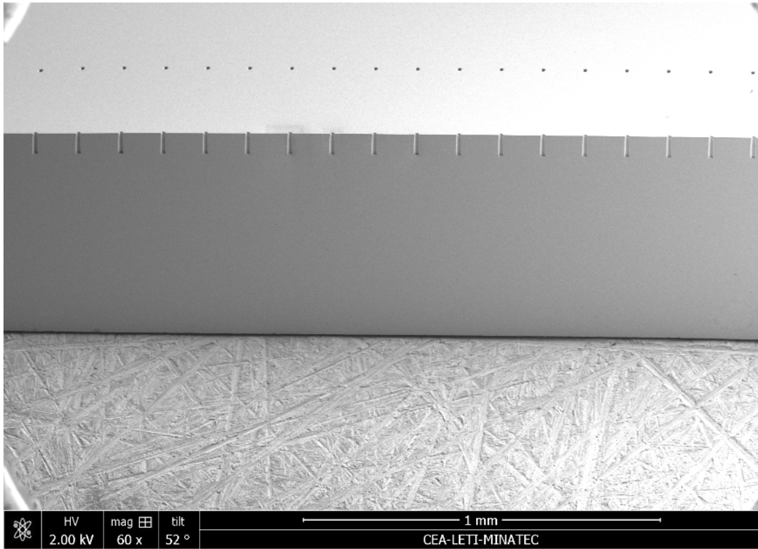
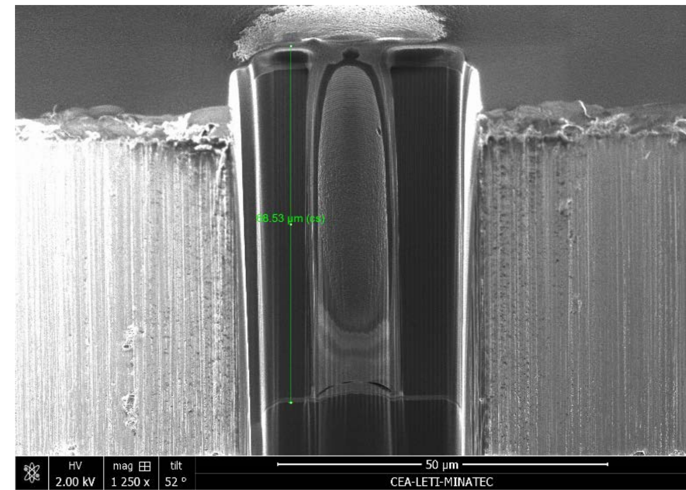
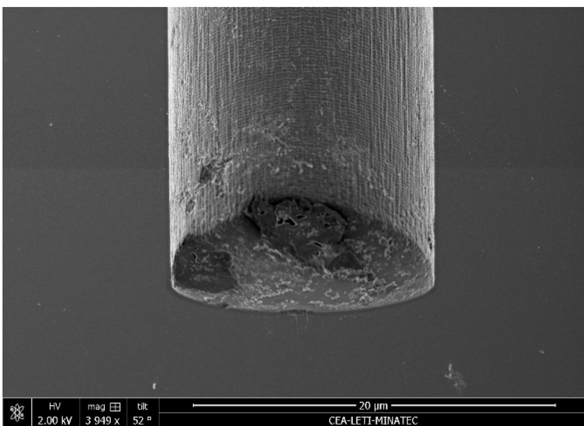
CHARACTERIZATION METHOD

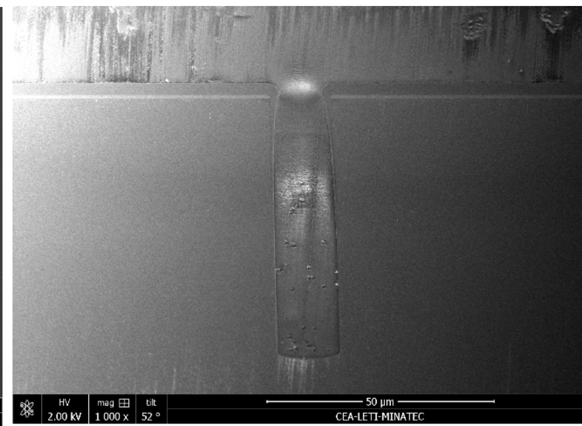
- **Mechanical polishing:**
  - Fast
  - Create defects



- **FIB observation :**
  - Time consuming
  - Edge effect, AR too high







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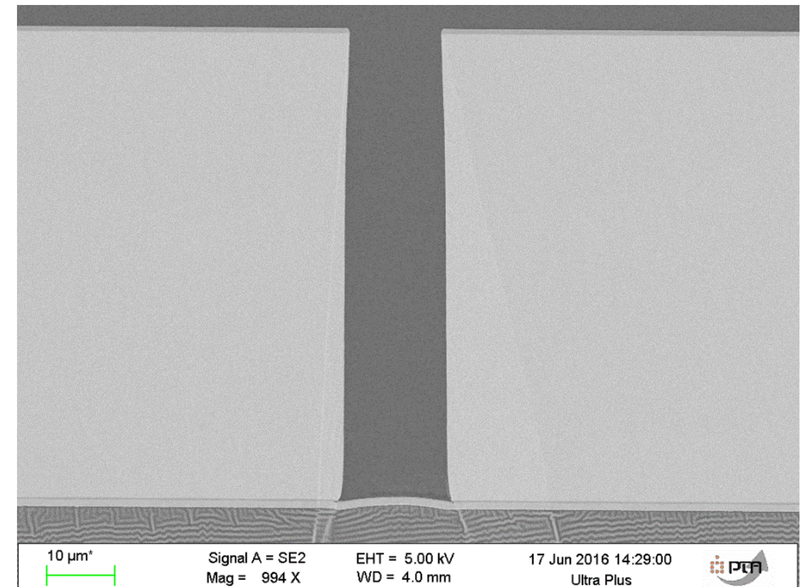
DEVELOPMENT OF A CHARACTERIZATION METHOD

- **TSV filling with resin to avoid edge effect**
- **Mechanical polishing using CENTAR equipment to approach the TSV very closely**
- **Ion beam etching using a ILLIONS equipment to cut a cross section within the TSV**
  - Slight edge effect at the corner
  - No damage of the bonding polymer



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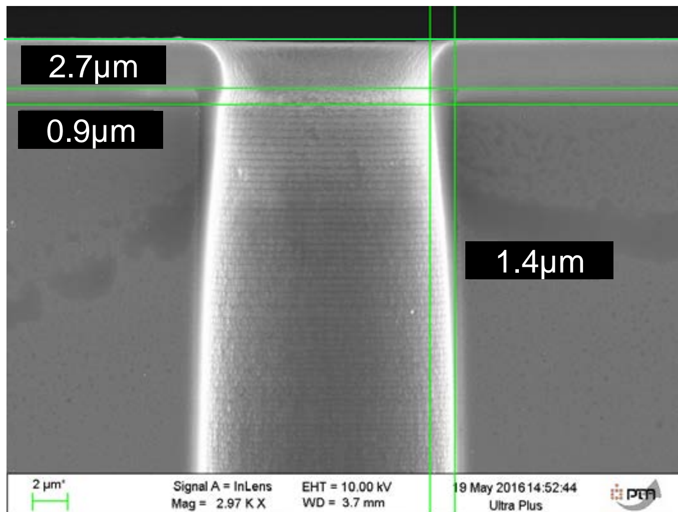
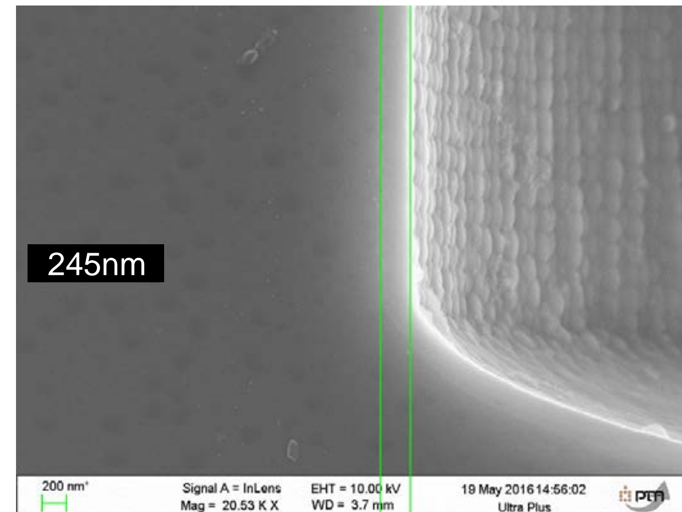
FABRICATION DEVELOPMENT (1/3)

- **Dielectric liner conformity validated on dummy wafers**

TSV TOP



TSV BOTTOM



About 50% of liner deposited on the top sidewall
About 9% of liner deposited on the bottom

➔ Define the top thickness to deposit

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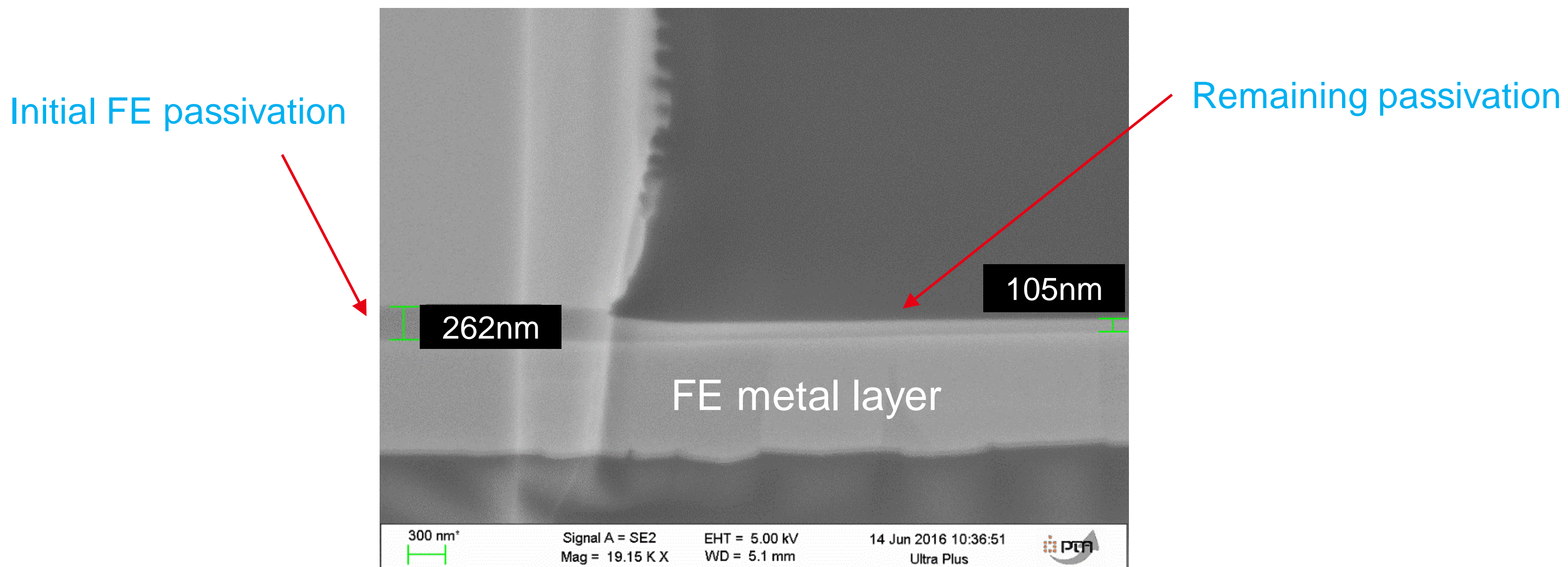
FABRICATION DEVELOPMENT (2/3)

- **Etch back study validated on bonded dummy wafers**
  - Two step etching process : to remove the BE + FE dielectric and stop on the FE metal layer
  - Partial etching of passivation to define the etching rate



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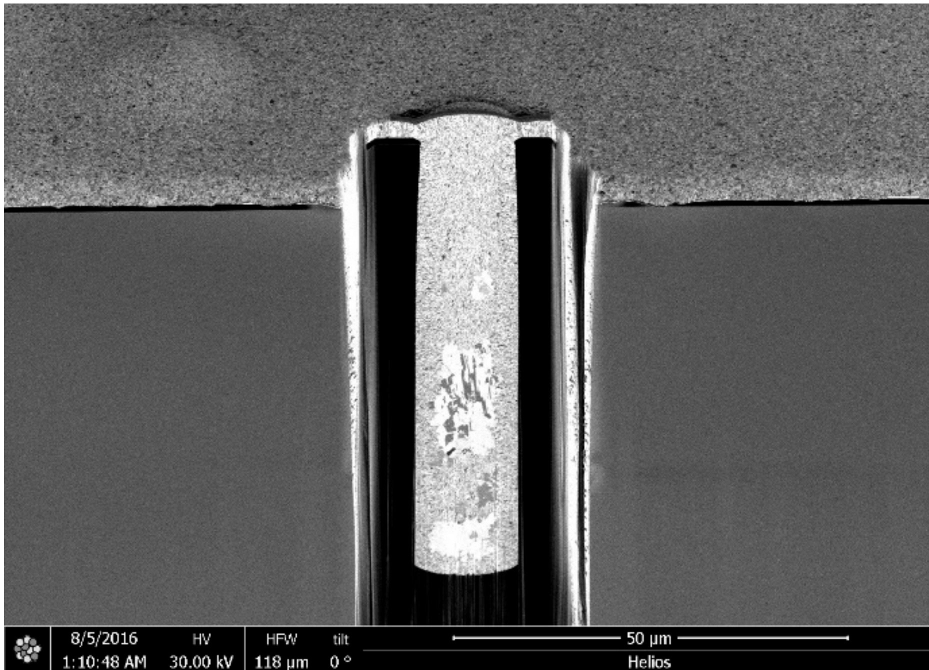
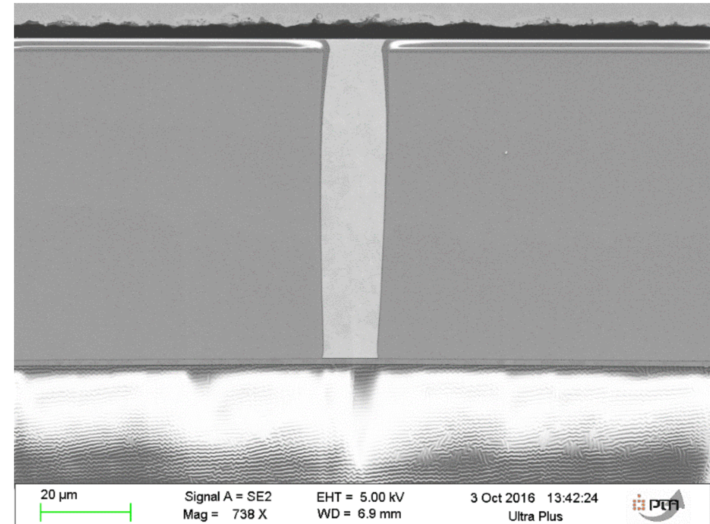
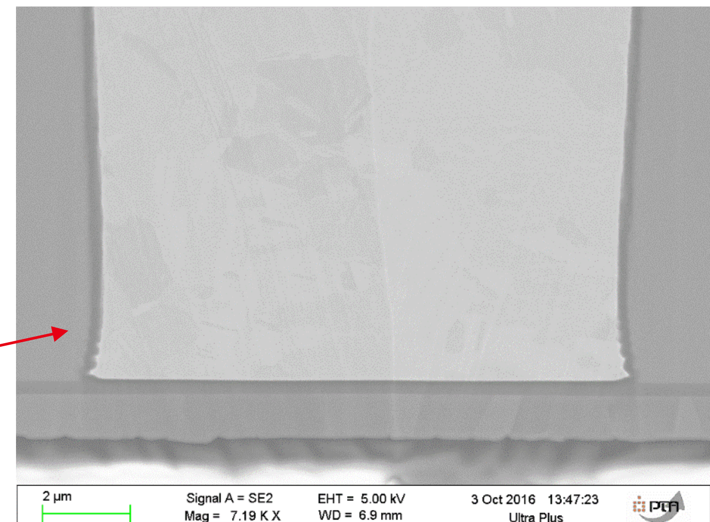
FABRICATION DEVELOPMENT (3/3)

- Cu ECD validation on dummy wafers and bonded wafers





Bottom of TSV



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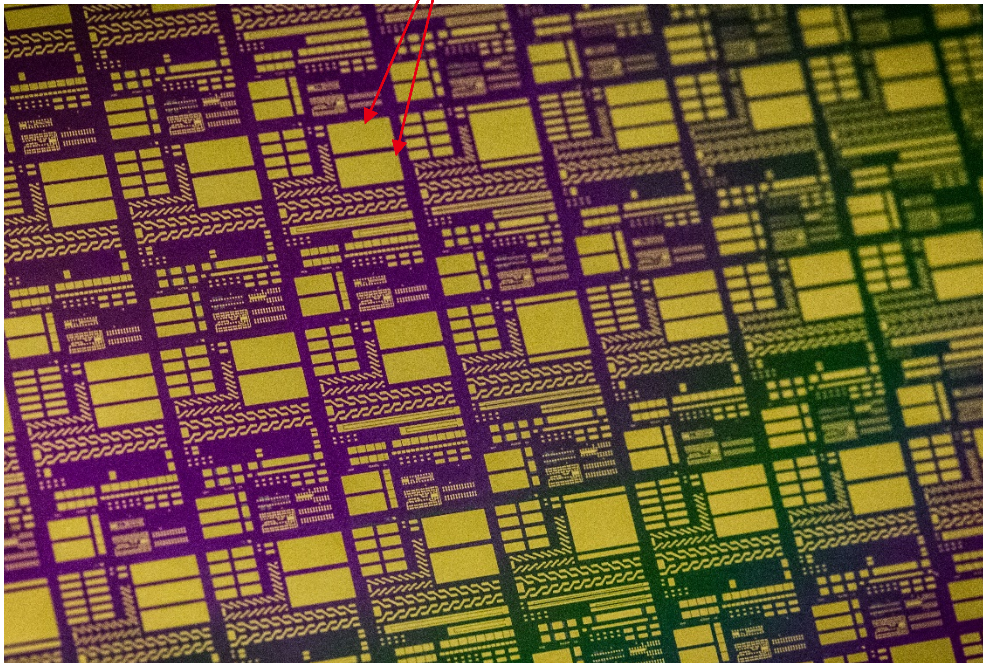
DEMO FABRICATION

- Implementation of all developed process parameters on fully functional wafers
- Ti/Ni/Au metallization for N and P back side contact
- Design of test patterns for electrical characterization

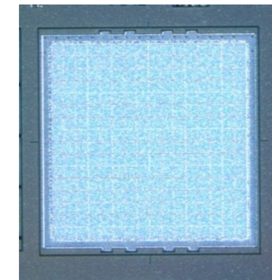
Back side view:

N and P contact



Front side view :

2x2 mm LED



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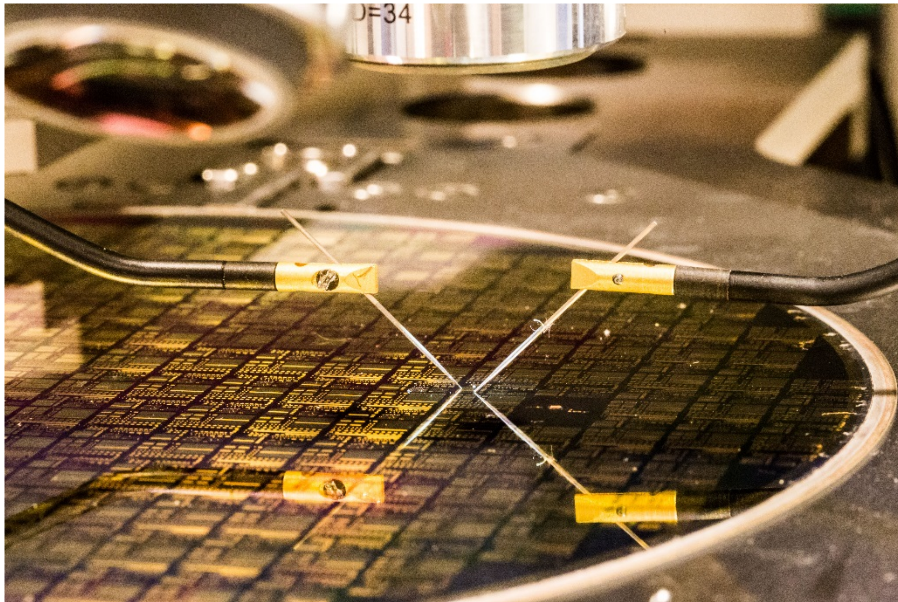
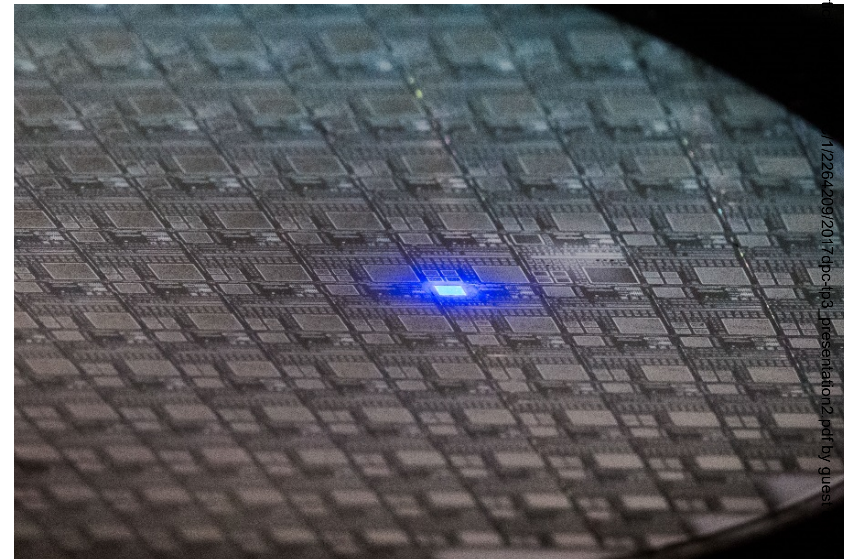
OPTICAL AND ELECTRICAL CHARACTERIZATON

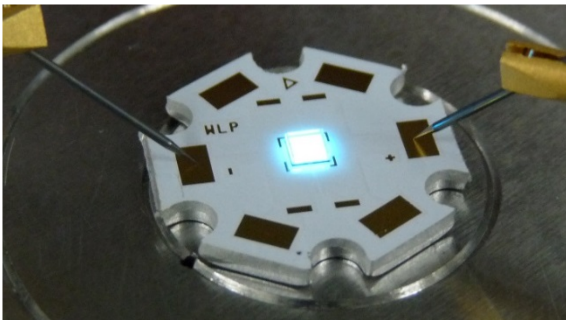


- **Electrical characterization showed**
  - Median resistance is 60mΩ per TSV (with some dispersion)
  - Breakdown voltage between two TSVs between 80V to 110V

Suitable for the application
Process need to be matured



- **Wafer Level optical test showed**
  - About 70% functional dies
  - Failure causes under investigation



Optical test on IMS starboard

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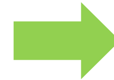
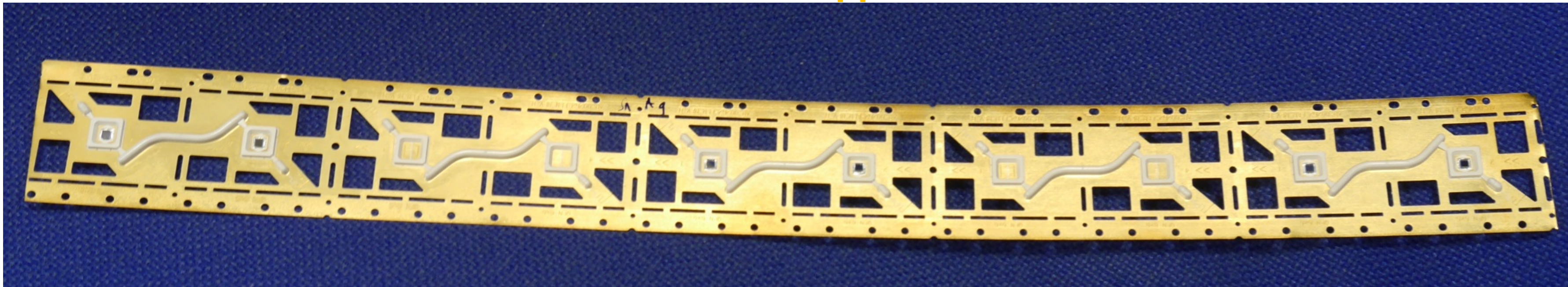
ASSEMBLY DEVELOPMENT

- ✓ Specifically designed lead-frame QFN
- ✓ Different solder formulations and solder thickness tested
- ✓ Different die thickness tested
- ✓ Different reflow process
- ✓ 4 Different LF design

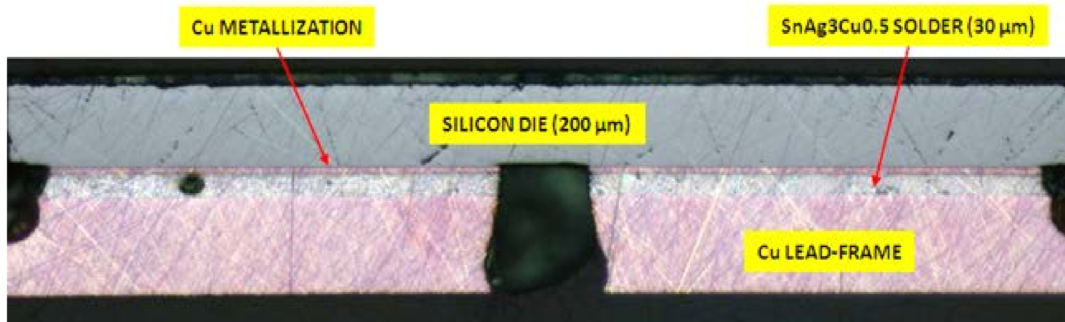


- ➢ Optimize thermal dissipation
- ➢ Reduce thermal stress
- ➢ Increase reliability

Copper LF with NiAu finish



Thinned dummy die for assembly development



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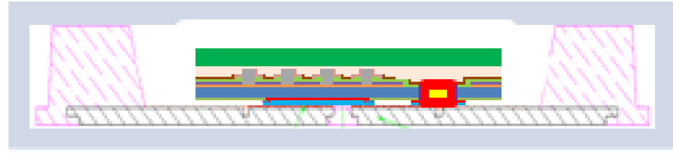
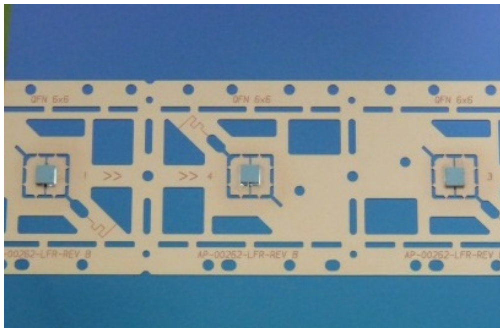
DEMO FABRICATION

Cross section view of the die mounted on the lead-frame into a package

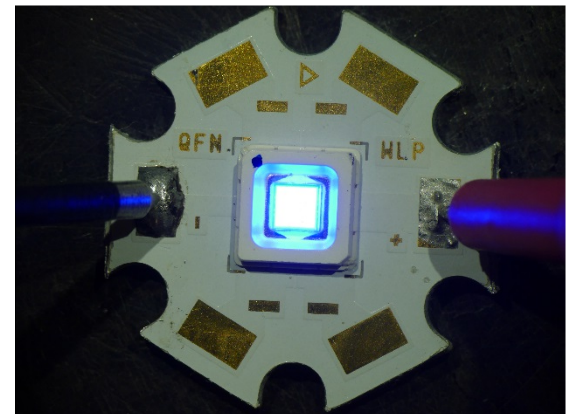


1. Collective assembly of dies: reflow in a belt oven



2. After QFN mounting

3. Test after packaged in the IMS



Dies were successfully mounted and tested

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CONCLUSION

- **A new wafer level packaging approach has been demonstrated with promising results**

- **Some WLP technological development were achieved to fabricate high AR TSV-last (~5):**
  - Characterization technique
  - Etch rate for silicon, TSV passivation and Cu ECD qualified

- **QFN package was specifically designed**

- **Perspectives**
  - Implementation of color conversion at the wafer level
  - Increase the maturity level of TSV fabrication
  - Achieve reliability tests
  - Complete some thermal measurements to fully characterize the QFN power package efficiency

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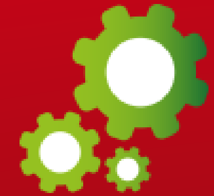
Thanks for your attention

QUESTIONS ?



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