Multi-Scale Modeling of Self-Heating Effects on Power Consumption in Silicon CMOS Devices

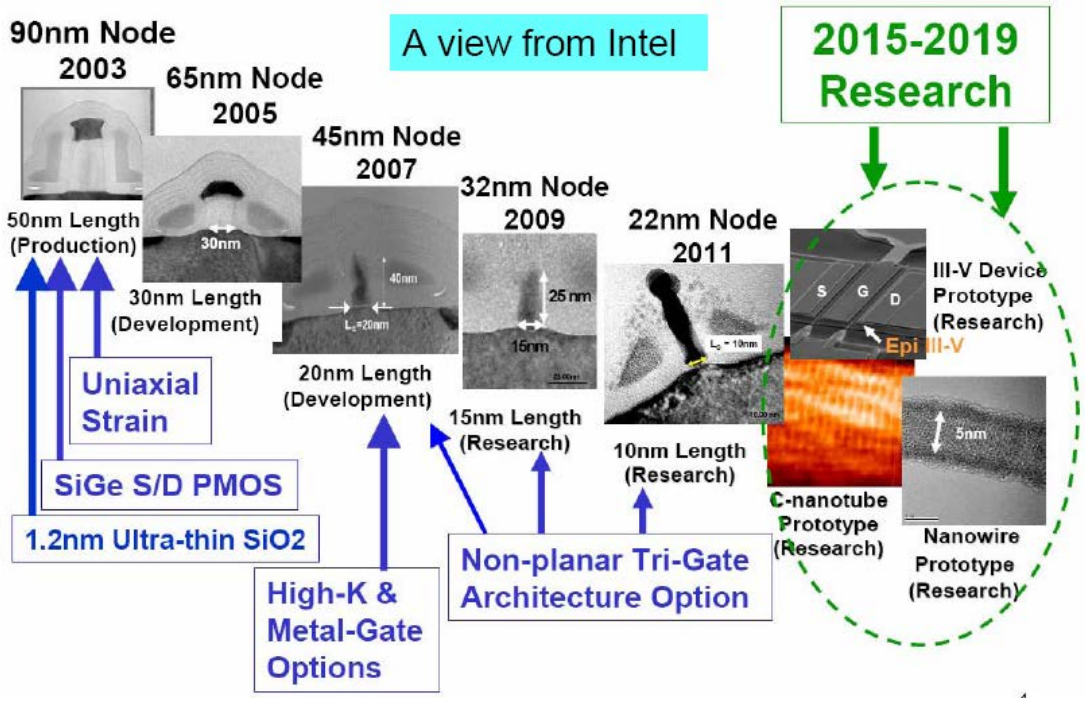
R. L. Daugherty, S. S. Qazi, A. R. Shaik, P. Muralidharan, and D. Vasileska

School of Electrical Computer and Energy Engineering, Arizona State University, Tempe, AZ, USA

Outline

- Motivation
- Thermal Transport
- Electro-Thermal Effects
- Device Modeling
- Multiscale Modeling
- Experimental Methods
- Results
- Future Work
- Conclusions

Motivation: Transistor Scaling



Some avenues for reducing transistor size or increasing on-chip density:

1. Alternative Materials
- Strained Si
- Strained SiGe
- High-K dielectrics

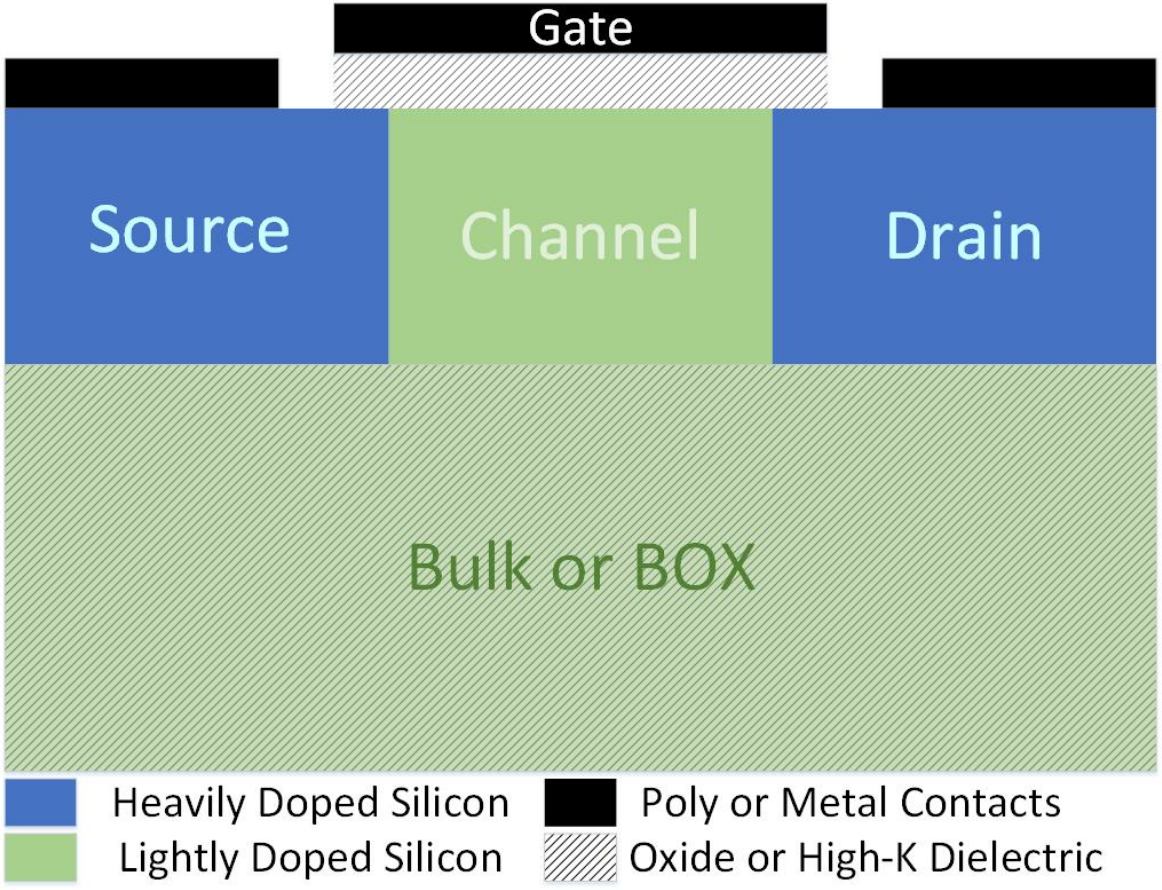
2. Alternative Devices
- FD SOI Devices
- Dual-Gate Devices
- FinFETs

3. Alternative Architecture
- Vertical Integration

Motivation: Why CMOS Modeling?

- Few applications use exclusively NMOS or PMOS
  - Some analog applications (BJTs?)
  - Active loads will still use CMOS
- Most digital circuit applications use CMOS
  - Power consumed only during switching or through leakage currents
  - More robust than NMOS or PMOS for most types of gates and buffers
- Physical interaction between closely spaced and inter-connected devices in CMOS circuits can be better understood by modeling both NMOS and PMOS devices simultaneously

Motivation:
Why Electro-Thermal Modeling?



Material	k_{th} (W/mK)
Si	148
Ge	60
Silicides	40
Si (10 nm)	13
SiO_2	1.4

Thermal conductivity for materials in semiconductor microelectronics

Poor thermal conductivity!

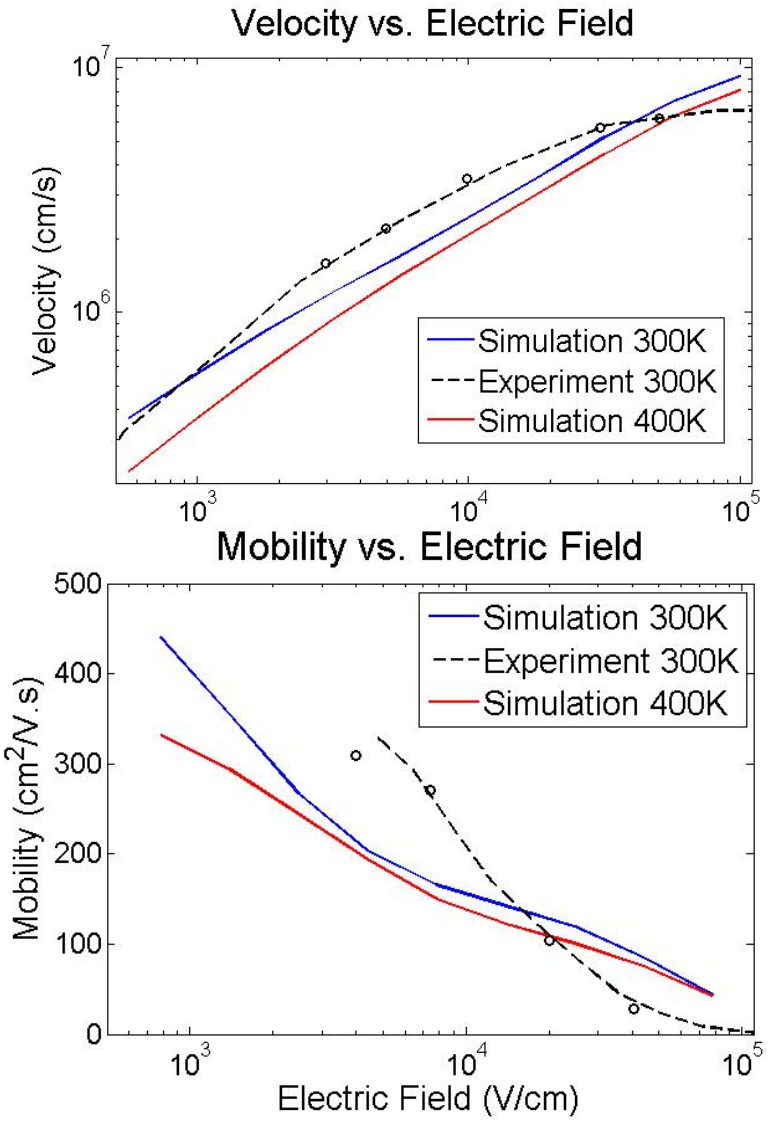
- Gate dielectric
- Buried oxide layer

(in SOI devices)

- Thin silicon channel

(in nanoscale devices)

Motivation:
Why Electro-Thermal Modeling?



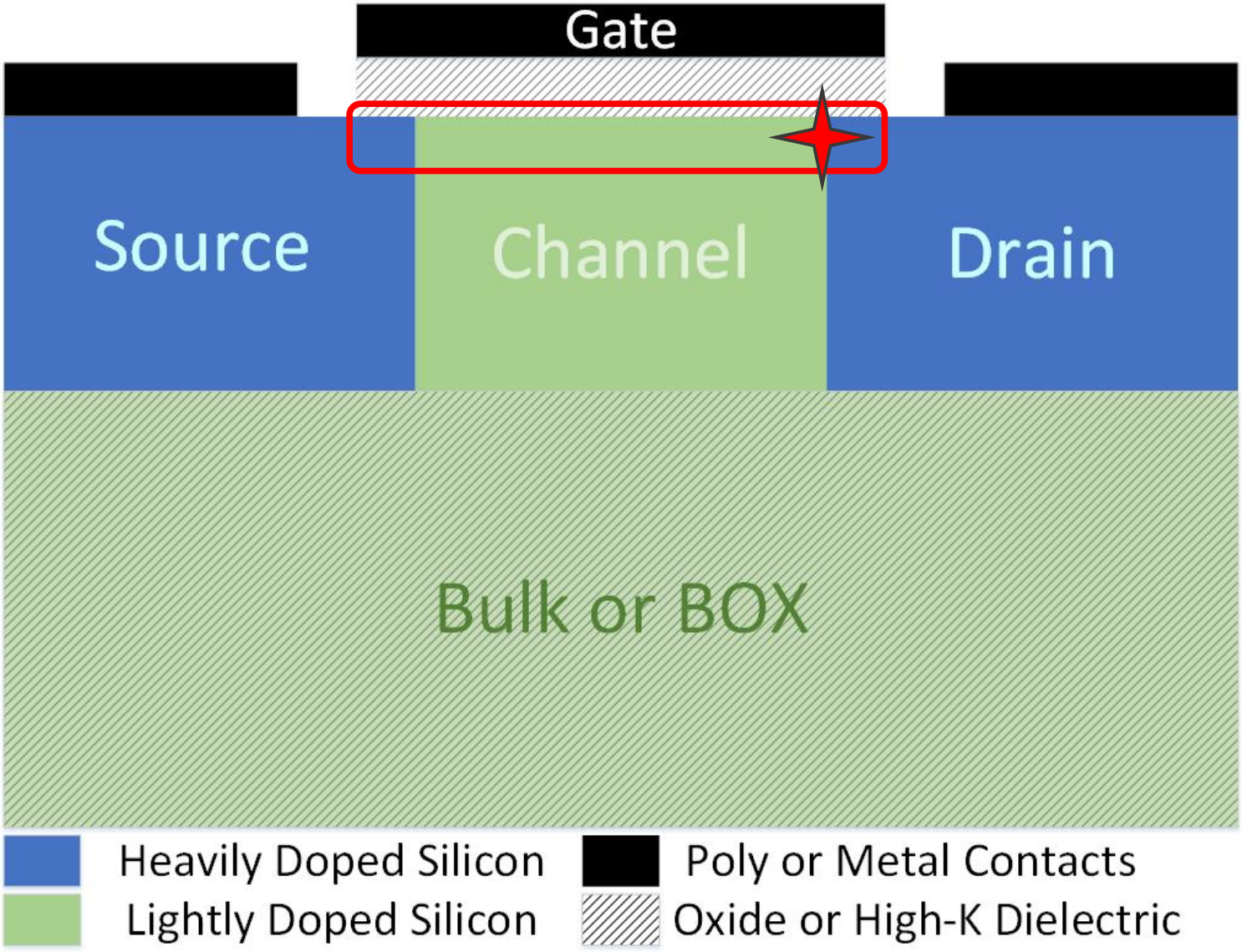
Degradation at increased temperatures!

- ❑ Velocity
- ❑ Mobility

This directly affects device performance:

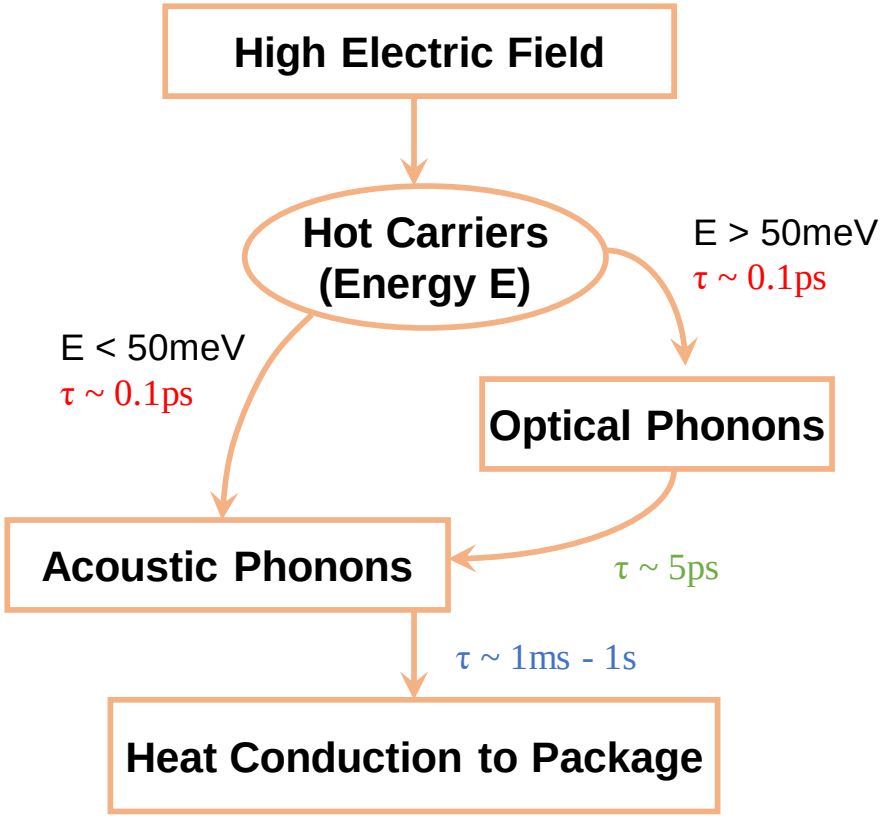
- ❑ Current Density
- ❑ Gain in Analog Amplifiers
- ❑ Switching Speed in Digital Circuits

Motivation:
Why Electro-Thermal Modeling?



Theoretical Model for Thermal Transport through Phonons

- Hot carriers (electrons or holes) quickly*1 release energy via acoustic or optical phonon scattering
- Optical phonons decay*2 into acoustic phonons
- Acoustic phonons slowly*3 conduct heat away from the device active region



Modeling of Electro-Thermal Effects

We solve self-consistently, via a global loop, the:

- *Boltzmann Transport Equation (BTE) for the Electrons or Holes* (using the Monte Carlo method) self-consistently coupled to a 2D Poisson Equation Solver
- *Energy Balance Equations for the Acoustic and Optical Phonons*

The BTE is solved by calculating the scattering rates and selecting the appropriate scattering mechanisms for the carriers (electrons or holes)

$$\frac{\partial f}{\partial t} = \left(\frac{\partial f}{\partial t}\right)_{force} + \left(\frac{\partial f}{\partial t}\right)_{diffusion} + \left(\frac{\partial f}{\partial t}\right)_{collisions}$$

$$\frac{\partial f}{\partial t} + \frac{\mathbf{P}}{m}\cdot\nabla f + \mathbf{F}\cdot\frac{\partial f}{\partial \mathbf{P}} = \left(\frac{\partial f}{\partial t}\right)_{collisions}$$

The energy balance equations are solved iteratively by solving 2nd order elliptic partial differential equations

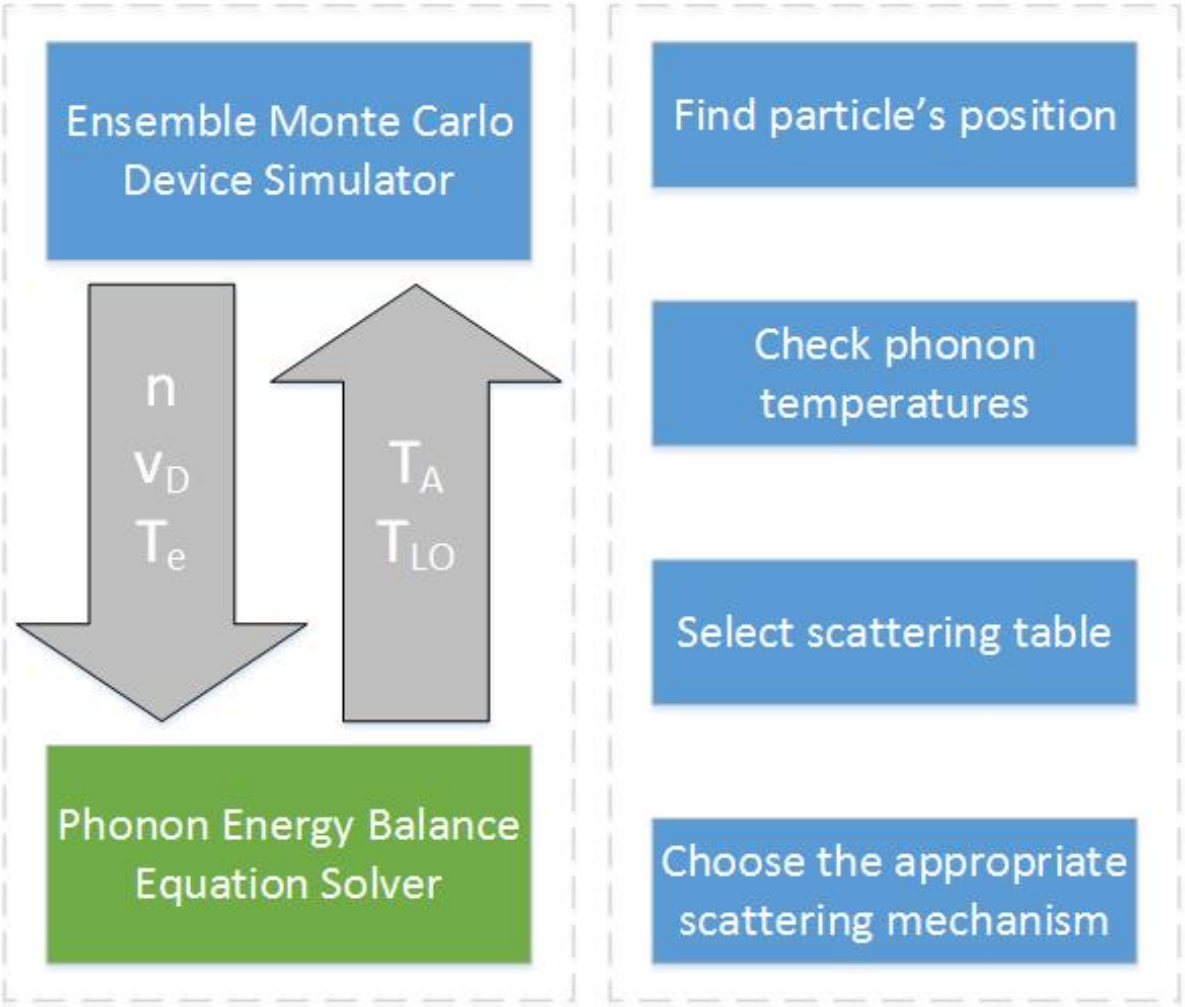
$$C_{LO}\frac{\partial T_{LO}}{\partial t} = \frac{3nk_B}{2}\left(\frac{T_e - T_{LO}}{\tau_{e-LO}}\right) + \frac{nm^* v_d^2}{2\tau_{e-LO}} - C_{LO}\left(\frac{T_{LO} - T_A}{\tau_{LO-A}}\right)$$

$$C_A\frac{\partial T_A}{\partial t} = \nabla\left(k_A\nabla T_A\right) + C_{LO}\left(\frac{T_{LO} - T_A}{\tau_{LO-A}}\right) + \frac{3nk_B}{2}\left(\frac{T_e - T_A}{\tau_{e-A}}\right)$$

Device Modeling:
Monte Carlo – Energy Balance Coupling

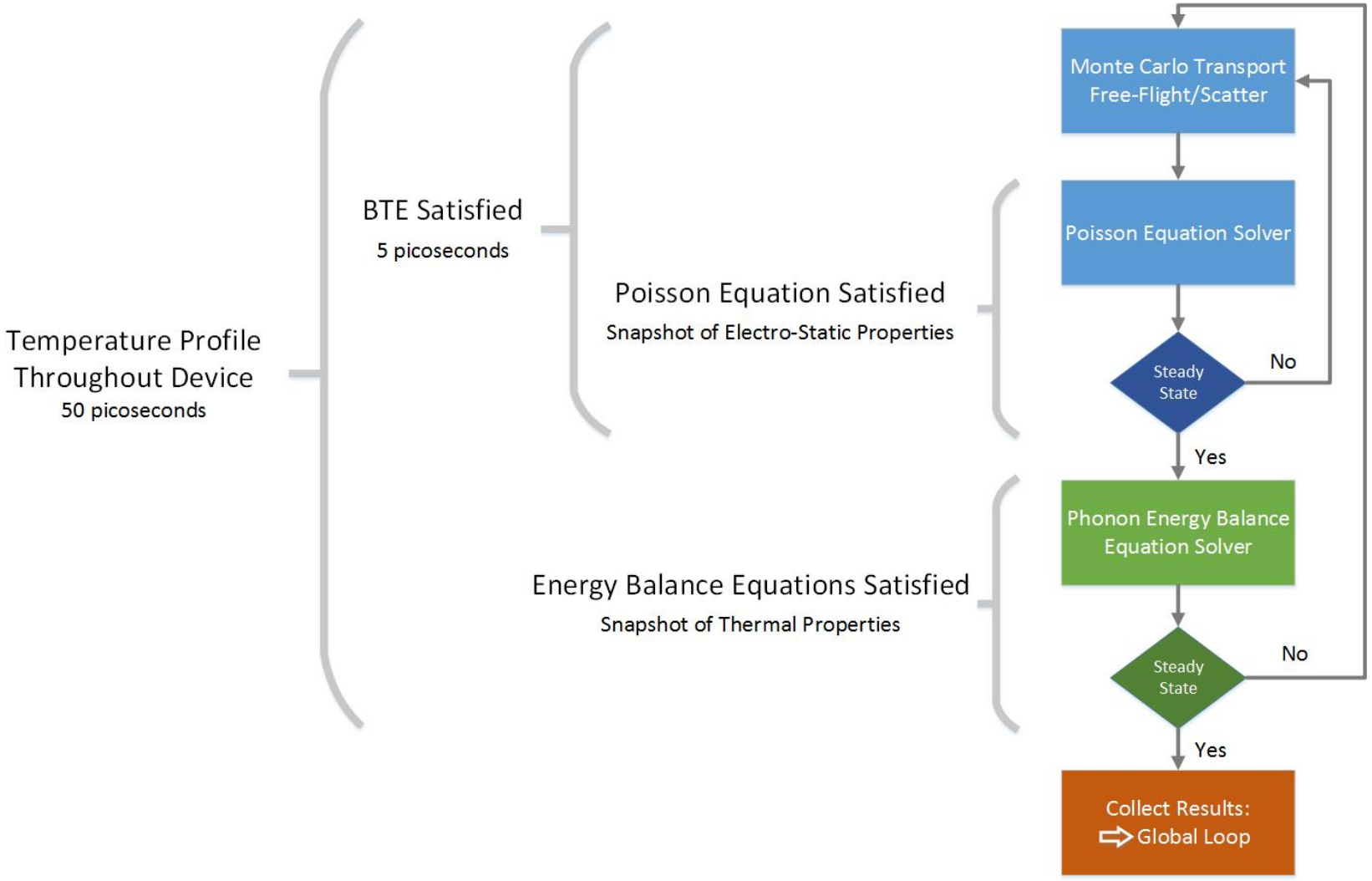
Particle Model

Fluid Model



K. Raleva, D. Vasileska, S. M. Goodnick and M. Nedjalkov, Modeling Thermal Effects in Nanodevices, IEEE Transactions on Electron Devices, vol. 55, issue 6, pp. 1306-1316, June 2008

Device Modeling:
Flow-chart of Electro-Thermal Solver



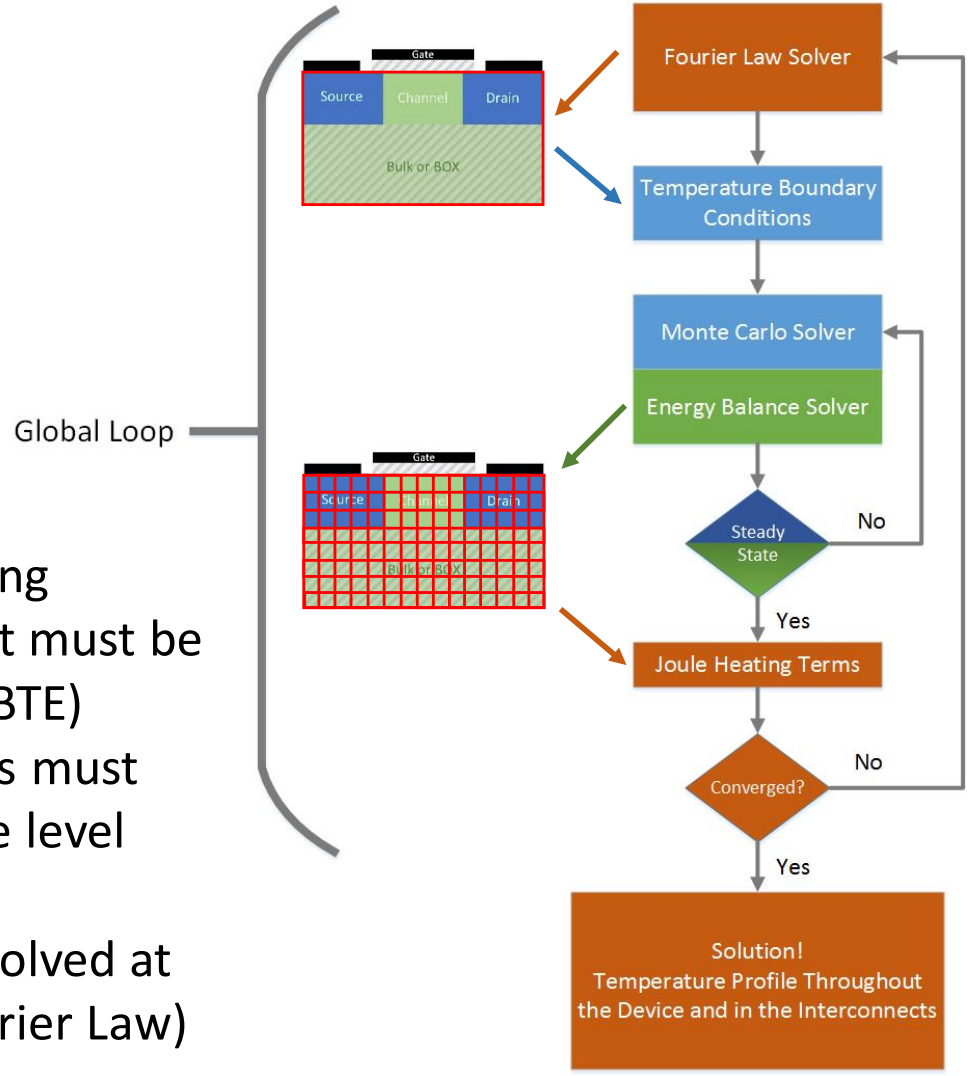
Multiscale Modeling: Flow-chart of Global Loop Solver

Carrier Mean Free Path:
Electrons: O(5nm)
Holes: O(2nm)

Phonon Mean Free Path:
Optical: O(>1nm)
Acoustic: O(300nm)

Reasons for Multiscale Modeling

- ❑ Electron and Hole transport must be solved at the device level (BTE)
- ❑ Optical phonon interactions must also be solved at the device level (Energy Balance Equations)
- ❑ Thermal transport can be solved at the interconnect level (Fourier Law)



Experimental Methods: Determining the Temperature

1. Thermoreflectance Method[1,2]

Emphasis on **average** temperature

2. IMEC Heater Sensor Approach[3]

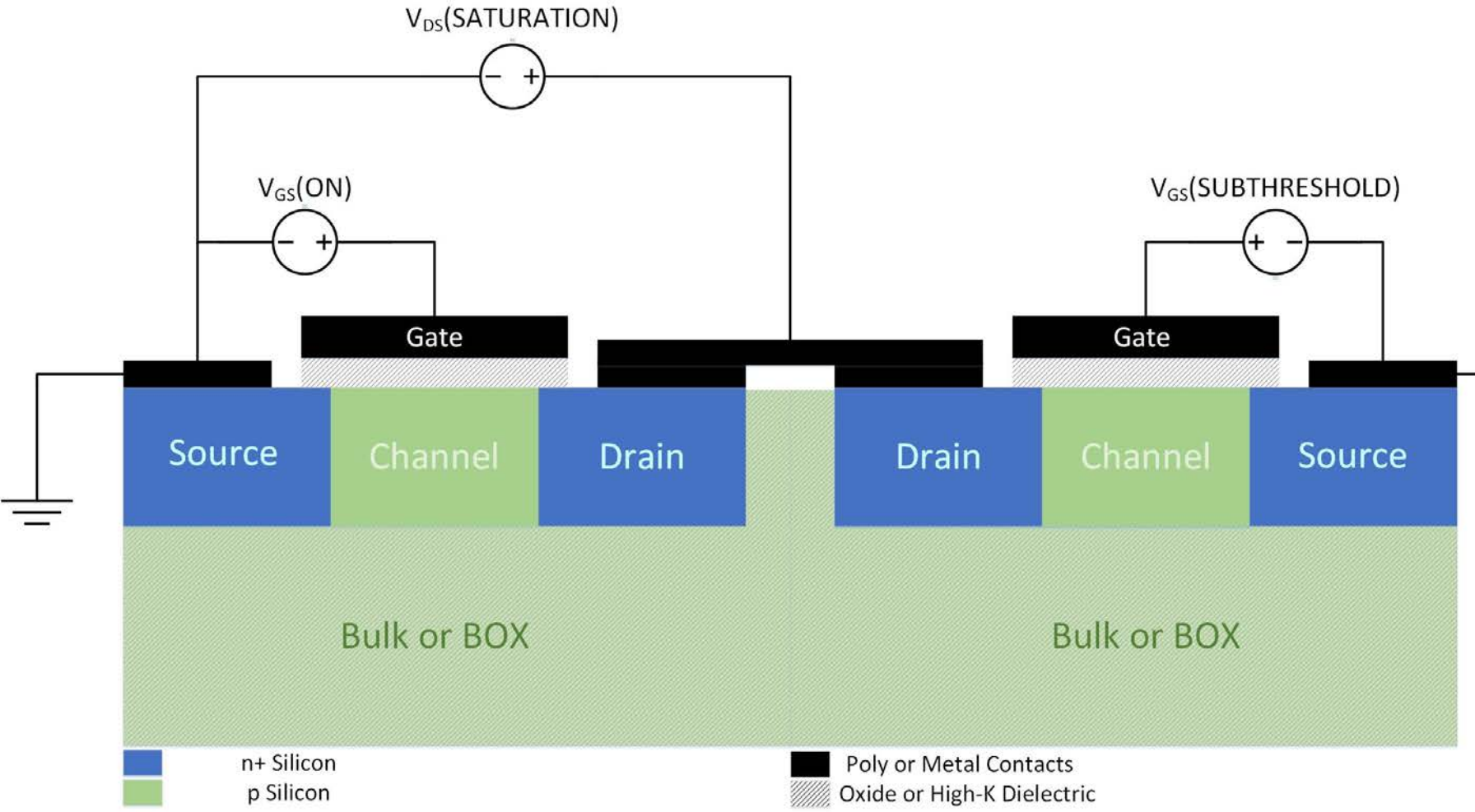
Emphasis on **hot spot** temperature

1. Nanoscale thermal transport. II. 2003–2012, David G. Cahill, Paul V. Braun, Gang Chen, David R. Clarke, Shanhui Fan, Kenneth E. Goodson, Pawel Keblinski, William P. King, Gerald D. Mahan, Arun Majumdar, Humphrey J. Maris, Simon R. Phillpot, Eric Pop, and Li Shi, Applied Physics Reviews 1, 011305 (2014)

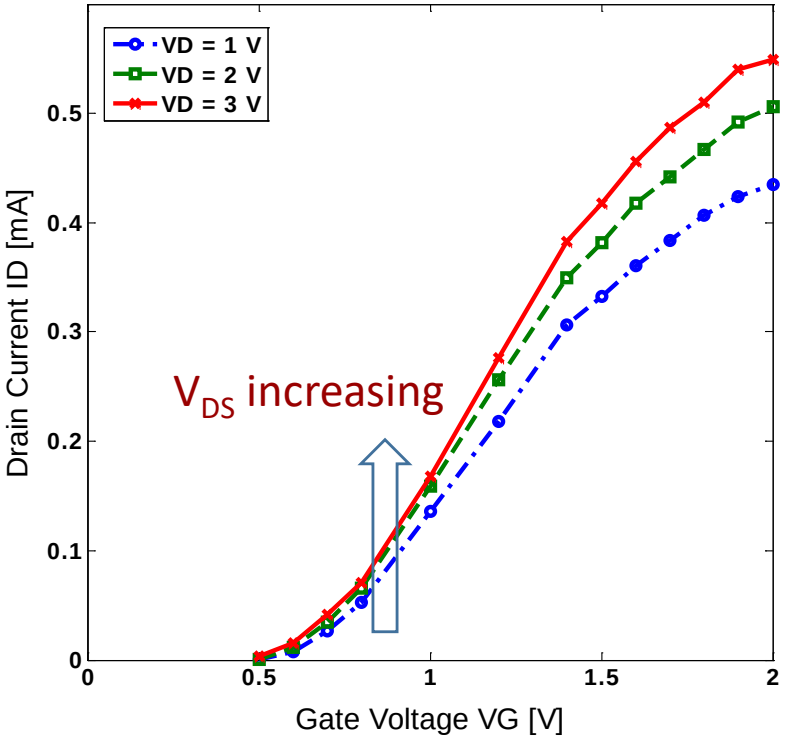
2. Bias-dependent MOS transistor thermal resistance and non-uniform self-heating temperature, Xi Wang, Younes Ezzahri, James Christofferson and Ali Shakouri, J. Phys. D: Appl. Phys. 42 (2009)

3. Uncovering the temperature of the hotspot in nanoscale devices, Katerina Raleva, Erik Bury, Ben Kaczer and Dragica Vasileska, Computational Electronics (IWCE), 2014 International Workshop on , vol., no., pp.1-3, 3-6 June 2014

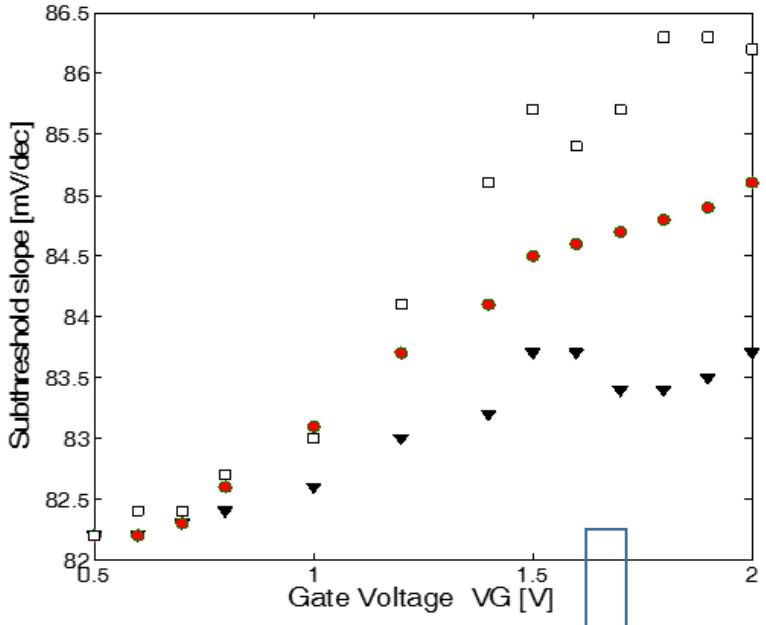
Experimental/Simulation Set-Up



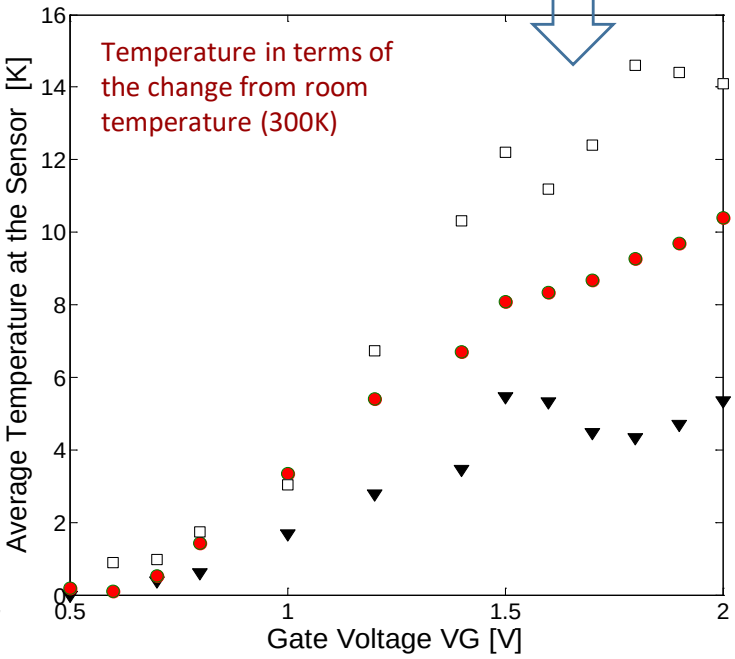
Experimental Data



Sensor Transfer Characteristics



EKV Model

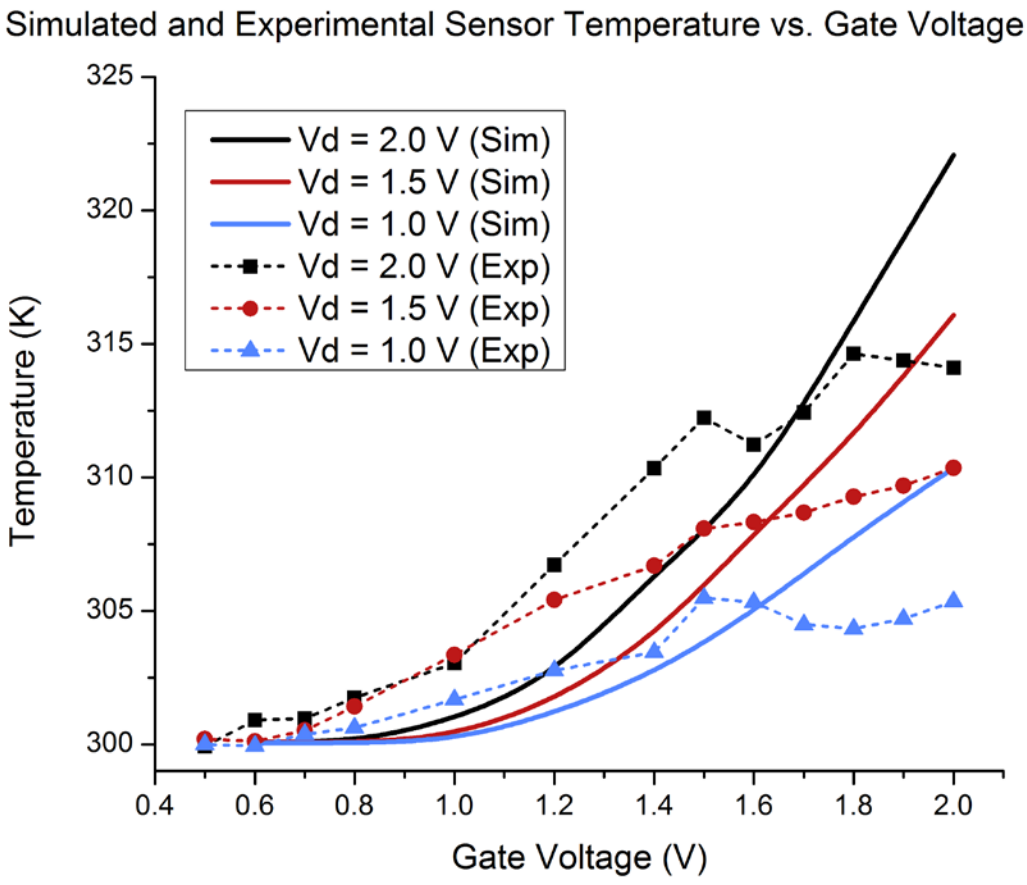


C. C. Enz, F. Krummenacher and E. A. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications", *Analog Integrated Circuits and Signal Processing*, **8**, pp.83-114 (1995)

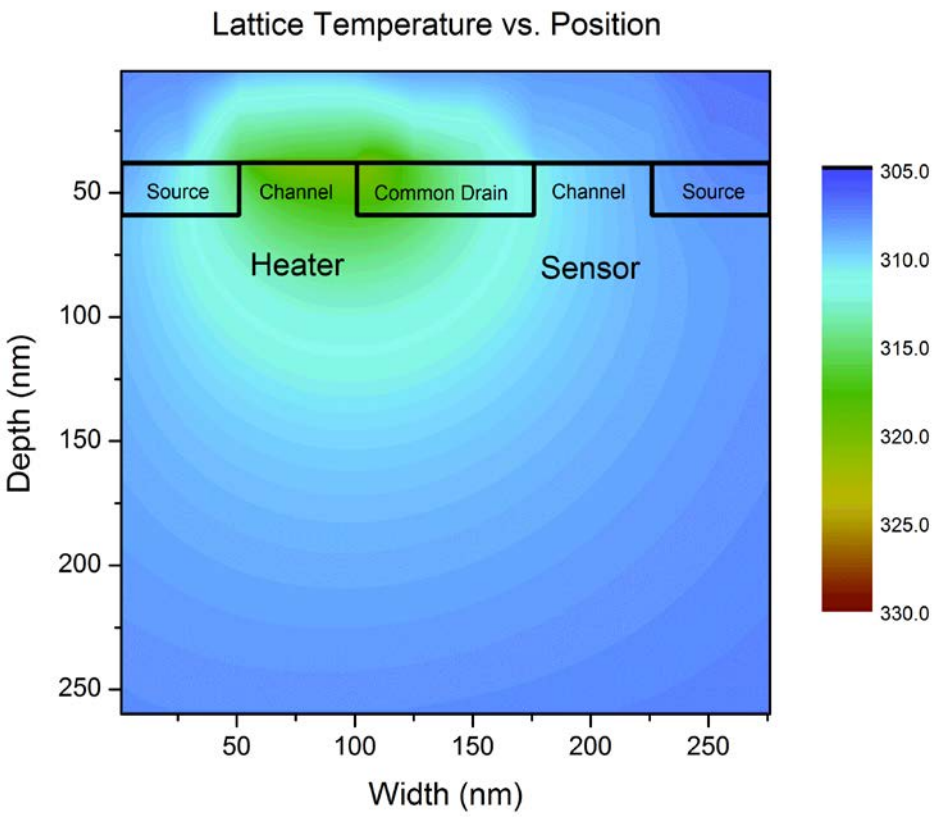
Results:
Temperature in the Subthreshold Device

Temperature cannot be measured directly in the **active** device!

- ❑ Temperature is measured in the adjacent subthreshold device using the EKG method
- ❑ Simulated temperature profile in the sensor is consistent with the measured temperature
- ❑ We can reasonably infer that our simulated temperature profile in the active device is consistent with reality

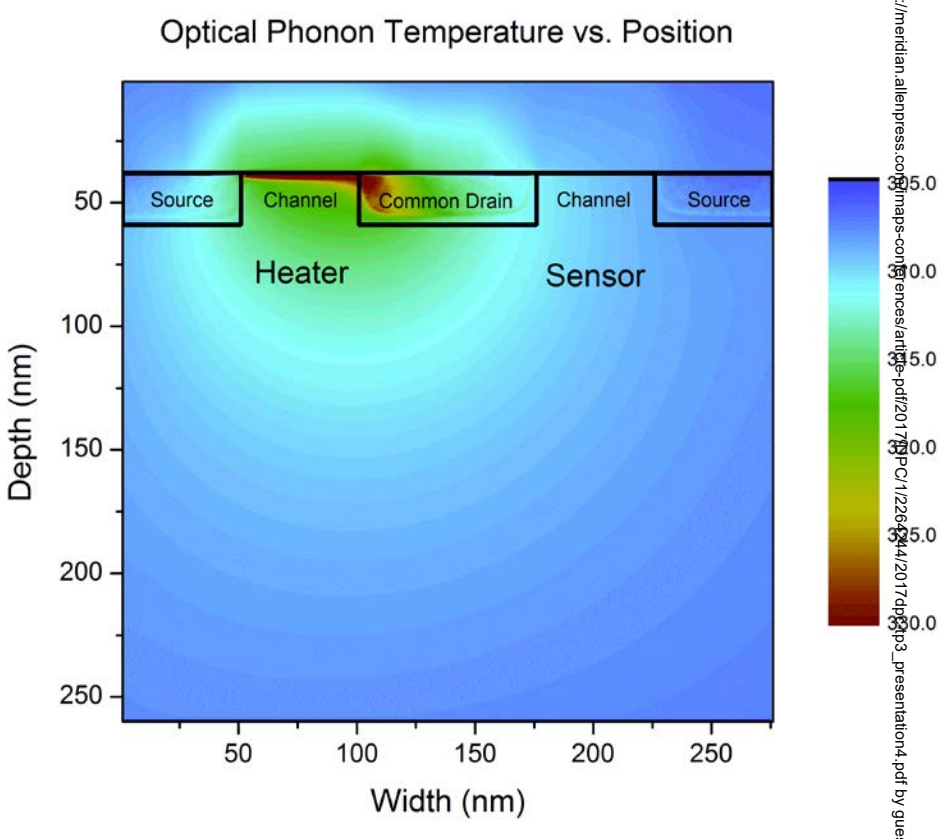


Results: Temperature Profile Using Multiscale Electro-Thermal Simulation



Global Lattice Temperature Profile

Max Temperature = 320.49K



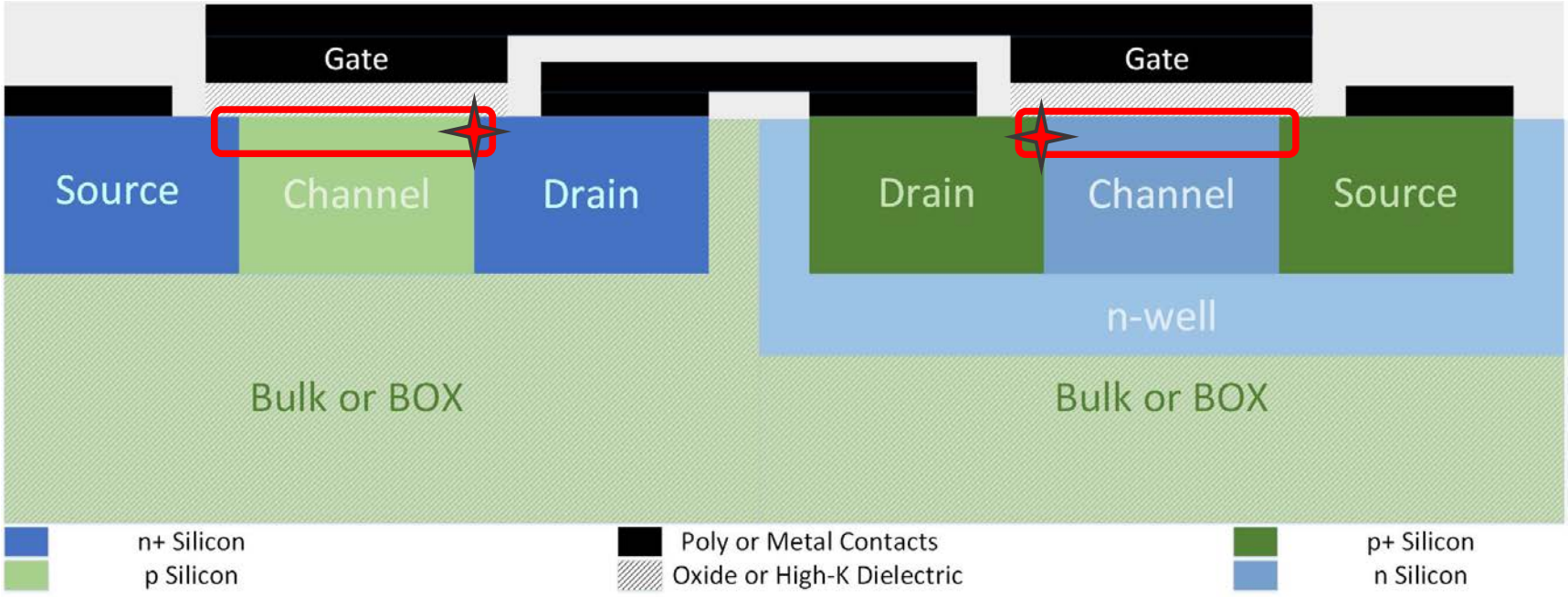
Global Optical Phonon Temperature Profile

Max Temperature = 356.42K

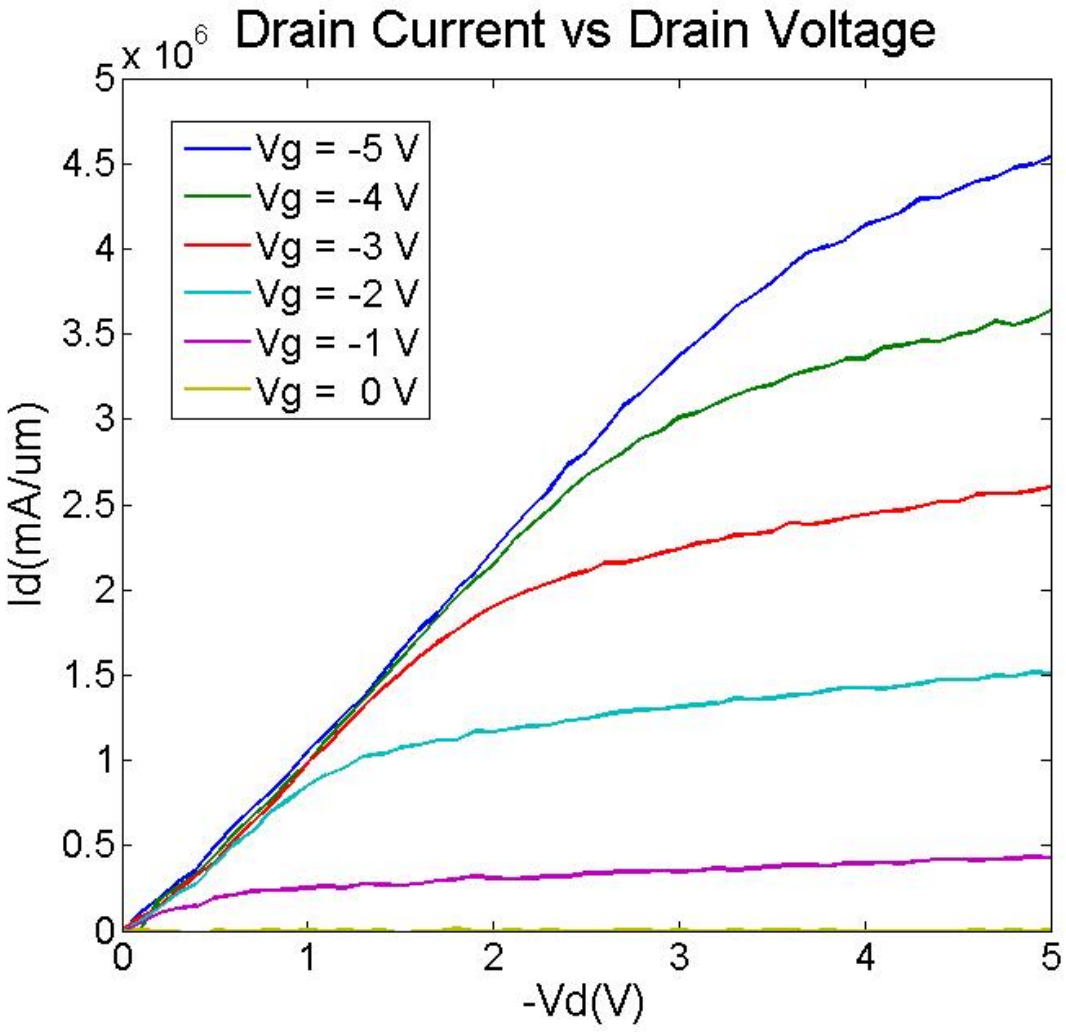
V_{GS}(ON) = 1.6 V V_{DS}(SATURATION) = 1.5 V V_{GS}(SUBTHRESHOLD) = 0.3 V

Why CMOS Modeling?

- Physical interaction between closely spaced and inter-connected devices in CMOS circuits can be better understood by modeling both NMOS and PMOS devices simultaneously



Results: PMOS I-V Characteristics



I-V curves for the simulated PMOS transistor show the characteristic behavior for cutoff, triode, and saturation

This hole Monte Carlo based PMOS device solver is ready to be coupled with the electron Monte Carlo NMOS device solver

An electron-hole Monte Carlo solver will be able to simultaneously solve for NMOS and PMOS devices (i.e. CMOS circuits)

Future Work

- Fully coupled electron *and* hole Monte Carlo solver
- Self consistent solution for individual NMOS and PMOS devices using electron/hole Monte Carlo solver
- Two Methods of Multiscale solution for CMOS simulations
  1. Fully self-consistent solution using electron/hole Monte Carlo solver for CMOS circuits
     - Some circuit behavior simulated at the device level
     - Current continuity maintained with injection and extraction
     - Multiscale approach for thermal transport in interconnects
  2. Multiscale solution using electron/hole Monte Carlo individually for NMOS and PMOS
     - All circuit behavior simulated using multiscale approach
     - Current continuity maintained with bias conditions
     - Multiscale approach for thermal transport in interconnects

Conclusions

- A multiscale simulator has been developed to model adjacent MOSFET devices and circuit level interconnects
- The electro-thermal solver solves the BTE for carriers (electrons/holes*) and the energy balance equations for phonons (optical and acoustic)
  - The coupled solver accurately calculates the lattice temperature in the device
  - Temperature BCs are required (previously assumed to be room temperature)
- The Fourier Law for thermal transport is used to find the temperature in the circuit and obtain boundary conditions for the device simulator
  - Fourier Law itself *underestimates* lattice temperature in the device
  - Sufficient for finding temperature boundary conditions in the circuit
- A hole* Monte Carlo solver has been developed in order to simulate PMOS devices; this will be coupled with the multiscale approach
- This multiscale approach can be used to simulate CMOS circuits at the device level and circuit/interconnect level self-consistently

Thank You

Robin Daugherty
Arizona State University
Tempe, AZ
rldaughe@asu.edu