IMAPS Device Packaging Conference 2017

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Precision Surface Processing

Wafer Thinning for Advanced Packaging Applications

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Outline

- Background
- Silicon Etching
  - Wafer Thinning
  - TSV Reveal
  - FOWLP
- Process Description
- Summary

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STACKED POTATO CRISPS

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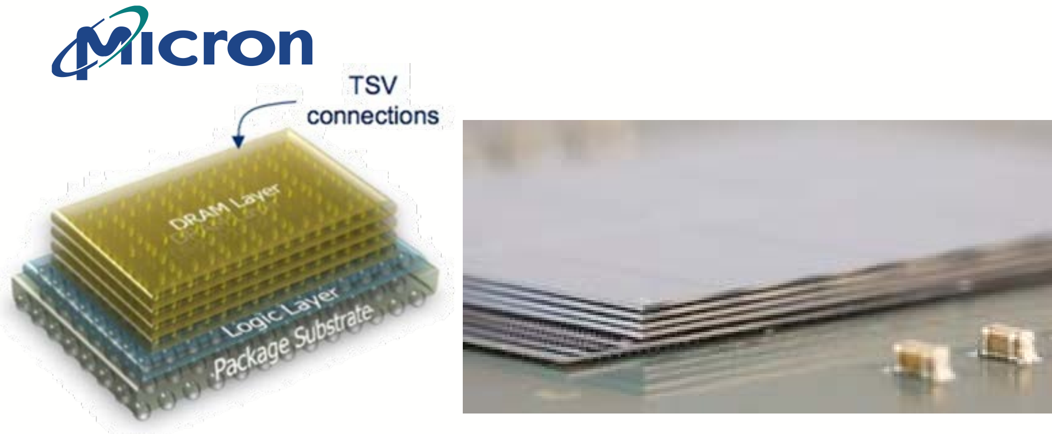
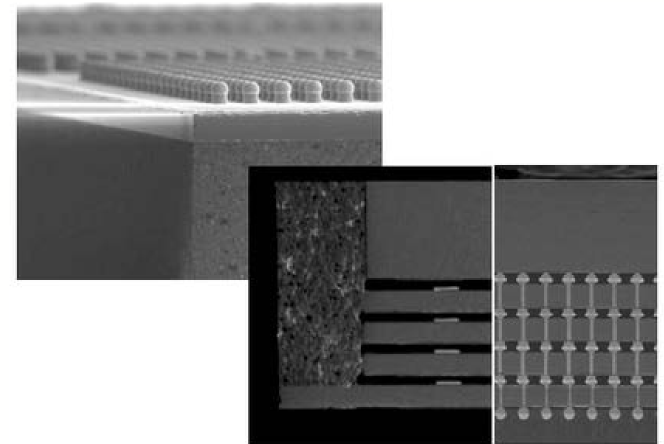
3D High Performance Devices require TSV

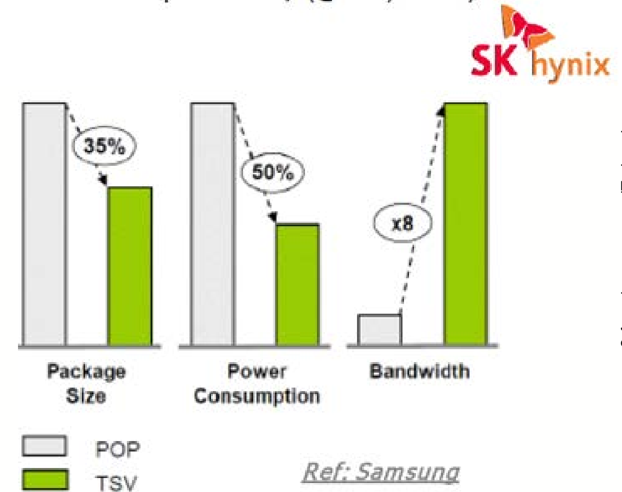
Hybrid Memory Cube (HMC)



High Bandwidth Memory (HBM)

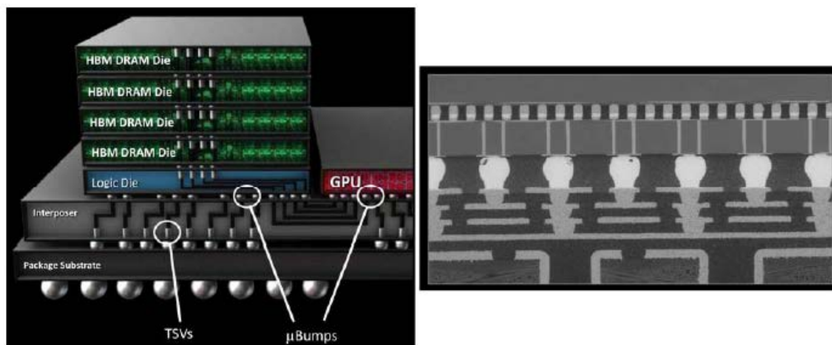


1GB HBM up to 128GB/s(@1.2V, x1024)



High End Graphics

Figure 2.1. AMD's Fiji with silicon interposer and HBM.



Source: AMD.

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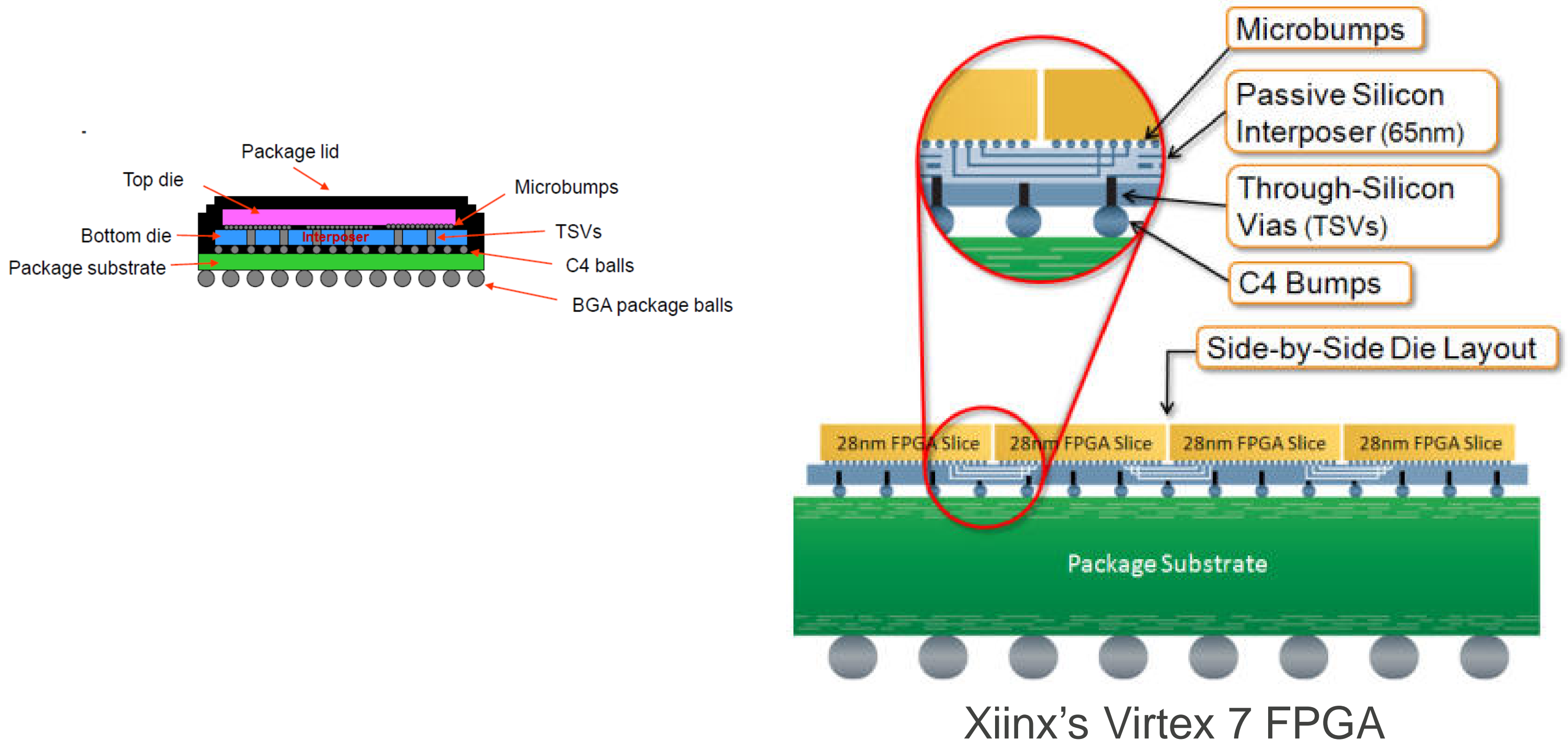
2.5D Interposers

A configuration where dies are mounted side by side on one side of a thin (~ 100 um) silicon, glass, or organic interposer using through silicon vias (TSVs), through glass vias (TGV) or through substrate vias (TSV), respectively through the interposer to connect the dies with the package substrate.



Xiinx's Virtex 7 FPGA

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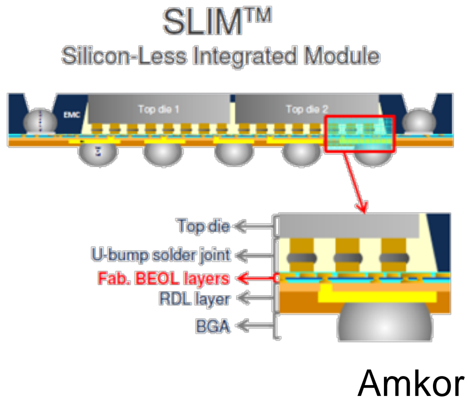
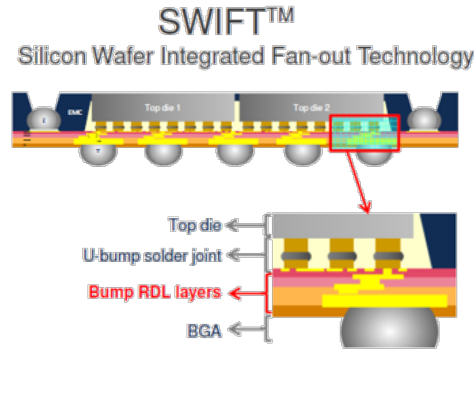
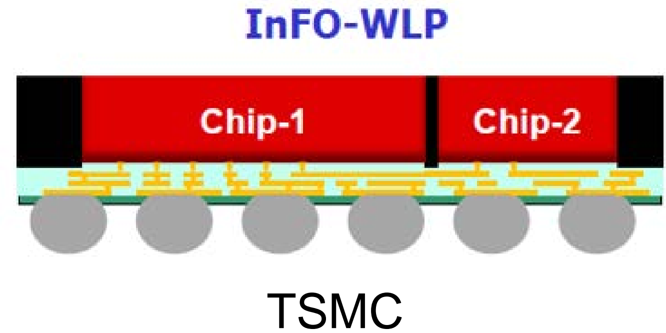
Technologies for Advanced Packaging

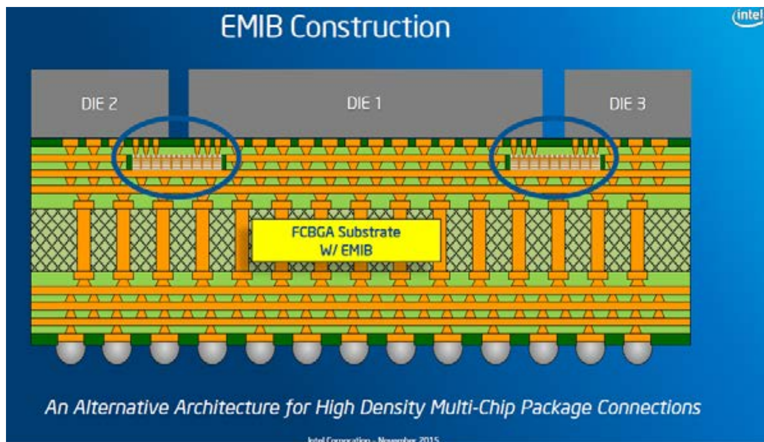




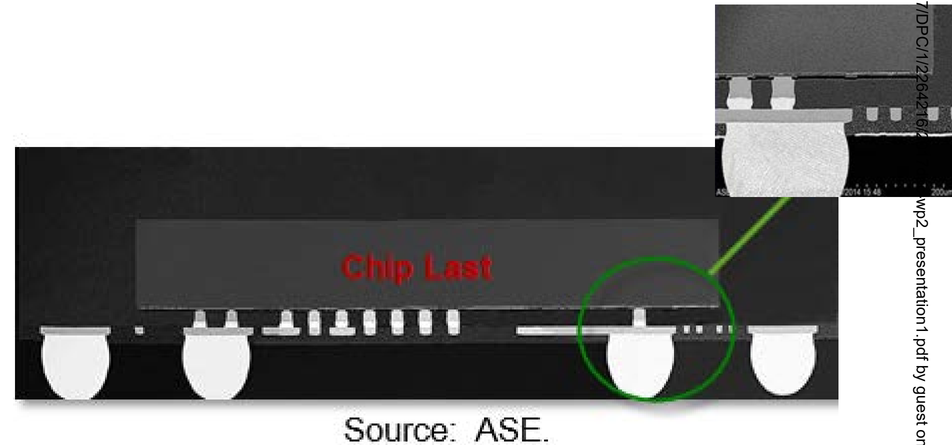
Amkor



TSMC



Intel



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Thickness Trends

➢ Smaller form factor requires thinner devices and packages

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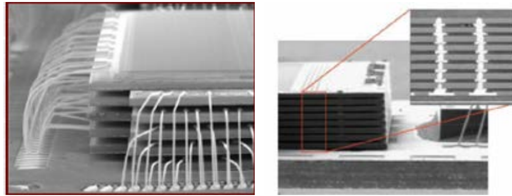
Wafer Thinning for Many Applications

Memory and Logic

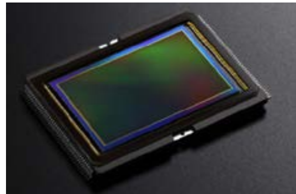


Thinner chips are needed for stacking by either wire bond or TSV

MEMS

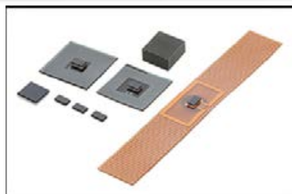
MEMS devices contain a sensor element, a cap and an ASIC. All three wafers must be thinned to achieve size reduction of the packaged device

CMOS Image Sensor



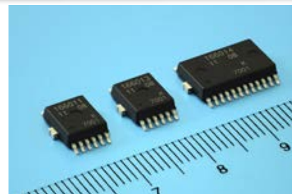
CMOS images sensors are thinned for via last TSV process and very small form factor. Backside illumination with extreme thinning to < 10µm for enhanced sensitivity

RF ID Devices



RF device wafers are thinned to improve form factor and enable very thin packages

Power Devices



Thin wafers are needed to improve current carrying capability, lower R_{on} and minimize power consumption. 60-70µm in production for IGBTs and Power MOSFETs

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Wafer Thinning – General Requirements

- Bulk of silicon is removed by Grinding
- Need to remove subsurface damage and residual stress in the wafer that results from the grinding process
- Smoothing of surface to eliminate grind marks
- Low cost of ownership

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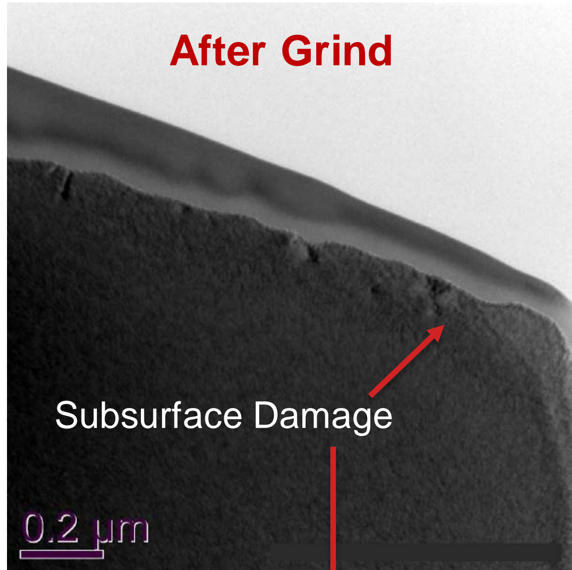
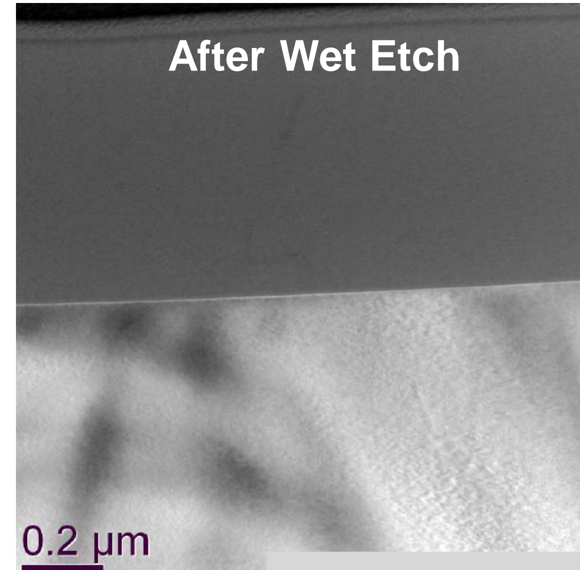
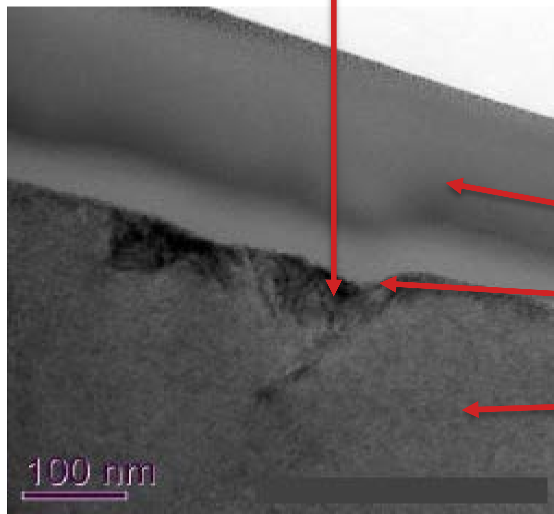
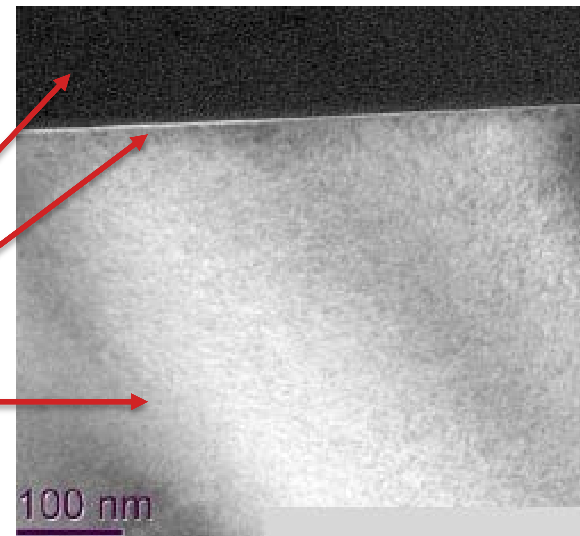
Wet Etch to Relieve Stress and Eliminate Subsurface Damage

TEM Images









TEM Protection Layer

Silicon Surface

Silicon Wafer

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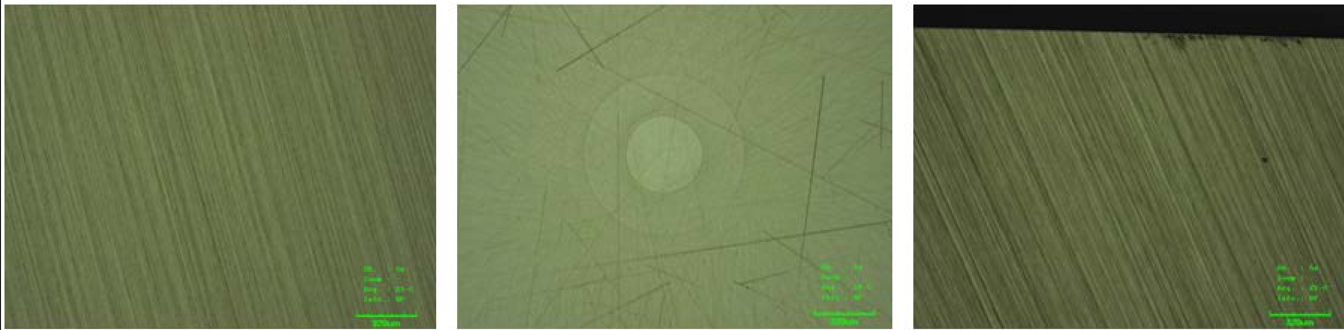
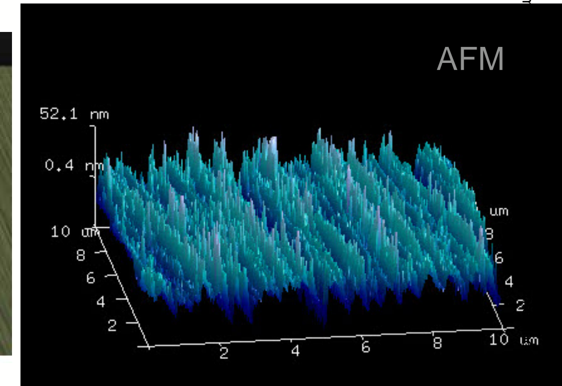
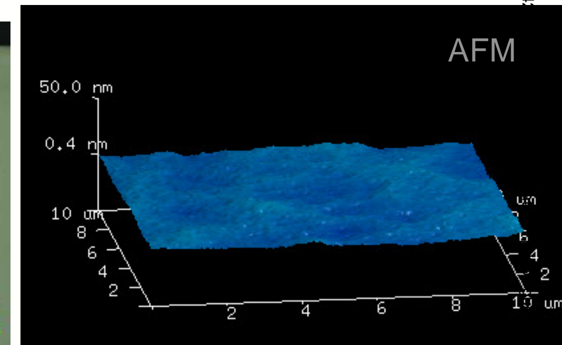
Surface Roughness - Reduced by Wet Etch





Post Grind



Post Wet Etch

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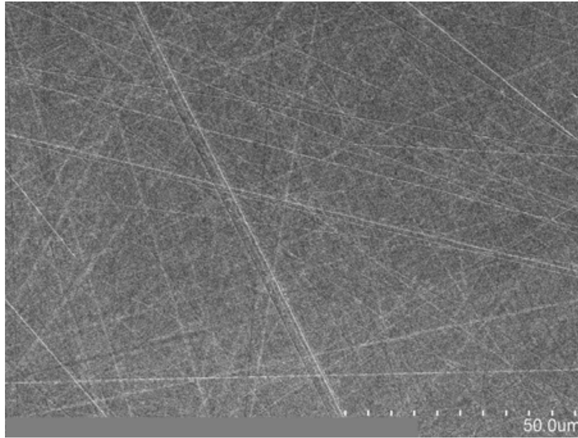
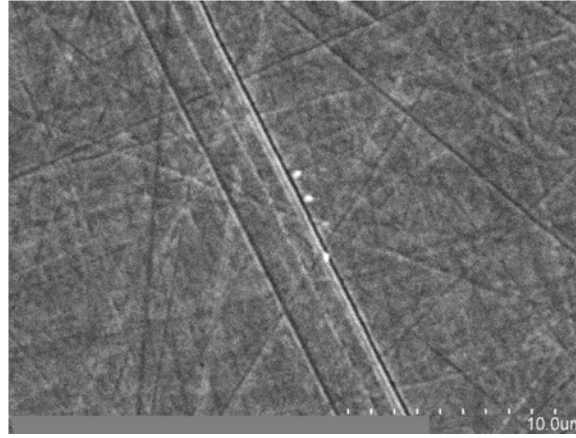
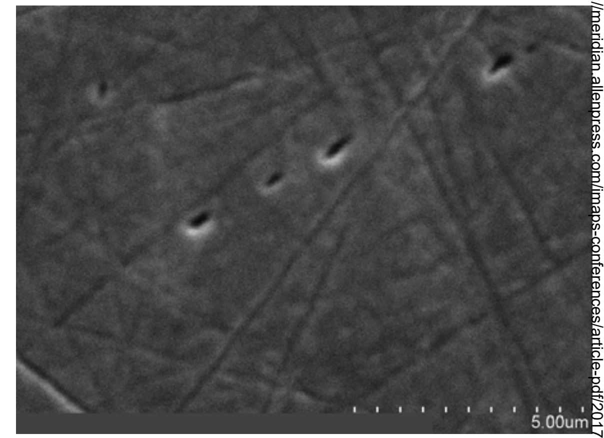
Wet Etch Smoothes Surface and Eliminates Need for CMP

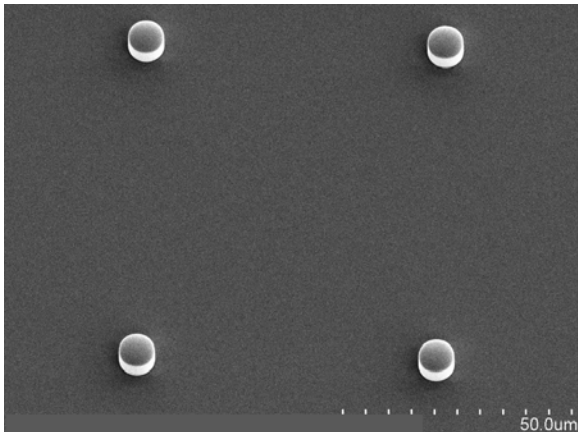
> PRE – Grind Marks

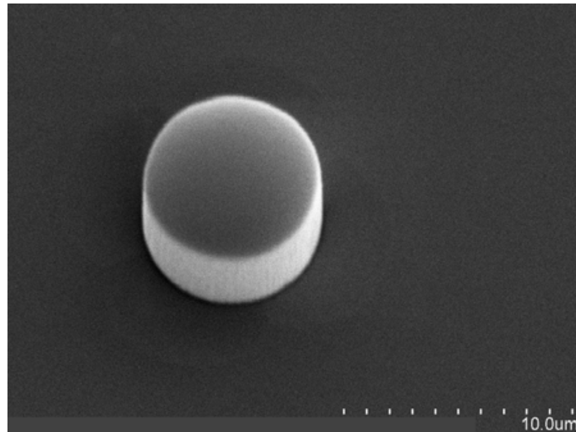


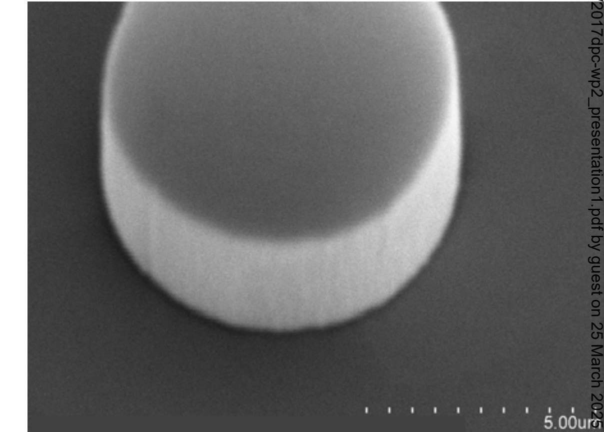




> Post wet etch – smooth surface







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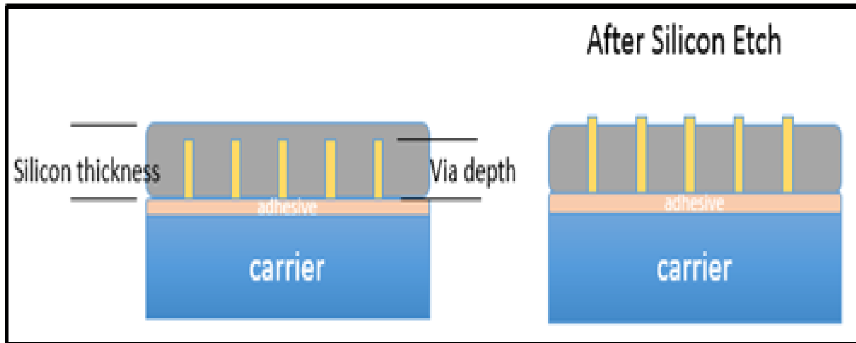
Requirements for other Wafer Thinning Applications

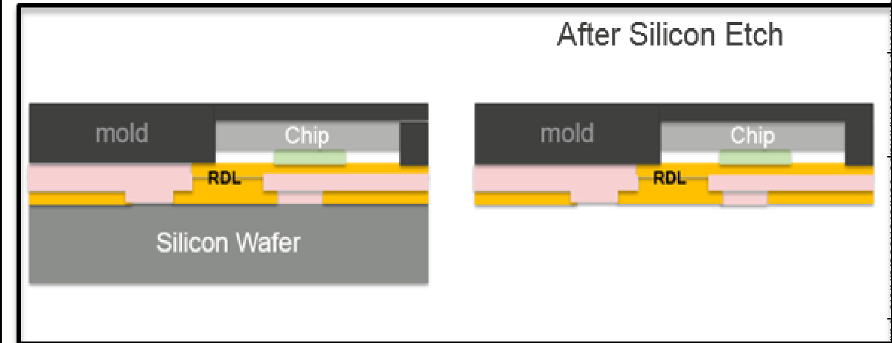
TSV Reveal



Si Etch for TSV Reveal:

- No etch of SiO2 liner or Cu TSV
- Fast Si etch rate
- Smooth surface finishing
- Good etch uniformity
- Cost effective

FOWLP



Si Etch for FOWLP:

- Compatible with materials present in package structure such as Cu, Ti/TiW, SiO2, Si3N4, PI, and PBO
- Fast Si etch rate
- Good etch uniformity
- Cost effective

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Silicon Wet Etch Options

- KOH (Potassium Hydroxide)
  - Good etch rate and selectivity (Silicon to Oxides /Cu)
  - Ionic contamination (K+)
- TMAH (Tetramethyl Ammonium Hydroxide)
  - Safety concerns (toxicity) at high concentration
  - Slow etch rate
- HF / Nitric based chemistry – "Spinetch"
  - High etch rates but poor selectivity (Silicon to Oxides /Cu)
- SACHEM Reveal Etch™
  - Lower toxicity than TMAH
  - Higher etch rate and good selectivity (Silicon to Oxides /Cu)

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Etch Selectivity

> Ability to etch silicon and stop on a variety of materials without causing damage

HF/Nitric Mixture*		
Material	Etch Rate (nm/min)	Selectivity to Silicon
Si	9000	
SiO2	50	180
Si3N4	2.7	3333
Cu	2400	3.8
Ti	750	12
TiW	144	63
PI	0	>10000
PBO	0	>10000

SACHEM Reveal Etch™		
Material	Etch Rate (nm/min)	Selectivity to Silicon
Si	711	
SiO2	0.5	1422
Si3N4	0	> 10000
Cu	12	59
Ti	0	>10000
TiW	1.9	374
PI	5.6	95
PBO	7.5	126

SACHEM ST2011		
Material	Etch Rate (nm/min)	Selectivity to Silicon
Si	150	
SiO2	0.5	300
Si3N4	0	>10000
Cu	0	>10000
Ti	0	>10000
TiW	0	>10000
PI	0	>10000
PBO	0	>10000

* Spinetch D 1:6:2:1 HF:Nitric:Phosphoric:Sulfuric

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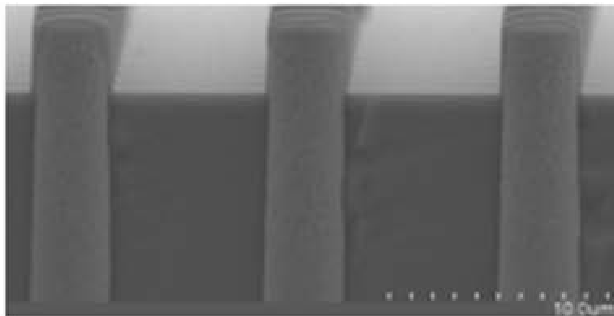
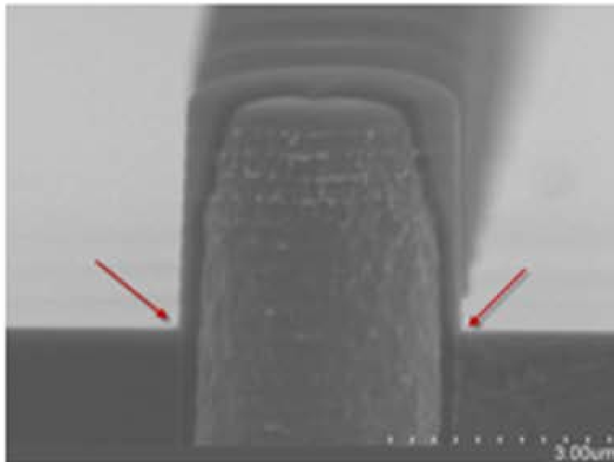
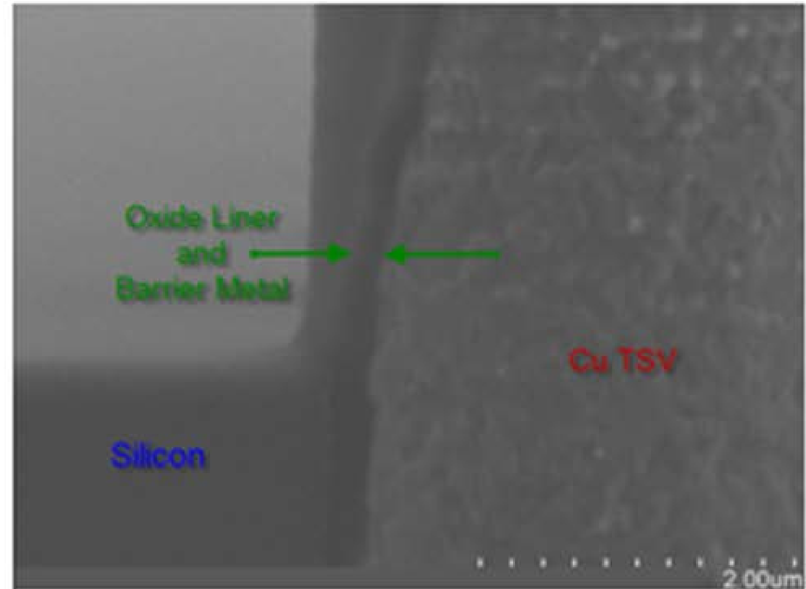
Integrity of Via and Oxide Liner







- No attack of oxide liner
- No preferential attack along sidewall

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Two-Step Etch Process Developed

- Step 1
  - Spinetch D (HF / Nitric mixture)
    - To smooth surface and eliminate grind marks
    - Contour silicon thickness for improved uniformity
- Step 2
  - SACHEM Reveal Etch™
    - Selective etch of silicon
      - TSV oxide liner and Cu via
      - Other materials present at end of silicon etch for FOWLP

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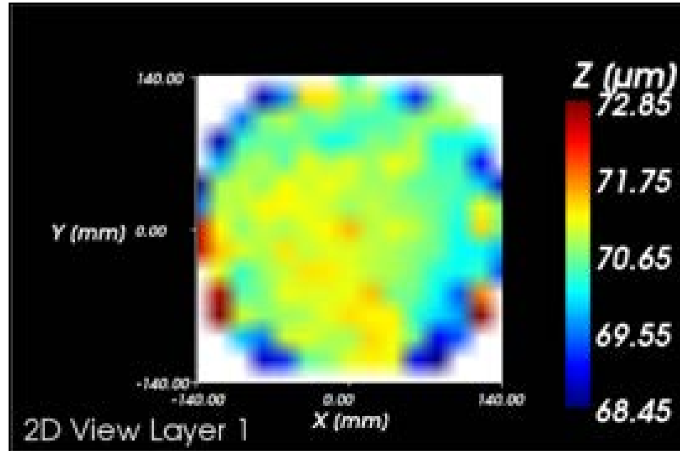
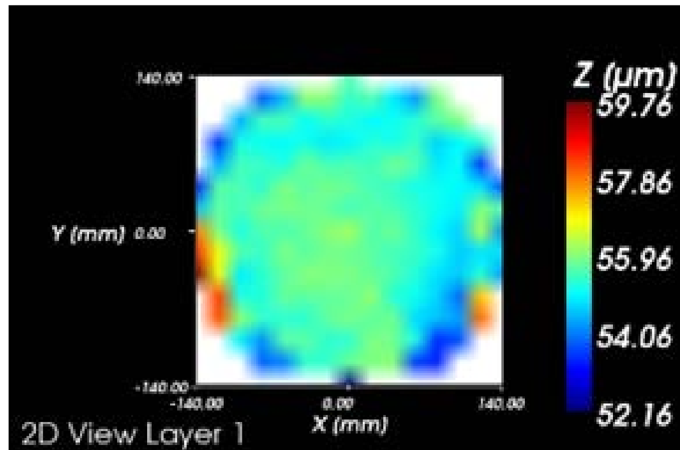
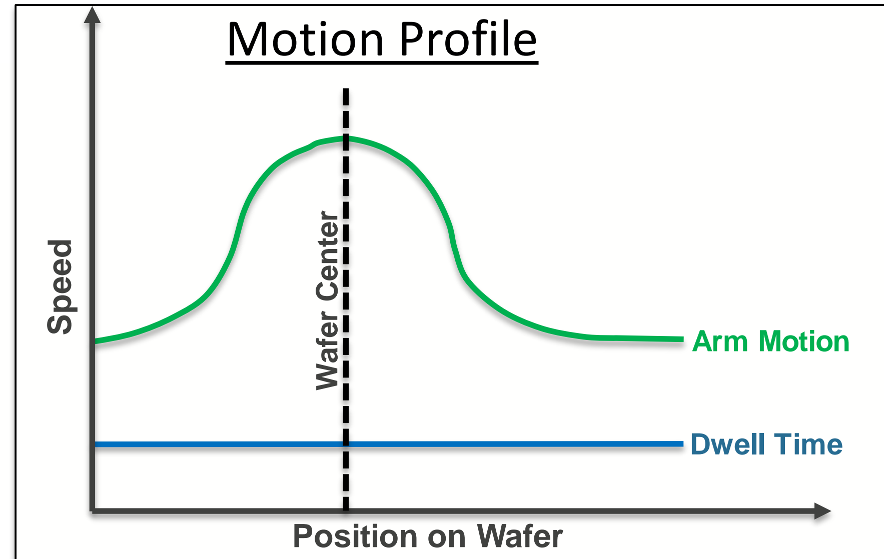
Hyperbolic Motion Profile

Post Grind



Post Silicon Etch





- **Post Grind non-uniformities can have radial dependence**
  - Center to edge variations
- **Single wafer etch process can compensate for radial non-uniformities**
  - More/Less etch in center of wafer
- **Resulting Silicon wafer thickness is more uniform**

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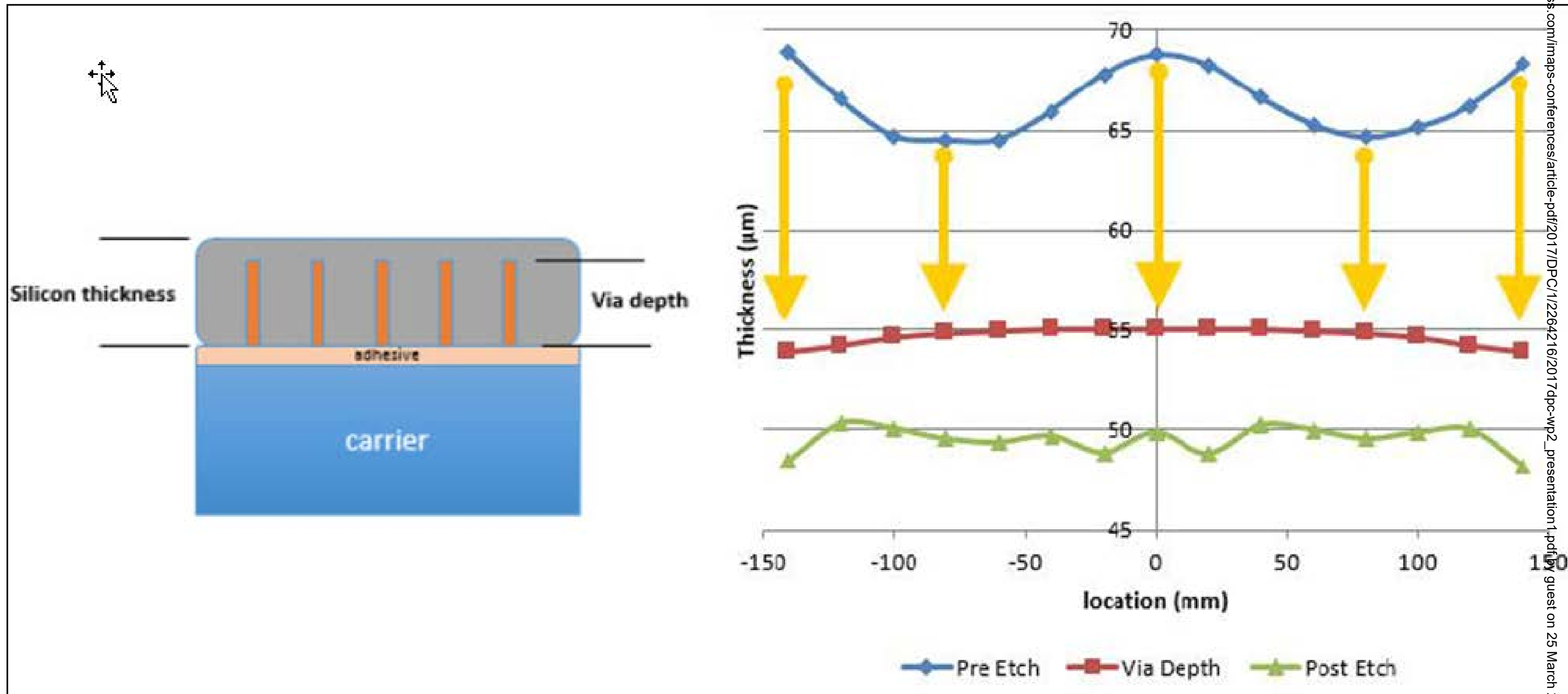
PMT - Profile Match Technology™

- Measure Silicon thickness across wafer
- Calculate desired etch profile



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Integrated Wafer Thickness Measurement System

> Wafer aligned for repeatable thickness measurements

> Radial measurements

> Measurements performed before and after etch to track uniformity and etch rate

→Process Control

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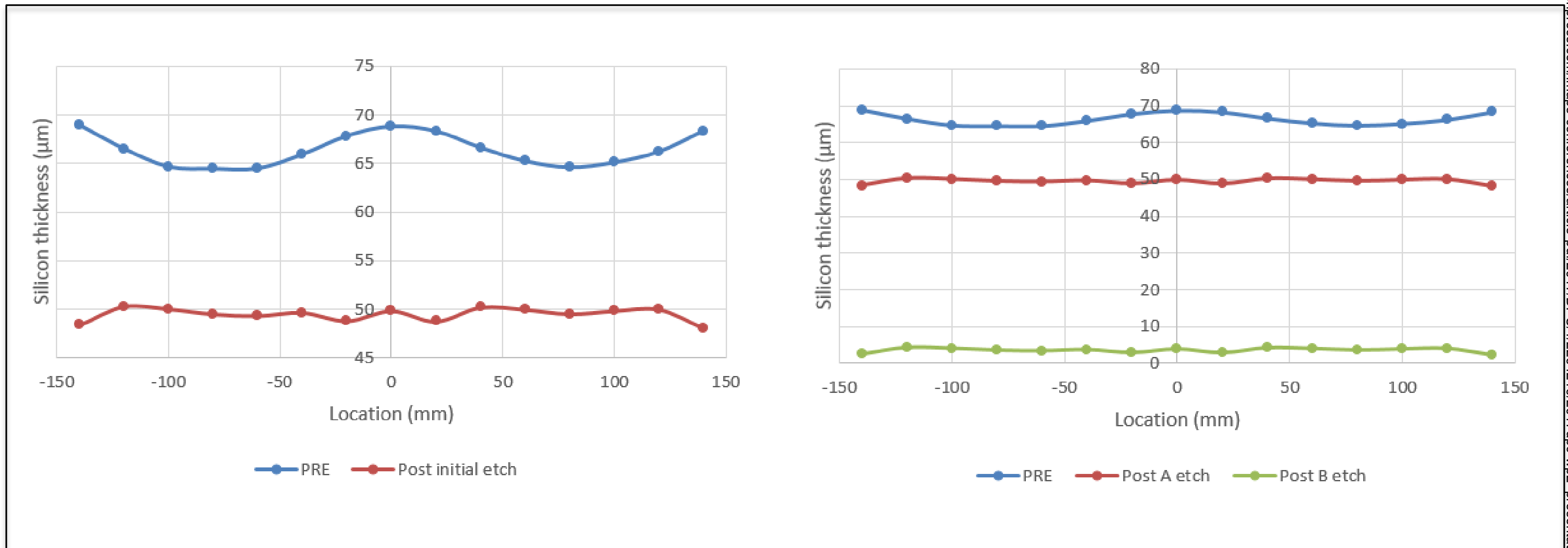
Profile Match Technology for FOWLP Applications

- Need to improve uniformity of silicon thickness to minimize etch or damage to underlying materials and structures



- Silicon will be completely removed after final etch

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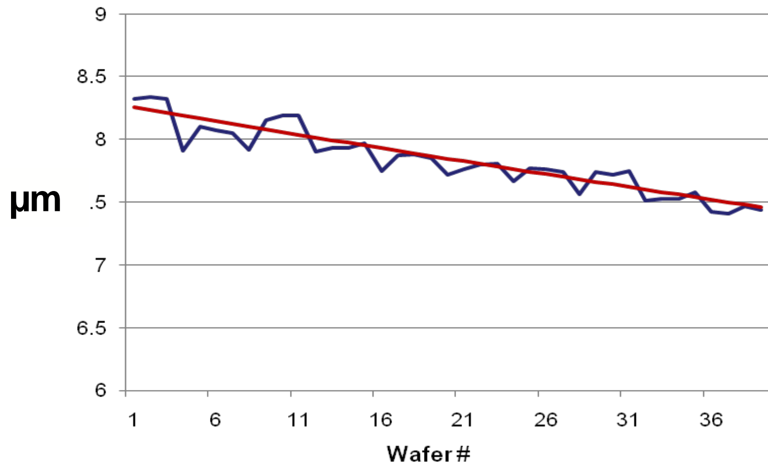
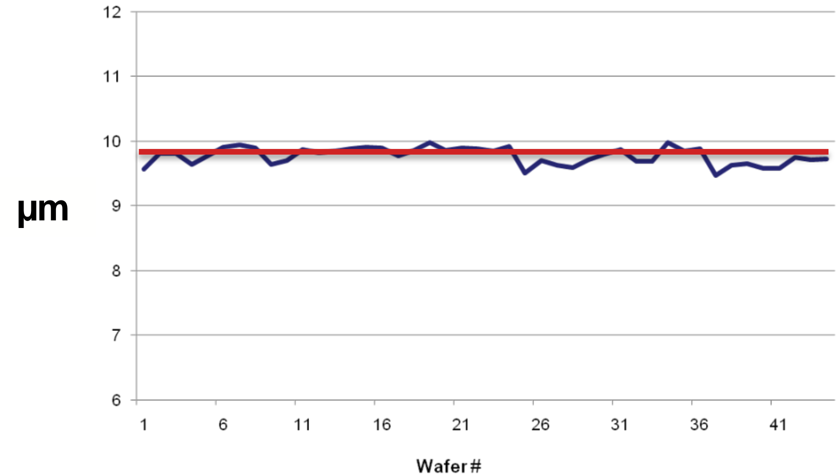
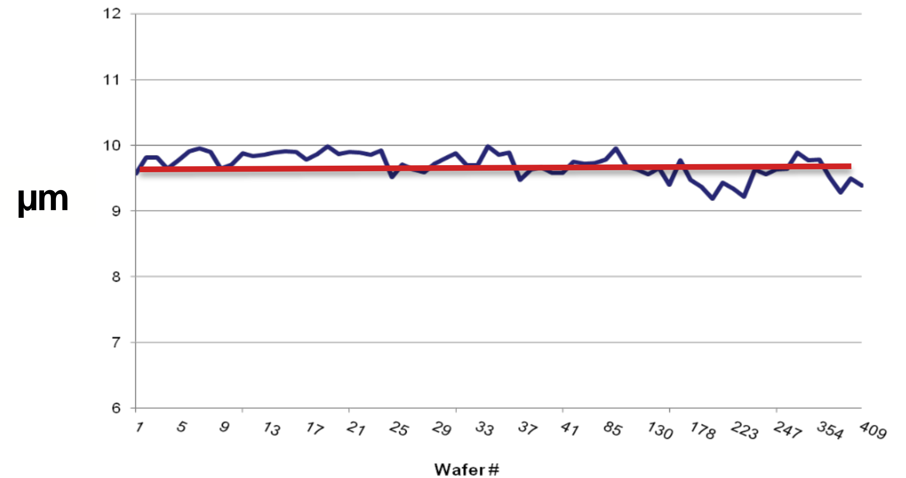
Consistent Etch Rates with Adaptive Spiking







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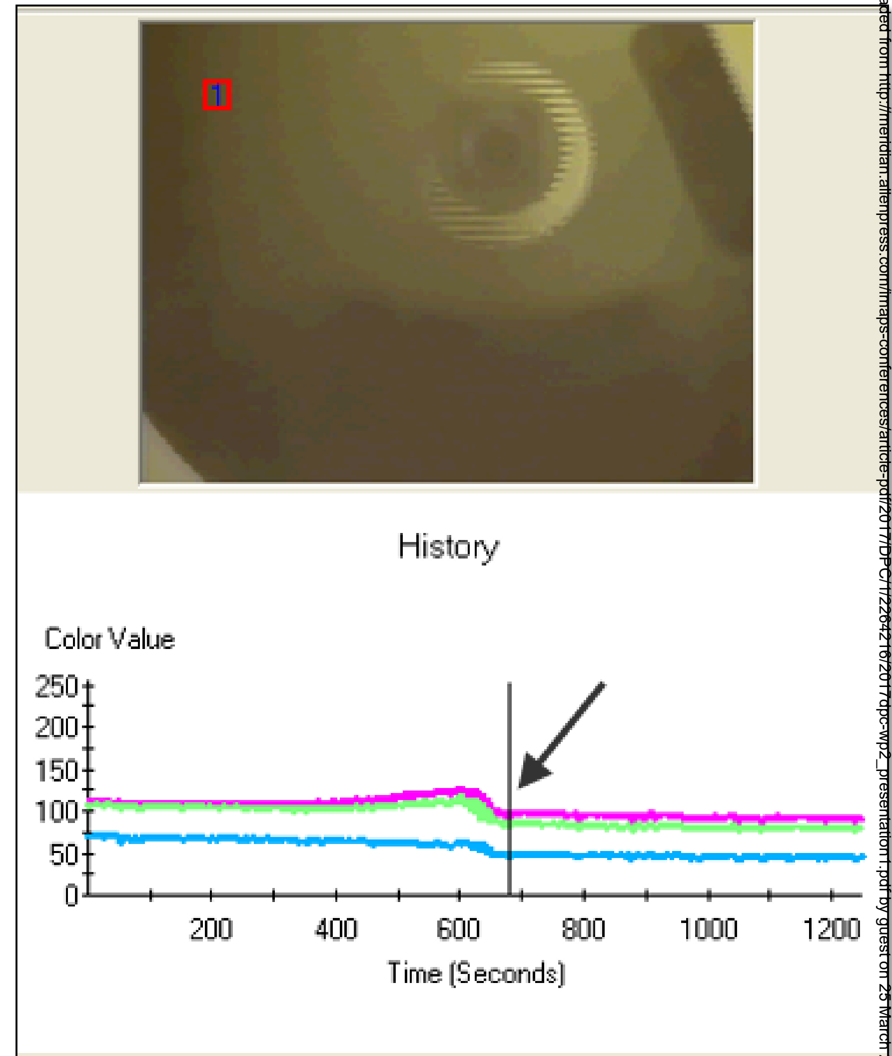
WaferChek® Process Monitor for FOWLP Si Etch

- Endpoint detection for Si etch on FOWLP wafers
  - Detects end of process by monitoring color changes in substrate as silicon is removed



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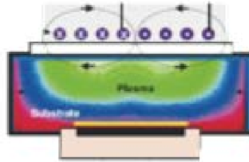
One Tool Process - Lowest cost of Ownership

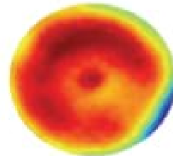
Process of Record
Requires 4 tools

CMP

Plasma Etch



Silicon Thickness Measurement



Cleaning Tool

WaferEtch®
Single Tool Solution

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Summary and Conclusions

- Wet silicon etch process that is applicable to many advanced packaging applications
  - Wafer Thinning
  - TSV Reveal
  - FOWLP
- High selectivity of the silicon etch relative to the other materials that are present in the package structure
- Endpoint Detection for FOWLP applications

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