Speed and Accuracy Optimization for Fan-Out Die Placement

Device Packaging Conference 2017

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Agenda

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- Overview
- Market growth information
- Fan-out process Main Process Flows
- Panel Implementation
- Global vs Local and Combo Alignment
- Die Placement by Process Flow
  - eWLB
  - InFO
  - SWIFT
- Conclusions

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Fan-Out Landscape for Die Placement

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Process Flow Attributes and Challenges

- Die placement face-up or face-down
- Alignment schemes include global alignment, local alignment or a combination of both methods
- Heat or Force may be required during die placement

Accuracy

- Steppers are typically used with the assumption die to die spacing is repeatable within a given field area
- Die placement accuracy in conjunction with die shift from the reconstitution process must accommodate the design rules for RDL via size, passivation opening size and pad pitch for the intended devices
- Die spacing will be somewhat irregular due normal process variation in placement and reconstitution

Cost Implications

- Die placement speed is directly related to cost and the highest UPH is preferred
- Accuracy is directly related to yield and the subsequent cost for advanced products
- Die placement equipment optimized for the best accuracy may not have the highest UPH

Critical factors influence die placement accuracy and UPH for each of the three standard flows

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Competing Fan-Out Process Options

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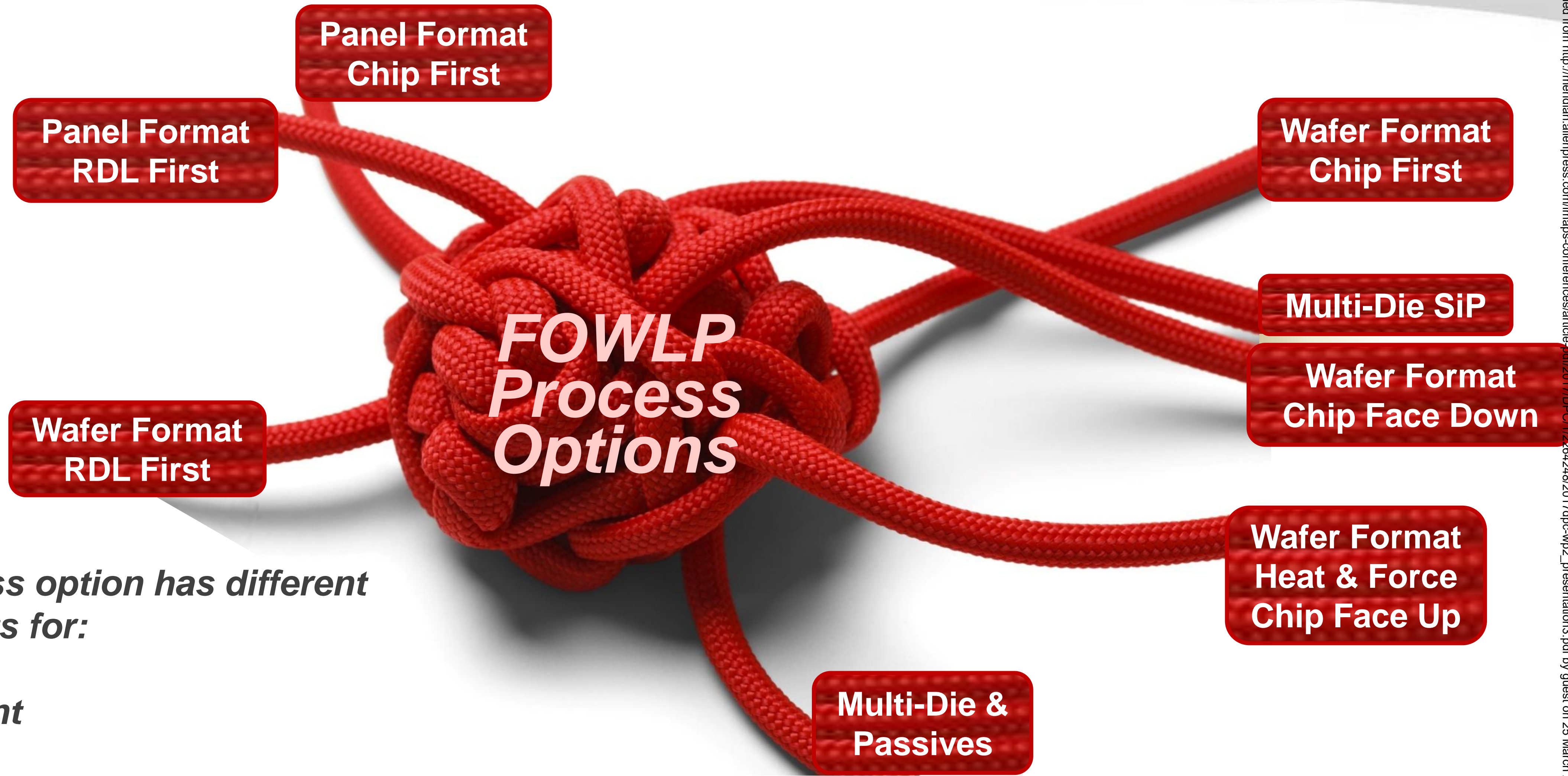

Each process option has different requirements for:

- *Materials*
- *Equipment*
- *Cost*
- *Accuracy*

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FO-WLP Process Flow Options and Requirements

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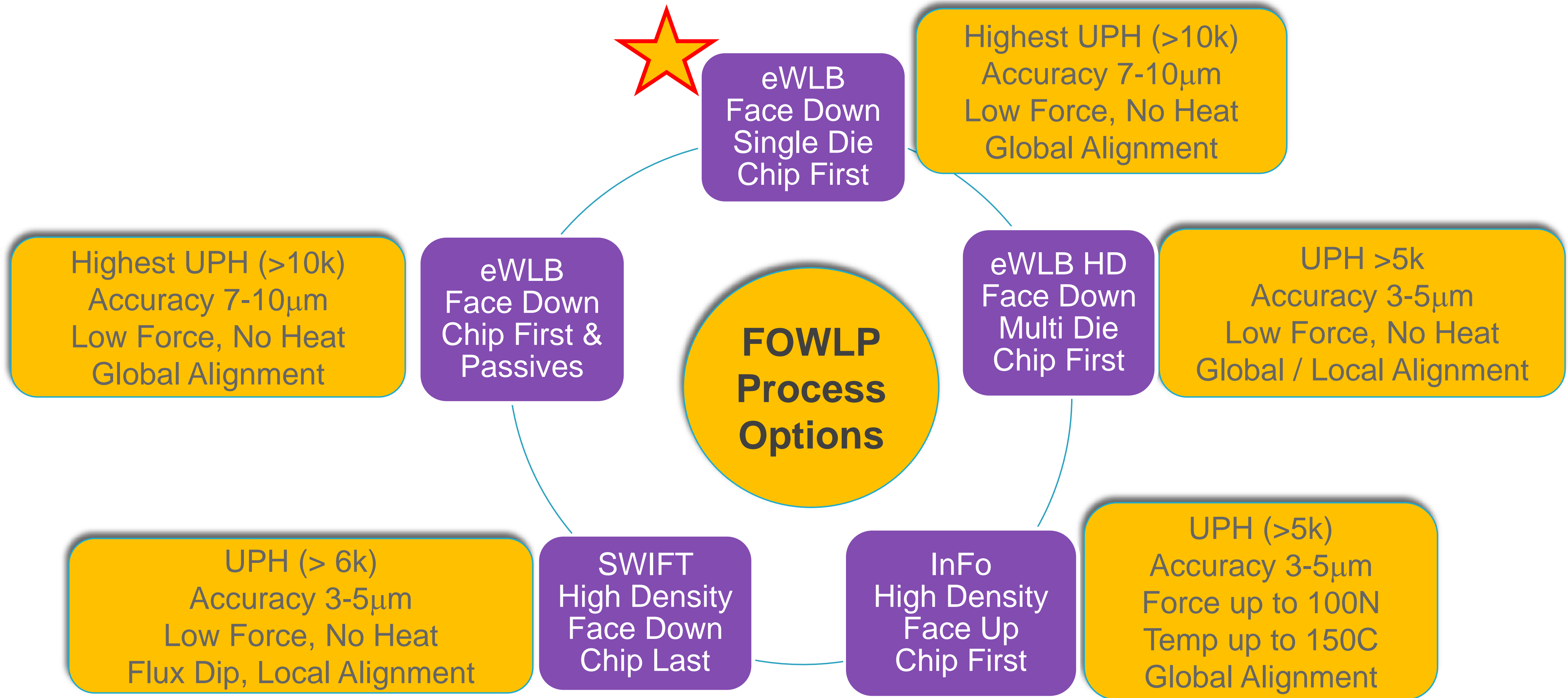

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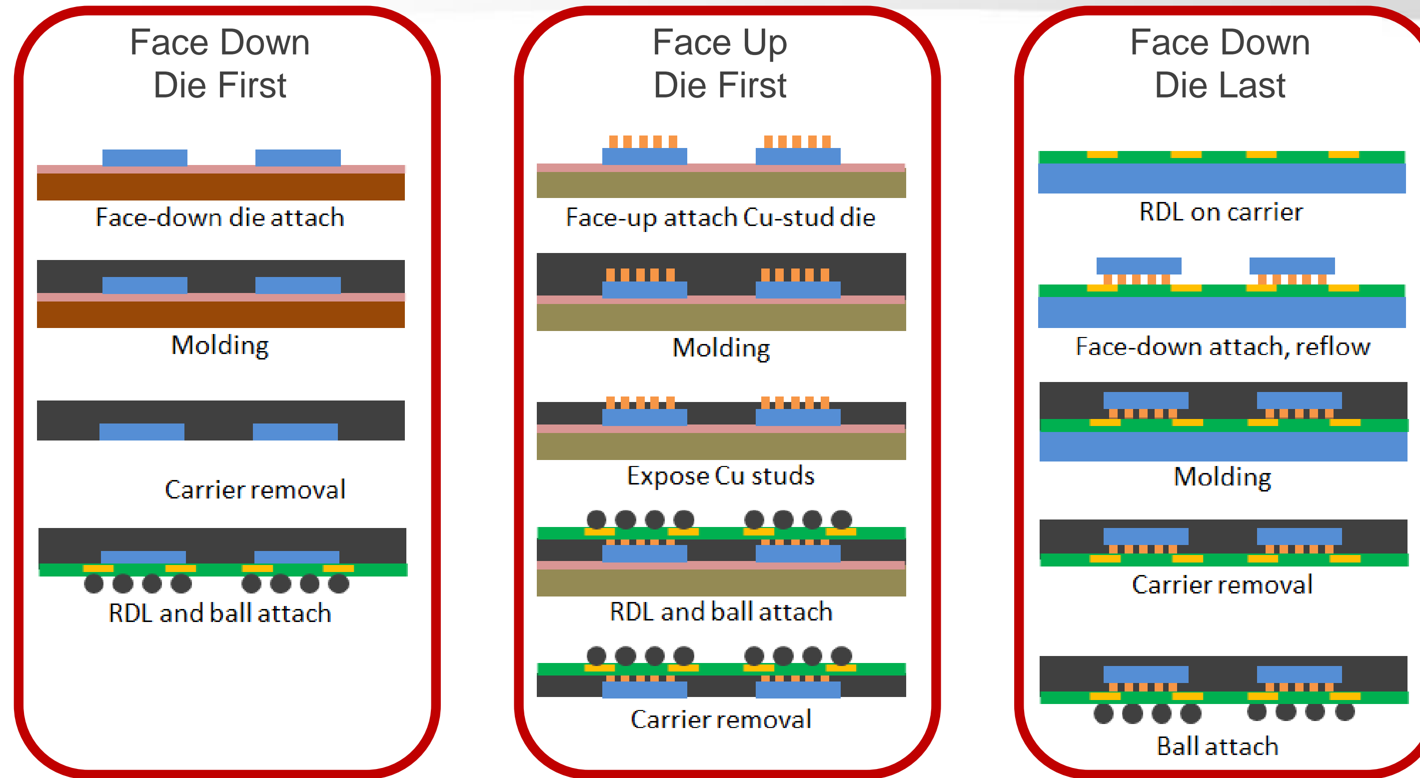
Available FOWLP Process Flows in HVM Today



- *Face Down, Die First: Typical Infineon licensed eWLB process, Highest Volume*
- *Face Up, Die First: Similar to flow used by TSMC and others, in HVM*
- *Face Down, Die Last: Similar to Amkor's SWIFT process flow*
- *Accuracy and UPH are Key Metrics for equipment selection in all flows*

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Fan-Out WLP Market Projections

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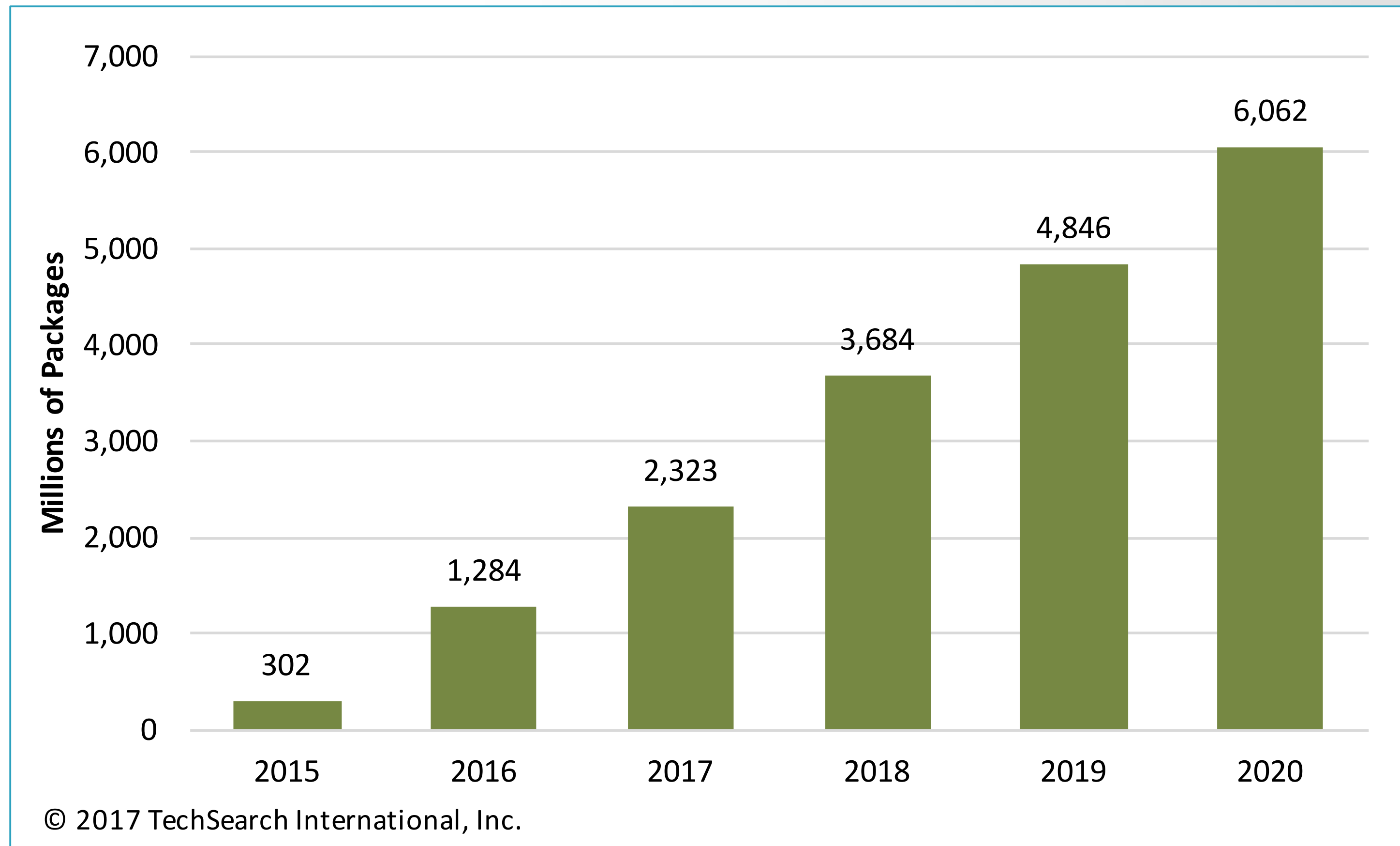

Market primarily driven by mobile products

- Applications include application processors, RF transceivers and switches, PMICs, audio CODEC, automotive radar, and connectivity modules
- Future applications include memory for top PoP and a significant growth in SiP
- Projected unit CAGR of 82% from 2015 to 2020 is the highest growth rate in Advanced Packaging

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Panel Implementation: FO-WLP to FO-PLP

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- ***FO-WLP dominates fan-out processes today***
  - HVM panel processing continues to be 2 years out
- **Panel size has not been finalized and there are many versions in development**
  - Panels commonly leverage the Flat Panel Display industry
  - Alignment to Gen 2 (360x465mm), Gen 2.5 (400x500mm) and Gen 3 (550x650mm)
    - Largest panel size appears to be 650x650mm
  - Quandary for equipment suppliers since both size and accuracy requirements are in flux
- **Yield is critical for fan-out processes**
  - Reconstitution with mold compound is not a clean process
  - >98% yield is required for each RDL layer
  - Compounding yield loss from multiple RDL layers rapidly erodes margins
  - Lower RDL count is better
- **Product allocation to panel and line utilization is challenging**
  - $100M cost for a panel line

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Process Challenges in FO-PLP

- Process challenges in FO-PLP
  - High speed die placement is absolutely required for reduced cost
  - Placement accuracy is very important
  - Panel warpage is a problem that can complicate die placement
  - Die shift can occur as molding compound cures
  - Die shift becomes critical as L/S ≤10µm
  - New dielectric dispense methods and materials are required (slit coating or dry film lamination)
  - Plating uniformity is difficult on a large area rectangular panel
- *Which products will drive the move to panel?*

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Fan-Out WLP Market Projections by Segment

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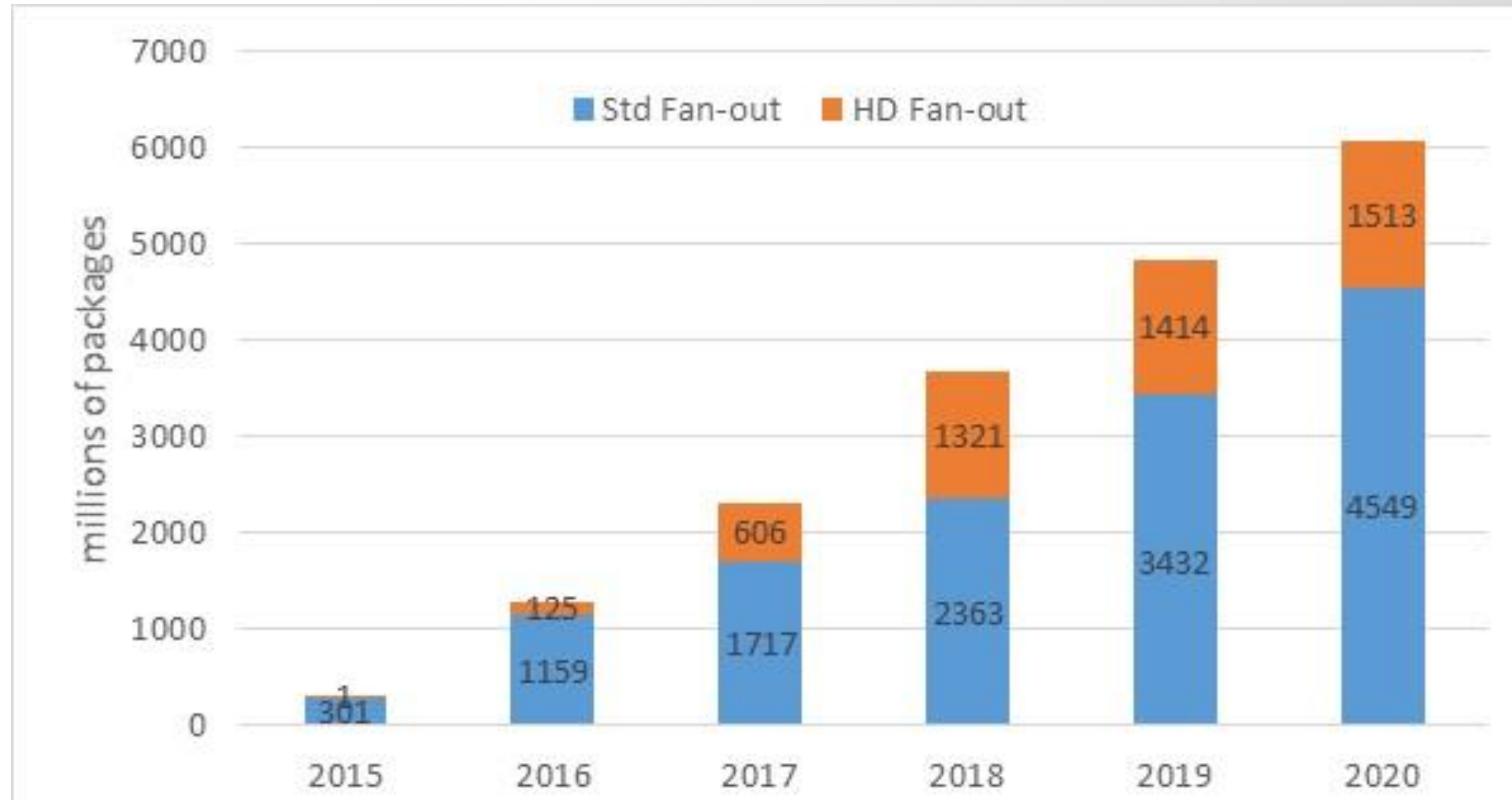

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- High Density Fan-Out market will remain on round format for the foreseeable future
- High value die will remain in highest yielding process flow (round)
- Much of the Fan-Out market will remain on round format (benefits in product mix and high yield)
- eWLB die first products will most likely be the first to migrate to panel for SiP

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Accuracy Challenges: Global vs. Local Alignment

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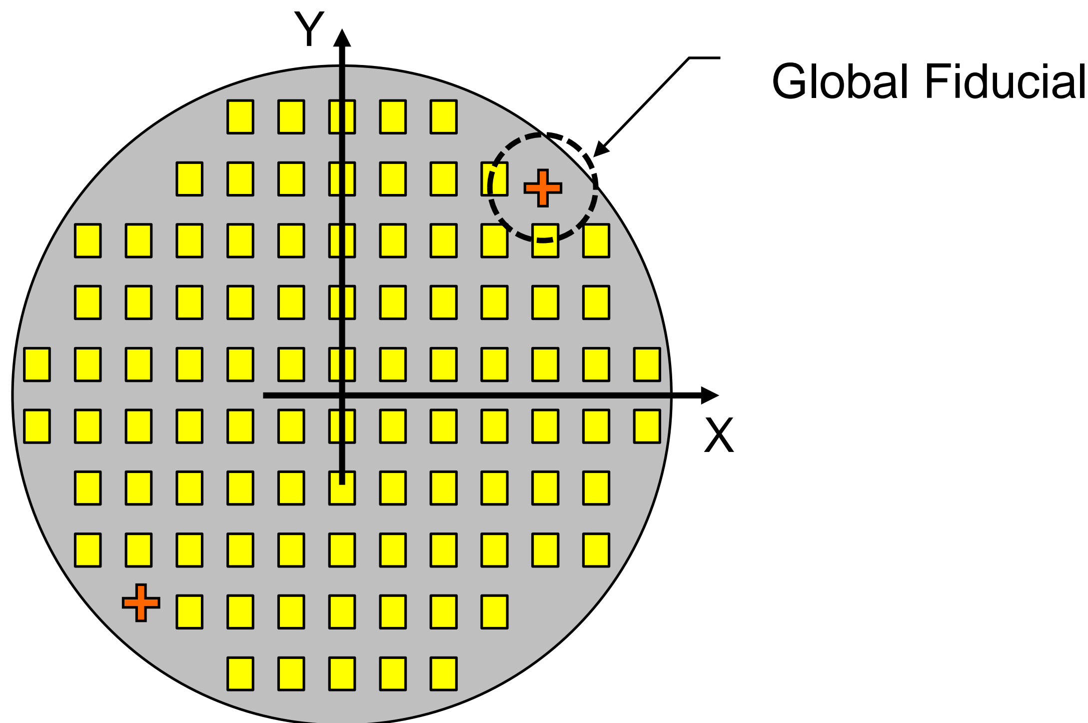
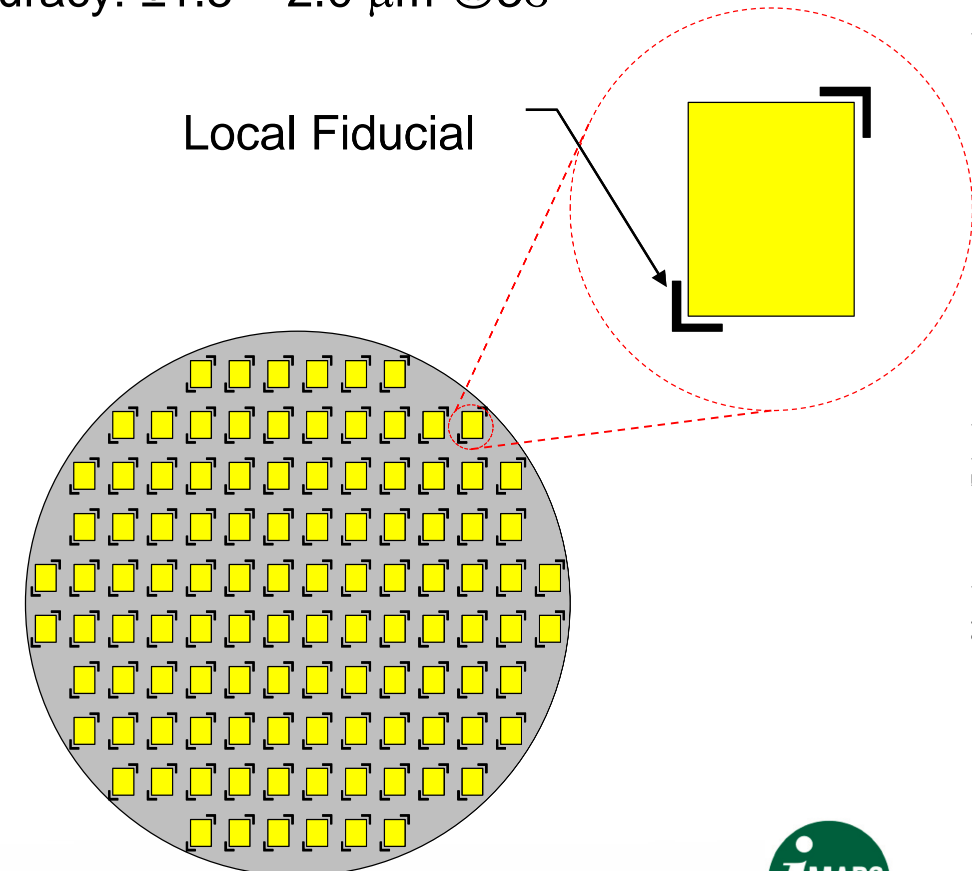
Global Alignment (fastest, lowest cost)

- All dies are aligned to a common Cartesian reference frame determined by two or more Global Fiducials
- Typically requires mapping of machine axes
- Accuracy: ±3.0 – 5.0 μm @3σ



Local Alignment (slower, higher accuracy)

- Each die is individually aligned to a Local Fiducial at the particular site where each die is placed
- Does not require machine mapping
- Accuracy: ±1.5 – 2.0 μm @3σ



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Multi-Die Alignment Capability for eWLB

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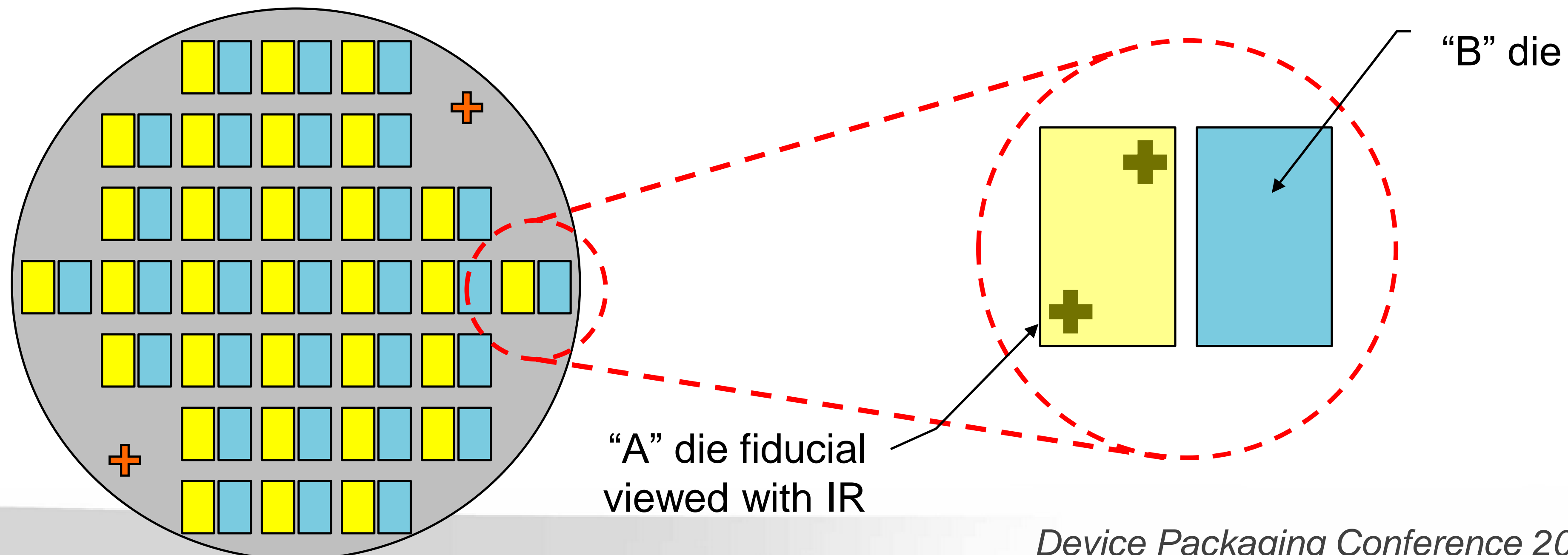
- RDL layers require accurate alignment of “B” die to “A” die
- Using global alignment for both “A” and “B” will roughly increase “A” to “B” placement error by ± 4.3 – 7.1 μm
- “A” die can be placed globally and “B” die can be placed locally, relative to “A” die
- Accuracy is reduced if aligning to the backside of “A” due to variation in dicing
- IR cameras looking through backside of “A” die can detect the fiducials
- Result is more accurate “B” die to “A” alignment



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Accuracy Challenges for FO-WLP

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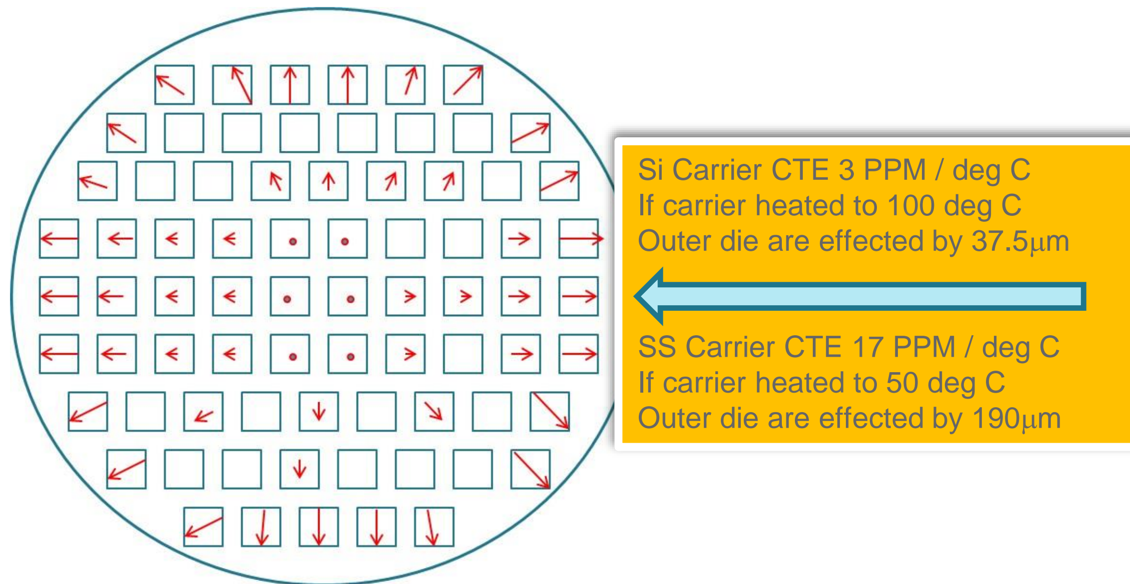
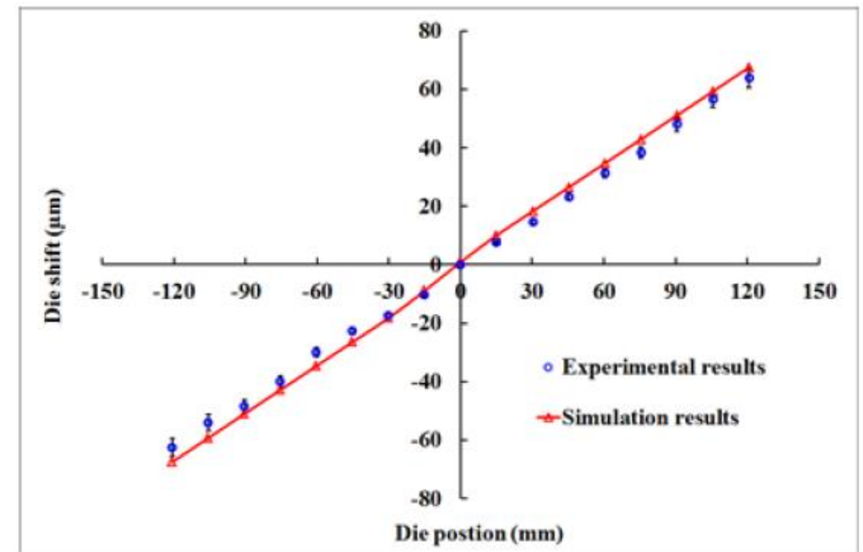
- Accurately placed die shift position during the reconstitution process due to competing factors
  - Thermal stability of equipment during die placement is critical (compounded for “hot” process)
  - Thermal expansion of carrier during placement must be controlled
  - Thermal expansion of the carrier material during molding
  - Shrinkage of mold compound during cure
- Placement error is lowest at center and greater at edge for molding and shrinkage errors





Source: Comprehensive Investigation of Die Shift in Compression Molding Process for 12 Inch Fan-Out Wafer Level Packaging Yong Han et. al. IME

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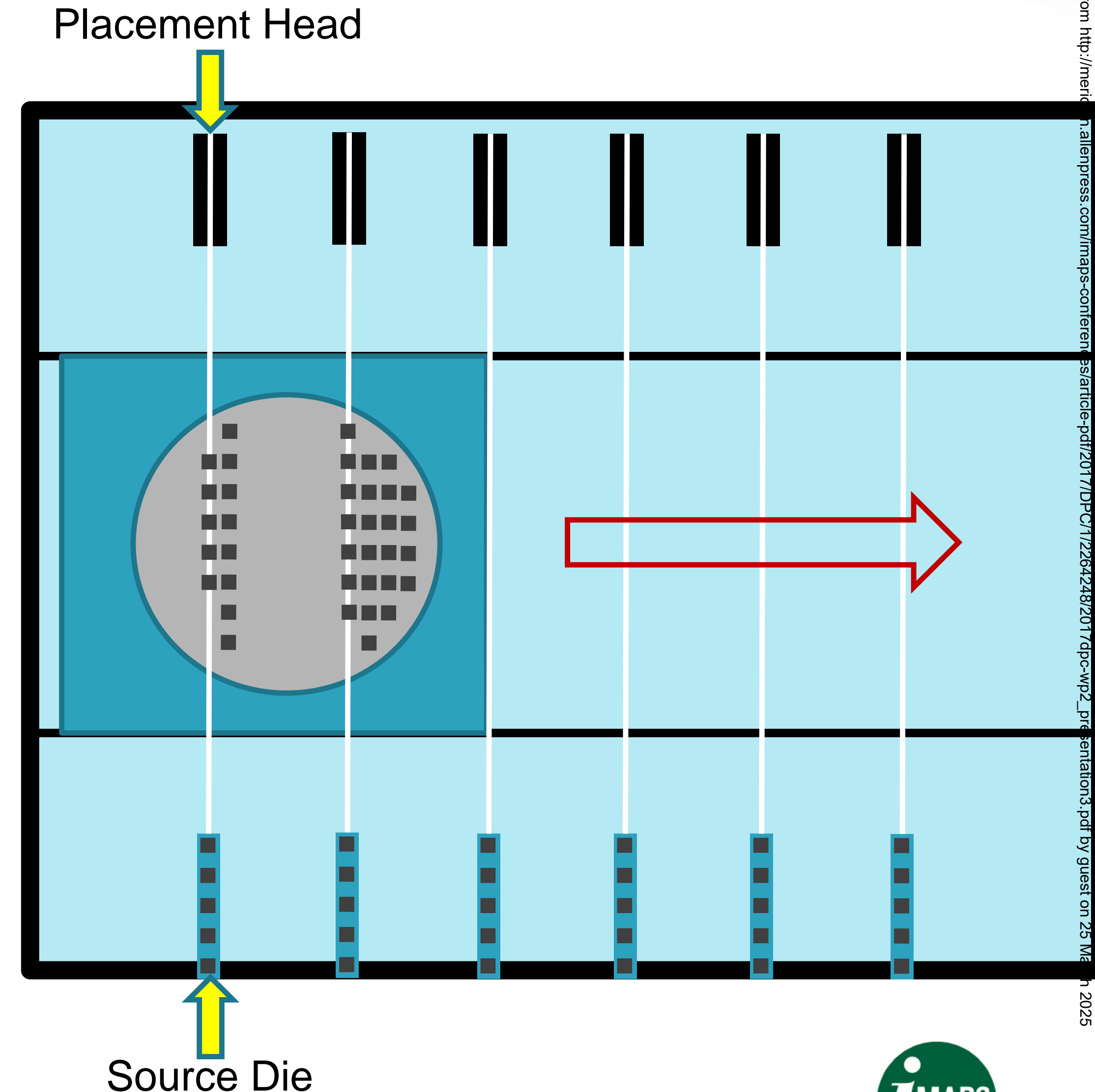
Parallel Placement Concept for High UPH

- High UPH placement using multiple heads and a linear flow of the target material
- Equipment has the potential to place die with accuracy of 7-10μm at 12k UPH
- Higher speed is possible with reduced accuracy
- Higher accuracy is possible with reduced speed
- Source die can be fed from T&R or wafer
- Passives can be added for SiP products
- Target material can be round or rectangular
- Typically no heat or force is used
- Good choice for eWLB products



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High Accuracy Placement

- High accuracy placement can be achieved with single or multi-head systems placing one die at a time
- HD die placement can use local or global alignment
- Placement accuracy is in the range of 3-5μm
- Speed is typically < 10k UPH
- Source die feed can be from either T&R or wafer on film frame
- Systems have been leveraged from equipment designed for TCB or high accuracy FC die placement
- Constant heat on for the source die and target material is available
- Force can be applied at time of placement
- TCB capability is available but no current use of TCB for fan-out

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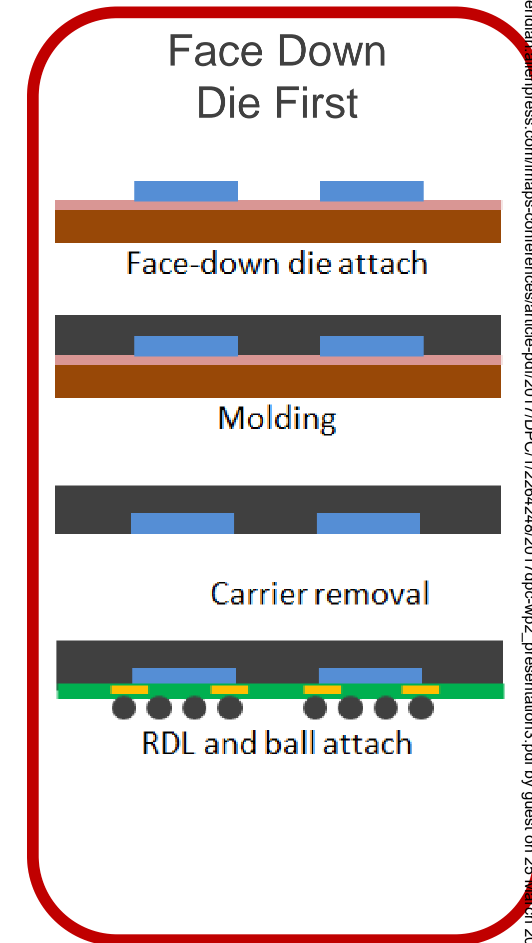
eWLB Process Flow

- Face-down, die-first process flows used for eWLB and similar processes represent the highest volume and most widely fan-out technologies in production today
- Process places the die face down onto an adhesive carrier surface prior to reconstitution using global alignment
- After reconstitution the carrier is removed
- Standard WLCSP processes are used to apply dielectrics, RDL layers and bumps
- High yield is possible for many products with a placement accuracy of 10 microns
- Round carriers are in use today with a maximum diameter of just over 300mm
- Flow is commonly used for single die products but it can also be used for multi-die products with a some requiring higher placement accuracy extending down to 3-5um
- The capability for passive placement prior to reconstitution is useful to enable some SiP products



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eWLB Process Requirements

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Speed UPH	Face Up / Face Down	Die Heat	Carrier Heat	Place Force	Flux Dip	Alignment	Die Value	Typical Flow	Applications
>10K	Face Down	low	low	< 5N	No	Global/ Local	Low	eWLB	Baseband, Power Mgmt, RF, Analog, BT

- High UPH of the placement process is the key attribute for this process flow to enable cost reduction
- Key requirements for die placement in this process include; very high speed, face down placement, no die heat, no carrier heat and low placement force
  - Placement force in the process must be well controlled to avoid the die embedding to deeply in the adhesive material
- Die shift after placement is driven by several factors including composition of the carrier material, the mold compound shrinkage during cure, and thermal expansion of the carrier during the placement process
- The process flow is typically used for single die products with lower I/O counts for mobile applications including audio codecs, power management, baseband processors, RF analog and Bluetooth
- The process flow is a good choice for SiP low cost products and it will probably be the first fan-out process to scale to panel in HVM

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InFO Process Flow

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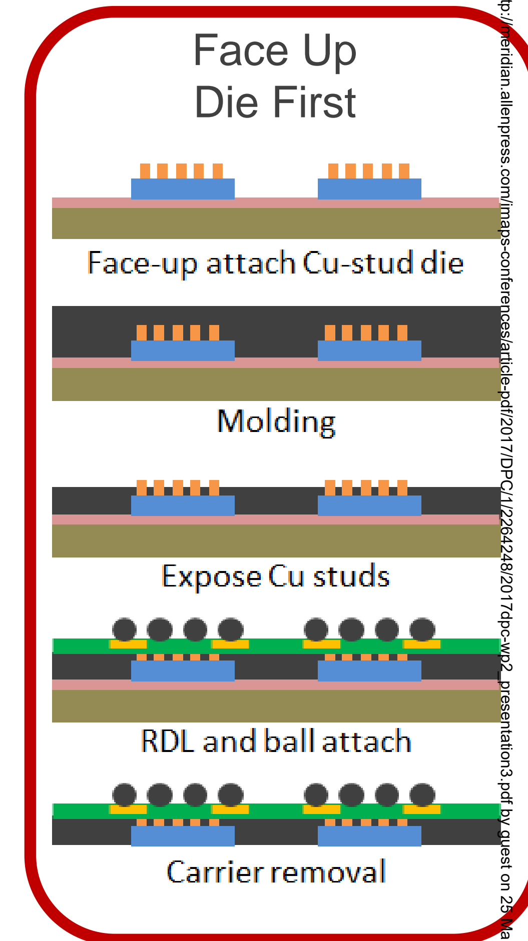
- Chip face up flows used for TSMC InFO and similar processes
- Several variations of the process from different suppliers that combine carrier or die heat up to 150C and force up to 100N
- Process flow can be used for high value die requiring fine line and space and pad pitch due to minimal die shift
- 3D versions of the process flow create an RDL layer and Cu pillars prior to die placement
- 2.5D and 3D versions of this process flow typically use global alignment schemes requiring accuracy in the range of 3-5μm
- Round carriers are used with a standard diameter of 300mm



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InFO Process Requirements

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Speed UPH	Face Up / Face Down	Die Heat	Carrier Heat	Place Force	Flux Dip	Alignment	Die Value	Typical Flow	Applications
> 5k	Face Up	<150C	<150C	<100N	No	Local / Global	High	InFO	Mobile application processors

- Accuracy of the placement process is a key attribute to ensure high product yield
- UPH >5k is possible
- The key requirements for equipment include; high accuracy, moderate speed, face up placement, die and/or carrier heat and controlled placement force up to 100N
- Process flow can support both 2.5D and 3D process options and has received much attention for packaging Apple A10 processors
- The process flow is well suited for high value die requiring fine pitch and multi-level RDL
- Typical products have high I/O counts and can include Application Processors, Memory or Multi-die heterogeneous integration

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SWIFT Process Flow

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- Amkor's SWIFT is a new addition to the portfolio of fan-out process flows
- Unique fan-out process uses a conventional Cu pillar bump structure and established assembly techniques to achieve a HD fan-out package with fine L/S
- Die are placed face down on a pre-formed RDL on a temporary carrier
- Interconnect metallurgy is formed immediately with either local or mass reflow
- Underfill is used prior to reconstitution to secure the die position and protect the solder interface enabling high accuracy and little die shift
- Reconstitution is completed, the carrier is removed and balls are attached
- Round carriers are used today with a standard diameter of 300mm

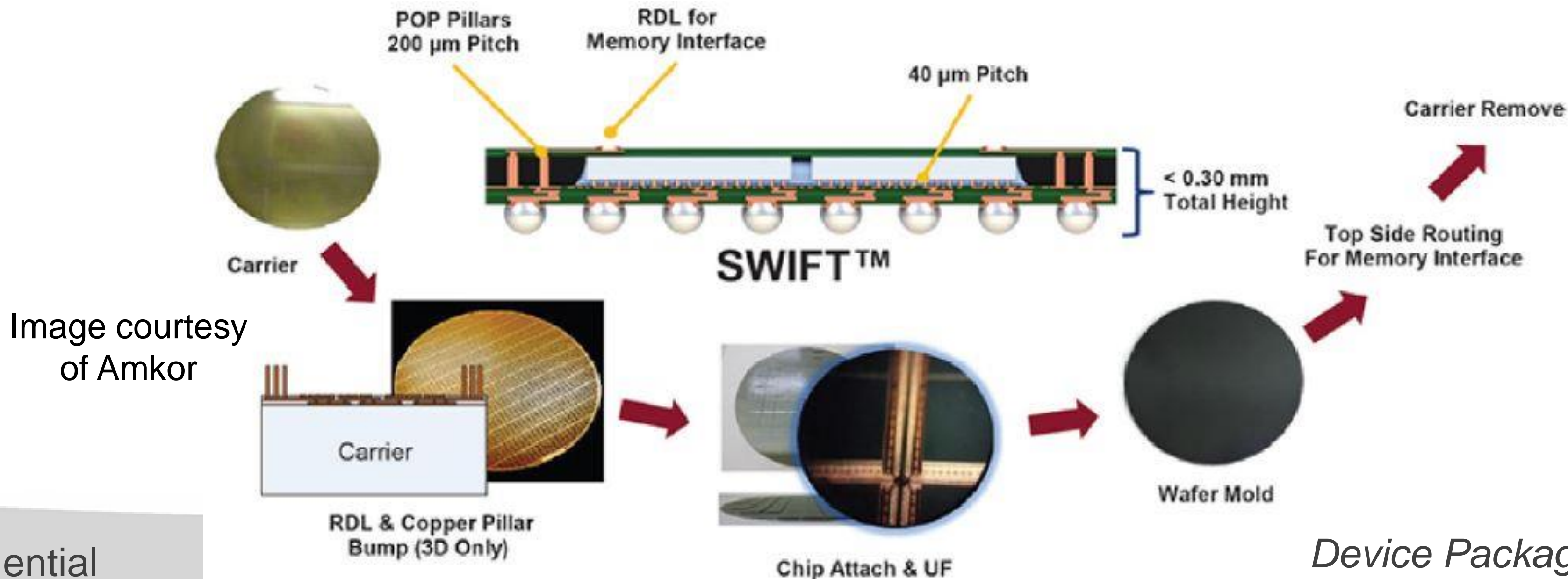
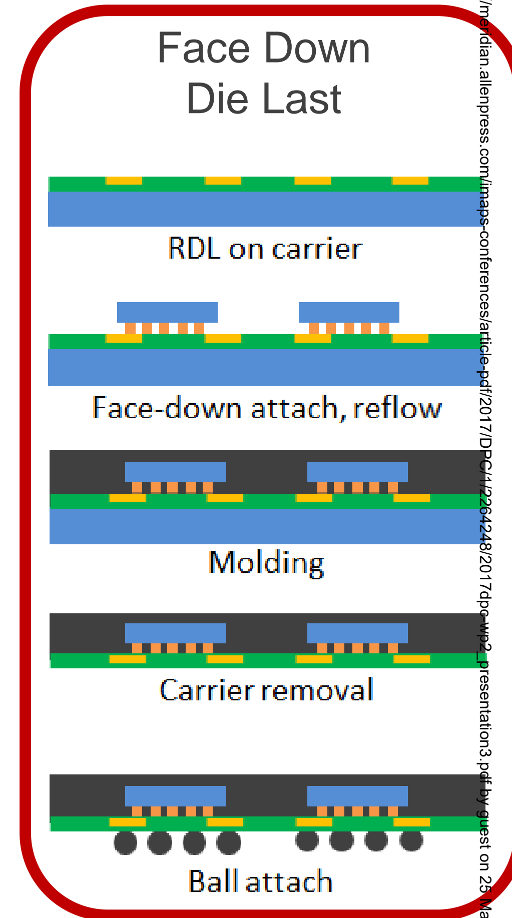


Image courtesy of Amkor



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SWIFT Process Requirements

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Speed UPH	Face Up / Face Down	Die Heat	Carrier Heat	Place Force	Flux Dip	Alignment	Die Value	Typical Flow	Applications
6-9K	Face Down	No	No	< 10N	Yes	Local	High	SWIFT	Mobile application processors, DRAM

- Key requirements for the process include; *flux dip*, high accuracy, moderate speed, face down placement, low die and carrier heat and low placement force
- Local alignment schemes are used to accurately place the die on a carrier with 3-5um accuracy
- The process is well suited for high value die or high density interconnect multi-die products with higher I/O counts due to containment of die shift
- Application Processors, Memory or Multi-die heterogeneous integration
- The process flow is a good choice for high value die requiring fine pitch and multi-level RDL with high yield

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Conclusions

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- The fan-out process space has three major groups of process flows
- Each flow has specific requirements for die placement to reduce cost, optimize yield and improve capability
- Two general categories of process flows are split between low cost and HD
- eWLB is the original commercial flow and is most widely used
  - Enables the lowest cost
  - Best candidate to move to panel
- InFO and SWIFT are competitive HD fan-out flows capable of providing fan-out solutions for high value products in 2.5D and 3D packages

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