Enabling a Robust Copper Seed Etch Process for Fine Line RDL by Electroplating on a Thin PVD Seed Layer

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Abstract

Integration of heterogeneous chips into fanout packages requires interconnection by redistribution lines (RDL). As I/O counts increase, higher density routing is required, and can be achieved by finer RDL line/space dimension, stacking multiple RDL layers, or both. Conventional WLP plating processes for pillar or RDL use a PVD deposited copper seed layer between 1000 and 4000Å thick. Removal of this copper seed layer by isotropic wet etching leads to sidewall loss that can be ignored on larger features, but can lead to significant copper cross sectional area loss on features with 2/2µm line/space and below. By enabling plating onto much thinner seed layers, next generation WLP plating chambers enable a conventional copper seed layer etch process with less sidewall loss and more uniform cross-sectional area across plated features.

Key words

RDL, Electroplating, Fanout

Introduction

In their simplest (and best defined) form, redistribution lines (RDL) allow for repositioning of the I/O pads of an integrated circuit – an extension cord of sorts. In CSP, this “within chip” RDL provides some flexibility in bond location. In fanout wafer level packaging, RDL is increasingly used to form connections between heterogeneous chips in a SIP, where these inter-chip connections are far removed from the traditional package I/O as in Fig. 1. While still massive by comparison to front end technology dimensions, the drive to higher I/O counts and placement of multiple dies within a package are driving RDL to finer dimensions. Historically WLP uses semi-additive or “through-resist” plating for RDL, with polymer passivation between successive layers as compared to the more complex (and expensive) dual Damascene approach for interconnect. RDL critical dimension is generally referenced as a line/space number in microns, so a 2/2 RDL refers to minimum line width of 2µm with closest spacing of 2µm. Of course, feature dimensions vary across the die, but smallest features plated include some 2µm lines. Current anticipated requirements to achieve highest connection density predict line/space values of less than 1/1. Yole Advanced Packaging Report for 2017 shows 2/2 entering volume production in the 2023 timeframe, but some high-end applications are likely to significantly beat this date (1,2), and in fact, are already likely in production.

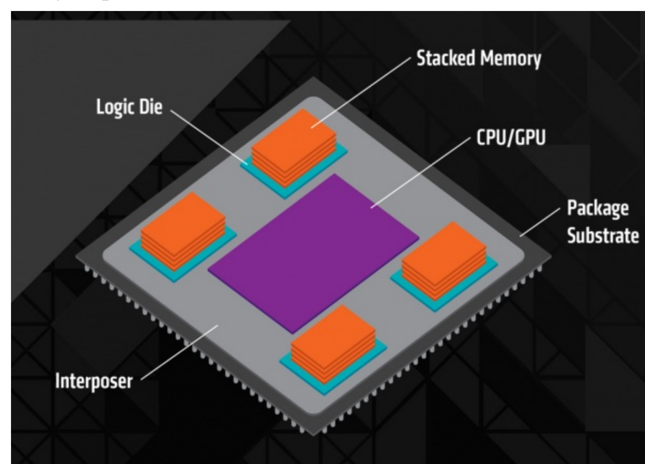

Figure 1. Representative heterogeneous SIP requiring high density fanout (3).

While there are certainly other integration challenges to fine line RDL for fanout packaging, one fundamental limitation for implementation is removing the copper seed

layer after plating the lines without impacting the electrical characteristics of the lines themselves. The seed/barrier etch process is performed in wet processing tools – first removing the copper seed with one etchant and then removing the barrier (usually titanium) with a second. By nature, the conventional copper etch process is isotropic, and removes the plated copper film (laterally and vertically) as well as the targeted PVD copper film (vertically). To ensure that the copper seed is fully removed, an overetch of 50-200% is required once the seed film is visually clear. Assuming 100% overetch on a 3000Å seed layer implies removal of 6000Å of plated copper height from the RDL (which can be compensated by plating thicker). Sidewall loss, however, should be 6000Å *per side*, so the theoretical result is a net 1.2µm loss from a line targeted at 2µm wide. Intentionally patterning a wider line to compensate for this loss creates a higher aspect ratio “space” that is more challenging to pattern and etch. This, coupled with variability in removal rates due to pattern density, also creates large variations in cross sectional area that directly influence line resistance and line resistance uniformity across the die and across the wafer.

The primary issue as mentioned above is copper sidewall loss during etching. While this is generally referred to as undercut, in a RDL there is usually nothing above the copper during the etch to create an actual “undercut”. There is some history of excessive undercut from etching of the titanium barrier beneath the RDL causing line lifting and other fails, but new etching chemistries have largely replaced dilute HF to reduce titanium undercut to manageable levels. Fig. 2 (left) shows superposition of a RDL pre and post etch – in this case about 0.4µm loss per side and 0.8µm from the top, versus undercutting of copper beneath solder in a pillar etching process (right).

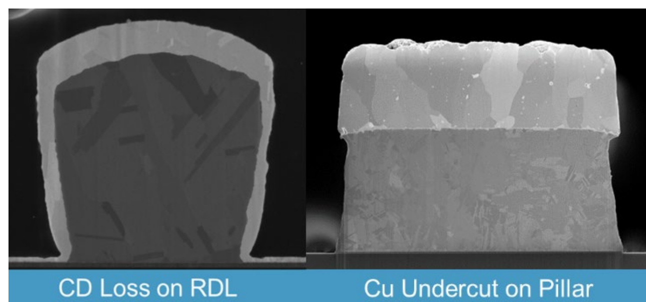

Figure 2. Superimposed pre and post etch RDL image showing sidewall loss (left), and copper undercut beneath a SnAg cap after UBM etch. (Applied internal test vehicles).

Most existing plating chambers for WLP plating require a reasonably conductive (thick) seed layer to facilitate uniform plating across the wafer. Thick in this case is 1000-4000Å of PVD Cu. A thin seed (<800Å) is highly resistive and will plate preferentially near the electrical contacts at the wafer edge, creating high thickness variation across the wafer. By using a chamber capable of plating uniformly on very thin seeds, the impact on conductivity introduced by the seed etch process can be minimized. For a nominal 200Å copper seed layer, feature sidewall loss becomes small even for much tighter line/space dimensions, and cross-sectional area uniformity is improved. We believe this reduction in copper loss, and improvement in cross sectional area uniformity, both within the die and across the wafer, should decrease line resistance and improve line resistance uniformity.

One other challenge of FO processes is the variability in plateable surface area by RDL metal layer. Depending on the density of interconnects and degree of stacking, each layer in the stack can have a different open area, ranging between 10 and 85 percent of wafer area. For thin seeds, the plated film can contribute significantly to the effective seed resistance and dramatically influence radial uniformity of the plated film. As soon as you start plating, the plated film also begins to carry current, so as you plate an 85% open RDL wafer, the effective seed resistance decreases quickly, while on a 10% open RDL wafer, the thin seed acts like a thin seed for the duration of plating time. While hardware (shielding) changes might accommodate a specific plating condition (seed thickness and open area), a second plating condition would require a hardware change to achieve acceptable results. A plating system capable of plating the full range of seed thickness and open area without hardware changes is critical for ease of use and the highest uptime.

The primary goals of this testing were as follows:

1) Demonstrate the capability of a new plating chamber to facilitate a uniform deposition of copper RDL onto thin seeds
2) Demonstrate plating capability across a range of seed thickness and open area without hardware changes
3) Optimize a UBM etch process for use in fanout processes
4) Validate that there is a benefit to using a thinner seed for fine line RDL processes and determine linewidth sensitivity.

Test Wafers

300mm silicon wafers were prepared with a blanket polymer layer (polyimide: Asahi BL-301, 7um thick) to more nearly match production wafer conditions for stacked RDL. On top of this polymer layer, a 400Å titanium barrier/adhesion layer was sputtered using an Applied Materials Charger^{TM} deposition system. Copper seed layers with thickness splits

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of 200Å, 500Å, 750Å, and 1000Å were then sputtered using the same PVD tool. Copper seed uniformity was maintained at <3% 1 sigma.

These wafers were then patterned with three different wafer masks with open areas of 10, 35, and 85%. For plating, the same chemistry (Dow 8540) and hardware were used for all runs with only recipe tunable changes to accommodate wafer variability. Plating rate was 0.8µm/minute.

The 10% open wafer was an internal test vehicle that includes 2/2 RDL features and the ability to measure RDL line resistance, line resistance uniformity, and leakage current. The 35 and 85% open wafers have minimum L/S features of 5/5 and 10/10 respectively and were used to validate plating uniformity only. It was only possible to validate copper sidewall erosion from the 2/2 features as the larger fraction of loss made the change measurable.

Hardware/Experiment

Thin seed plating was performed in a next generation plating chamber on an Applied Materials Nokota^{TM} plating tool. The plating chamber uses a patented design to mitigate current crowding at the edge of the wafer. Only one recipe input is required to dial-in uniformity in addition to total current, which defines plating rate. In most cases, acceptable uniformity was achieved within one dial-in run. Initial results are fed back into a plating model to define changes for the next run. Model parameters include seed thickness, edge exclusion, open area, plated height, and bath conductivity. After plating, the wafers were photoresist stripped and measured using an optical profilometer to validate within wafer and within die thickness.

Pattern	Open Area	Minimum Feature	Plated Thickness
A	10%	2/2µm	3µm
B	35%	5/5µm	3µm
C	85%	10/10µm	3µm

Figure 3. Platable area, minimum feature size, and plated film thickness by wafer type.

Wafers were then UBM etched using an Applied Materials Blazer^{TM} etching tool. Copper seed was removed using a standard persulfate based seed etching solution. Etch time was determined by measuring blanket layer etch rate, calculating a time to clear the target seed thickness, and then adding sufficient overetch to clear all features. Results were validated by SEM inspection as in Fig. 4. The titanium barrier layer was etched using a commercially available etching solution. Etch time was determined as above, with overetch set at 100%.

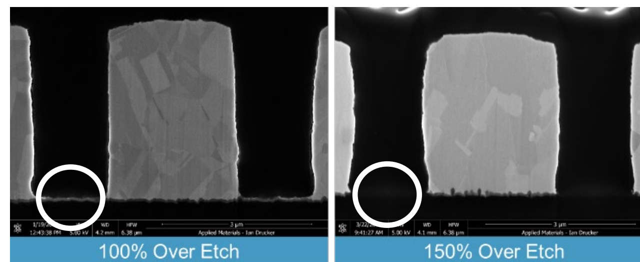

Figure 4. RDL cross sections showing residual seed layer with 100% overetch, and clear surface between lines at 150% overetch. These images after titanium barrier etch. Variability in lineshape due to lithography variation, not an artifact of the etch process.

After etching, the 2/2 line features were processed at Applied Materials Packaging Development Center (APDC) for electrical evaluation including line resistance, line resistance uniformity, and leakage current. All other wafers were analyzed for thickness uniformity. Sidewall loss on 2/2 features was measured by cross section and top down imaging on a FIB/SEM.

Results

Plating.

Using a 5% one sigma uniformity value as target, plating results on seeds down to 750Å for all open areas could be optimized within two runs. On 200Å and 500Å seed layers, the model prediction converged quickly on 85% open and 100% open (blanket film) allowing quick optimization. While the plating chamber was clearly capable at 10% and 35% open with a 200Å seed, creating both dished and domed wafers to bracket the target profile, the model for defining optimized thief current did not immediately converge to a final acceptable condition, and several additional runs were required to dial in the within wafer uniformity. Due to low wafer counts at 35% open, we focused on 10% open at 200Å seed thickness to define the challenge condition. Thickness uniformity and radial thickness profiles after plate and strip are detailed in Fig. 5 and Fig. 6.

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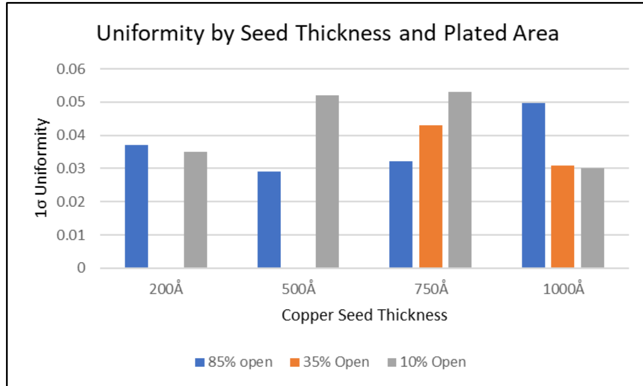

Figure 5. Calculated Within wafer uniformity, nominally less than 5%, to be further optimized.

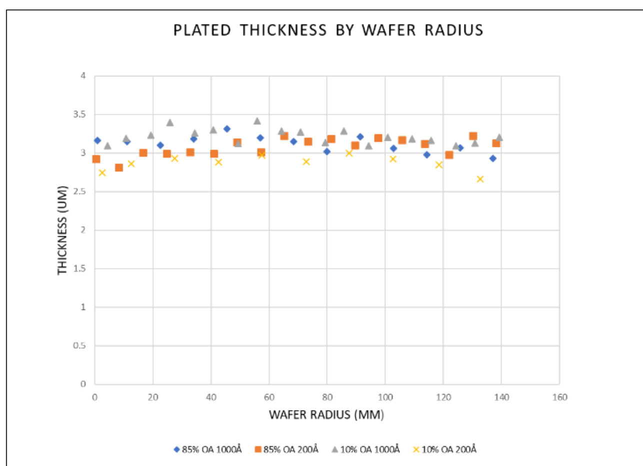

Figure 6. Radial plated thickness showing flat edge profile for 10 and 85% open, 200 and 1000Å copper seed thickness.

Etching.

The UBM etch process was defined as the process to be enabled by thin seed plating. Most etching processes are fundamentally isotropic in nature, so side wall loss can be minimized by plating on a thinner seed. While there are some possibilities for processes that are non-isotropic (dry RIE, or "seed specific" wet etching), these are not widely used and will require further development before wide acceptance. The UBM etch as implemented here uses standard hardware and chemicals currently in production.

Due to variations in lithography both within die and across wafer on the 2/2 features, it was challenging to accurately quantify sidewall loss visually. We used top down SEM and FIB cross section CD to measure sidewall loss in the 2/2 arrays. In addition to the four seed thicknesses targeted, we also processed a 1000Å seed wafer for the equivalent of a 3000Å process time to generate an extreme case. Sidewall loss versus seed thickness is presented in Fig. 7. The data shows sidewall losses on the order of half the expected loss assuming completely isotropic etching on all copper surfaces. Since the etchrate results are based on blanket etchrate data, it is not too surprising that etching into tight features (serpentines) might be slower. Most copper etch processes (persulfate included) are diffusion limited reactions, so rate will be governed strongly by aspect ratio and mass transfer.

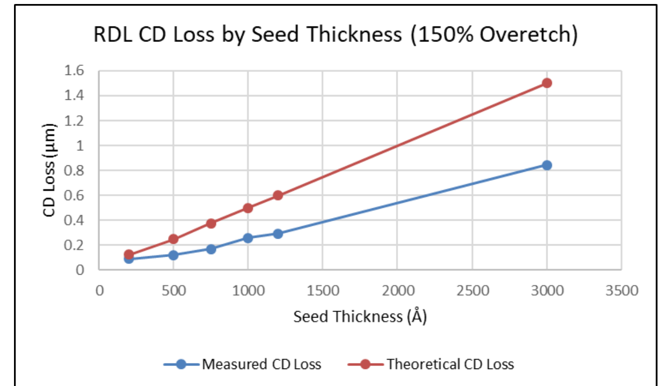

Figure 7. 2/2 line CD loss versus seed thickness versus theoretical isotropic etching.

One of the goals of this testing was to validate that a thin seed could enable a UBM etch process that has some benefit to a high density fanout flow. Presumably, the primary functional aspects of the process would be minimizing line resistance and line resistance uniformity. Using the wafers outlined above, we had hoped to demonstrate E-test results with a measurable difference in line resistance and line resistance uniformity by seed thickness on a 2/2 RDL. 2/2 lines were targeted as the feature that should show the largest loss of cross sectional area and thus show the largest increase in line resistance. In fact, due to high die to die variability in the 2/2 line (recall Fig. 4), we could not distinguish a statistical difference in either line resistance or line resistance uniformity based on incoming seed thickness. Wafer quality (2/2 lineshape consistency) was likely the dominant factor increasing variability, and while we could not demonstrate a consistent trend using the wafers from this dataset, Fig. 8 shows some historical (internal) data that indicates the expected trend in line resistance based on a larger amount of copper removed in a thicker seed etch. It seems likely that for smaller linewidths (or on wafers with more consistent 2/2 features), the increase in cross sectional area loss by etching a thicker seed should magnify the line resistance response.

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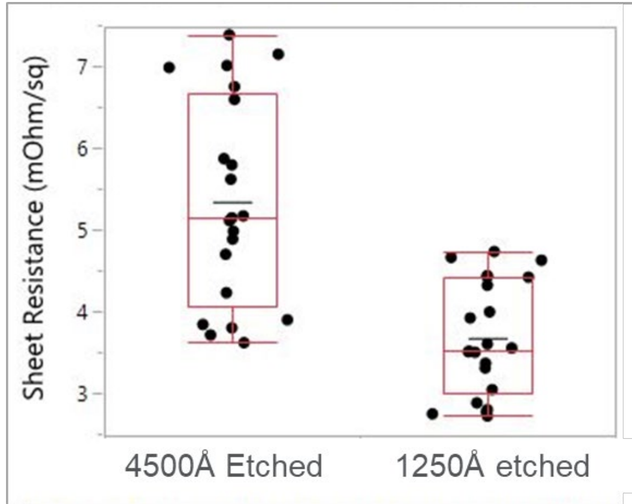

Figure 8. Etest data from a 2/2 serpentine on 500Å seed layers with 800% and 150% overetch. Data from 200Å and 1000Å seeds with 150% overetch (corresponding to 500Å and 2500Å etched) did not show a measurable difference in line resistance.

Since the copper sidewall loss was of most importance for this study, a standard etching condition for 400Å titanium barrier etching was implemented on all wafers. Titanium undercut results for each side of a 2/2 feature at wafer center and edge are shown in Fig. 9. Undercut values measured by FIB/SEM are on the order of 0.1µm per side. This is the nominal result expected using optimized chemistry on a feature not subject to strong galvanic etch effects.

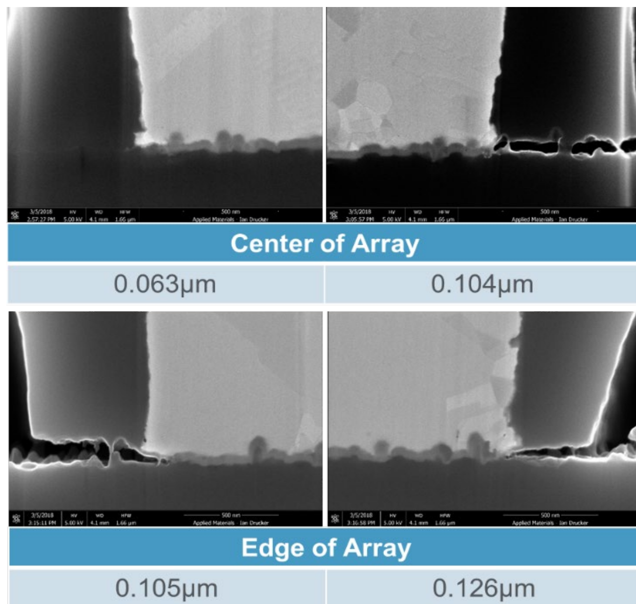

Figure 9. Nominal titanium undercut of about 0.1µm, from 400Å titanium barrier etch.

While copper seed thickness is unlikely to have much influence in the titanium barrier etch process, we have included some data here to highlight options as part of a complete UBM solution for fanout.

Conclusion

A baseline process utilizing thin copper seed layers for high density fanout has been demonstrated. Wafers with seed layers as thin as 200Å were plated uniformly using a next generation WLP plating chamber designed for flexibility and ease of maintenance. Plated thickness uniformity matches conventional reactors plating onto much thicker seed layers, and all plating variables to compensate for seed thickness and open area are recipe programmable (no hardware changes).

While the results presented here hint strongly of a process advantage to using thin seed plating for high density fanout on fine RDL features, our electrical data did not fully support this conclusion. Intuitively, reducing total copper etch time to remove a thinner seed layer during UBM etch will reduce cross sectional area loss, and as feature dimension drops to 2/2 and below, the expected decrease in line resistance and improvement in line resistance uniformity should be enable higher I/O counts and better device reliability.

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