AIP Conference Proceedings

RESEARCH ARTICLE | JANUARY 29 2001

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AIP Conf. Proc. 550, 33–37 (2001)
https://doi.org/10.1063/1.1354372

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HTML ABSTRACT

Technology in the Internet Era

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Abstract. In the PC Era, Microcomputer (µC) and memory were the components that drove growth of the PC industry. In the Internet Era, Digital Signal Processing (DSP) and Analog will be the components that drive growth in Internet Products. Over the next 10 years, technology will continue to follow Moore's Law of scaling, and in addition System-on-a-Chip (SOC) integration will drive technology.

INTRODUCTION

Since the late 70's, the Personal Computer has been the application which dominated the semiconductor industry, and Moore's Law of shrinking gate transistor size has been the principle that drove the technology. This made a lot of sense: PC's are built around a microcomputer and memory, and shrinking the transistor made these functions smaller, faster, and cheaper.

But Internet Products are replacing PC's as the dominant application for semiconductors (Figure 1). Internet products depend, not on a microcomputer and memory, but on Digital Signal Processors (DSPs) together with analog functionality [1]. For most Internet System-on-a-Chip (SOC) products, shrinking transistor size alone does not improve system cost and performance. It is necessary to integrate the DSP and Analog functions into Mixed Signal SOC's. This means that, in the Internet Era, Moore's Law will have to share the driver's seat of semiconductor technology with SOC integration.

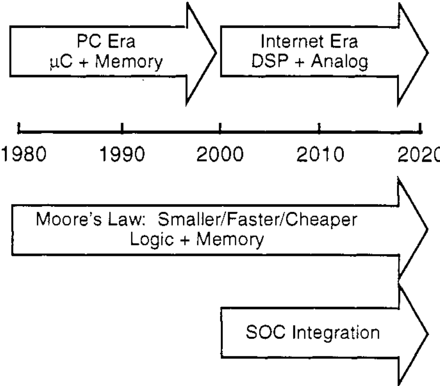

FIGURE 1. In the PC Era, µC & Memory were the semiconductor components that fueled the PC industry. In the Internet Era, DSP & Analog will drive the Internet industry. SOC Integration together with Moore's Law will be the imperatives for Si Technology innovation.

MOORE'S LAW: 2010

There is evidence that planar CMOS will continue to follow Moore's Law scaling at least to the 35 nm generation [2] [3]. Figure 2 shows the International Technology Roadmap for Semiconductor (ITRS) forecast [4]. The 1998 and 1999 forecasts both show DRAM half-pitch shrinking by 70% every three years. This results in a doubling of logic density every three years and projects that the 35 nm generation will be in production in 2014. Also shown in Figure 2 is the forecast gate length for high performance Microprocessor Units (MPUs).

However, competition is driving some companies to achieve a 70% shrink every **two** years. Whether this pace can be maintained through the decade is problematic and depends on their ability to solve the Grand Challenges discussed below. If these Grand Challenges can be solved, the industry could be at the 35 nm generation by 2009!!

CP550, *Characterization and Metrology for ULSI Technology: 2000 International Conference,*
edited by D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith, and E. M. Secula
© 2001 American Institute of Physics 1-56396-967-X/01/$18.00

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A recent trend in the industry is very aggressive scaling of poly gate length (here defined as the length of the poly gate where it contacts gate insulator). Gate length of around 100 nm is in production today (180 nm generation), and gate length of 50 nm or less will be in production in 2003. By 2009, gate length is expected to 20 nm or less (35 nm generation).

There are many obstacles to overcome, but the Grand Challenges are Lithography, Gate Insulator, and Static Leakage Current.

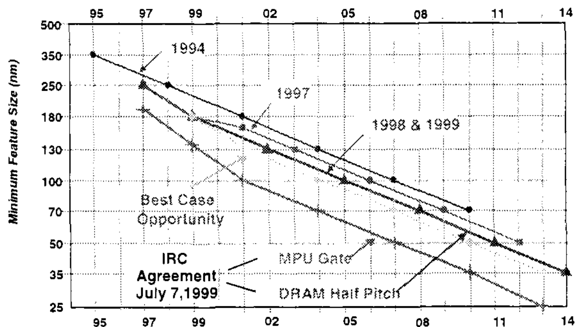

FIGURE 2. ITRS forecast for DRAM half-pitch. Also shown is the ITRS-99 forecast for MPU gate length. Many companies appear to be exceeding this forecast.

Lithography

Figure 3 illustrates the well-known fact that the feature size of ICs in manufacturing today is well below the wavelength of light being used. 193 nm optical tools will replace 248 nm tools in 2001 for patterning of critical geometries. But products having 100 nm gate length are in production today, using 248 nm exposure tools, and gates are expected to shrink to 50 nm by 2003. 157 nm production tools are forecast to be available for production in 2004-2005, but by this time gate lengths will be below 50 nm.

As device feature sizes continue to get smaller, Optical Proximity Correction (OPC) becomes necessary to compensate for diffraction effects in the patterning operation. The exposure masks used to print the circuits are corrected by addition or subtraction of geometries to the design database to ensure the fidelity of the printed pattern.

Phase Shift Masking (PSM) is another technique that has been used to produce DRAMs. This technique will be required to print 90 nm gates for logic products in 2001 with 248 nm lithography tools, and its use will continue as the minimum feature size continues to shrink faster than the wavelength of light.

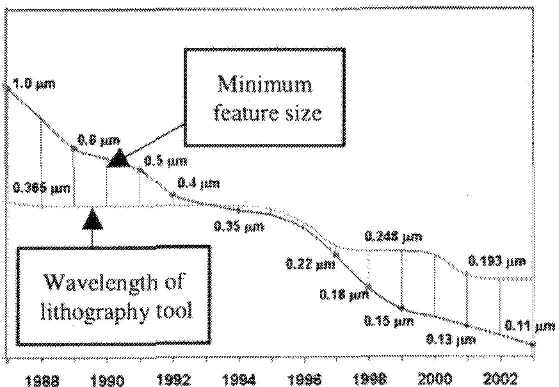

FIGURE 3. Minimum feature size has been shrinking faster than the wavelength of the exposure radiation requiring the use of Resolution Enhancement Techniques (RETs).

OPC and PSM are examples of Resolution Enhancing Techniques (RETs) that are being developed. Other RETs that will see increased use include the use of hard masks, thin resist and off-axis illumination.

In the latter part of the decade several Next Generation Lithography (NGL) approaches are being planned.

- SCALPEL: A masked e-beam exposure technique
- EUV: An exposure technique based on Extreme UV: 13.4 nm
- X-Ray

Gate Insulator

In 1970, MOS transistors had gate oxide thickness of 100 nm. Today the transistor gate length is 100 nm, and gate oxides are shrinking below 2 nm. There are two factors that limit the continued shrinking of SiO_2 for the gate insulator.

1) Reliability
2) Gate leakage

Figure 4 shows the history of gate oxide reliability at constant 8MV/cm field strength. Below 40Å, the reliability margin decreases dramatically [5]. Figure 5 shows the exponential increase in gate leakage that results when SiO_2 thickness shrinks.

Nitrided oxides are being used to increase the dielectric constant of the gate insulator. Figure 5 shows that Remote Plasma Nitrided Oxide (RPNO) can be used to increase the physical thickness and reduce tunneling current.

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RPNO and other nitridation techniques maintain the Si-SiO_2 interface which is so critical to device behavior. Within the next 5 years, however, alternate high-k dielectrics will be required. Materials being considered include:

- Si_3N_4
- Ta_2O_5
- TiO_2
- Al_2O_3
- ZrO_2
- Y_2O_3
- $SrTiO_3$
- Zr/HF Silicate

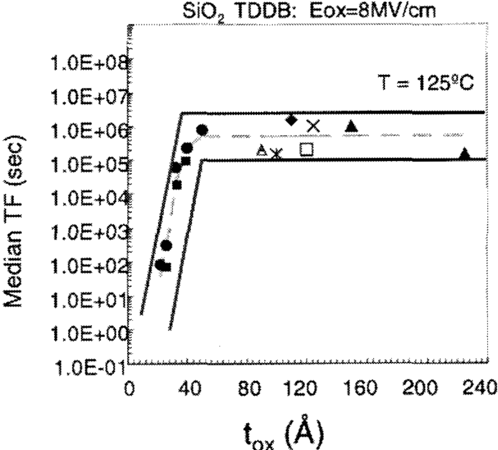

FIGURE 4. At the oxide field of 8 MV/cm, oxide reliability is constant down to about 40Å. Below 40Å, reliability degrades.

Leakage Current

Transistor drive current I_{drive} and off leakage current I_{off} are approximated by the equations

$$I_{drive} \approx \frac{C_{ox}\, v_{sat}\, (V_{DD} - V_t)}{1 + 2\, v_{sat}\, R_{SD}\, C_{ox}} \qquad \text{Eq (1)}$$

$$I_{off} \approx A \exp\left[\frac{-qV_t}{mkT}\right] \qquad \text{Eq (2)}$$

As V_{cc} drops, technologists have decreased V_t in an effort to maintain I_{drive} constant from one generation to the next. As a result, I_{off} has increased substantially. This causes high standby leakage which limits battery life for hand-held products. Digital electronics in battery operated products such as cell phones typically have off leakage of 10pA/µm of width whereas high performance CPUs have 1-10nA/µm of leakage.

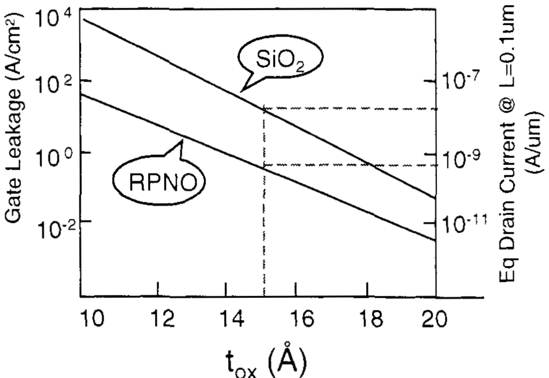

FIGURE 5. Gate tunneling current as a function of t_{ox} for SiO_2 and RPNO. For SiO_2 t_{ox} is physical thickness. For RPNO, t_{ox} is the electrically equivalent physical thickness. As t_{ox} shrinks gate tunneling current increases exponentially. An RPNO gate insulator, because its effective dielectric constant is 20% higher than SiO_2 has a 20% thinner electrically equivalent thickness.

In addition to sub-threshold leakage given in Equation 2, gate tunneling leakage below t_{ox} = 20Å becomes a substantial power drain (Figure 5). For SiO_2 gates, we are at the point today where continued performance gains cannot be made unless we relax the 10pA/µm leakage spec. High k insulators will relieve this limitation by allowing C_{ox} in Equation 1 to increase, but the trade-off between I_{drive} and I_{off} will be one of the major imperatives at the next decade. It will be addressed in two ways

1) New design techniques will be developed that will reduce chip-level static leakage even though the transistors are "leaky."
2) The technology for battery operated products will continue to diverge from the technology for high performance CPUs.

SOC INTEGRATION

The electronics in a typical cell phone are shown in Figure 6. From this, it is clear that further shrinking of the major ICs will have only limited impact on the overall cost of the electronics: The key to further dramatic cost reductions of phones having today's functionality is the integration of diverse functions.

As shown in Figure 7, most Internet Products consist of a Radio, a Modem, an Applications Processor and Power Management functions. This generic functional block diagram applies to Cell

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Phones, 3G phones, DSL modems, Cable modems, PDAs, Short distance wireless, VoIP electronics and many more products.

Today's Cell Phone	
ICs	12
Discretes	16
Passives	214
Other	8
Total	250

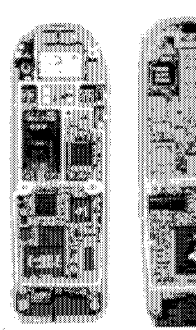

FIGURE 6. Shrinking the size of the ICs in a cell phone has limited impact on board area. Component reduction through SOC Integration will be important to cost reduction.

The functions in Figure 7 require diverse process technologies which is the reason they are on separate chips today.

- High performance, high density digital CMOS logic having low active power, and in portable applications, low standby power.
- Embedded RAM: SRAM or DRAM
- FLASH EEPROM or non-volatile memory replacement such as FeRAM
- Analog CMOS for Analog Baseband functions.
- RF BiCMOS or CMOS for radio or tuner functions.
- Extended Drain CMOS capable of withstanding 5-10V voltage surges.
- Technologies to enable passive integration: capacitors, inductors, varactors.

SOC integration does **not** mean combining all functions of the application on a single chip. What it **does** mean is an integration strategy that continually reduces the number of components. A representative integration strategy for today's functional cell phone is shown in Figure 8.

The end state of SOC integration is often characterized as a "single chip." In many cases, this is not possible: power amplifiers, line drivers and some passives will probably remain "off-chip" for the foreseeable future.

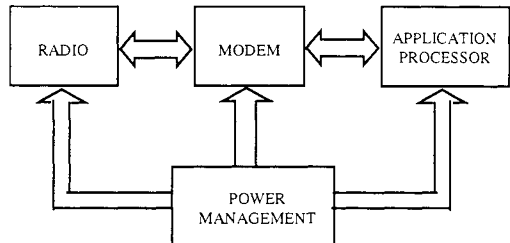

FIGURE 7. Most Internet Products consist of a Radio, a Modem, an Application Processor and Power Management functions.

In cases where the integration strategy involves integration of analog functions (analog baseband, rf and power management) onto digital chips, it is obvious that functions must be implemented in state-of-the-art deep submicron CMOS. However, even in cases where the SOC integration strategy involves integrating analog functions together but separate from digital functions, state-of-the-art deep submicron CMOS offers the lowest cost solution. Analog functions do not scale as rapidly with shrinking feature size as digital functions, but the chip size reduction is significant. Digital logic scales in a highly predictable way as the square of the feature size: A 70% shrink of the feature size results in a 50% shrink in logic area. Analog functions are not as predictable in their scaling but seem to scale linearly with feature size: A 70% shrink in feature size results in a 70% reduction in area for analog functions.

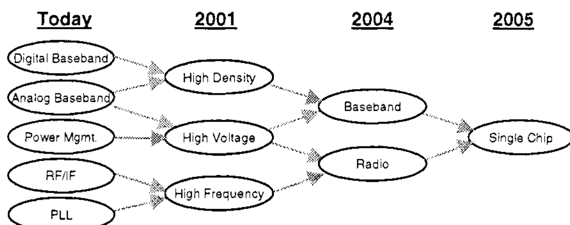

FIGURE 8. Example of a possible integration strategy for cell phone electronics. Integration of passive components will occur in parallel. The "single chip" is a misnomer: For GSM, the Power Amplifier will be a separate component, and some discrete passives will remain.

In summary, the primary advantage of SOC integration is cost reduction through reduction in number of components and component cost. There are additional benefits: reduction in assembly cost,

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performance improvement, and power reduction. However, there are many challenges.

The biggest challenge to implement analog/rf functionality in deep submicron CMOS is the reduced voltage. Figure 9 shows how the supply voltage of digital CMOS has come down in recent years. Many analog circuit architectures and circuit design techniques are not extendable to low voltage, and new architectures need to be developed. Particularly useful at low voltage are architectures which employ digital logic to replace analog functionality: Architectures such as

- Digital compensation for fractional-N PLLs
- On channel modulation for phase modulated systems (GSM)
- Digital error correction in ADCs
- Digital linearization of amplifiers and tuners.

Another solution to the voltage problem is to add higher voltage "analog" components to the digital logic flow

- A 2.5V CMOS having a thicker gate oxide from the core logic
- A 2.5V-3.5V Si or SiGe BJT

In these instances 3-4 masks are added which adds 10%-12% to chip cost.

Extended drain (ED) CMOS can be used in power management functions which require interface to a battery charger and which must withstand voltage surges of 5V-10V.

Other technology modules that will be useful for implementing analog functions include

- Isolation including SOI
- High-Q inductor
- High density, high-Q capacitors
- Varactors

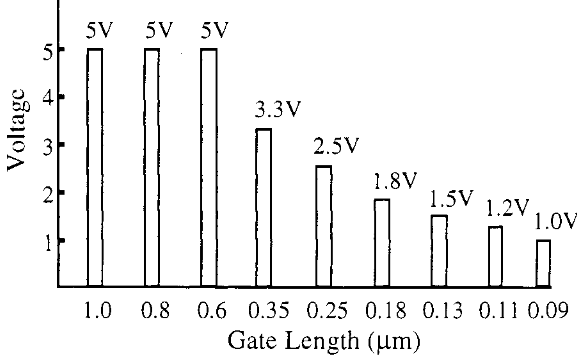

FIGURE 9. Supply voltage has been coming down in recent years making it difficult to design analog circuits.

and in the future, MEMS high isolation, low impedance switches and MEMS mechanical resonators.

SOC integration also poses challenges in terms of

- Testing chips which contain complex analog and digital functions
- Rapid migration to the most advanced technology

CONCLUSION

Moore's Law scaling of feature size together with SOC Integration will provide the two drivers of Si technology development in the next decade.

Technology R&D costs will continue to increase at a faster rate than semiconductor revenue. As a consequence of this, small companies will become fabless, and foundries will increase market share.

By the end of the decade, deep submicron IC manufacturing will be about equally divided between foundries and a small number of large Integrated Device Manufacturers (IDMs) who can afford the increasing cost of technology R&D.

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