Journal of Electronic Packaging

Editorial

Special Section on InterPACK 2015

InterPACK 2015, the flagship conference of the ASME Electronic and Photonic Packaging Division held on July 6–9, 2015 in San Francisco, CA, is the premier international forum for the exchange of state-of-the-art knowledge in research, development, manufacturing, and applications of electronic packaging, MEMS, and NEMS. This is the first time that the InterPACK has been held jointly with the International Conference on Nanochannels, Microchannels, and Minichannels (ICNMM). Jointly organized and held, there was an outstanding technical program featuring more than 600 technical presentations in nine technical tracks. The Technical Track Committees comprise leading researchers and engineers from industrial companies, government laboratories, and academic institutions throughout the world. The nine tracks are: (1) Advanced Electronics and Photonics: Packaging, Interconnect, and Reliability, (2) Emerging Technology Frontiers, (3) MEMS and NEMS, (4) Thermal Management, (5) Thermal Management Using Microchannels, Jets, and Sprays, (6) Fundamentals of Thermal and Fluid Transport in Nano-, Micro-, and Mini-scales, (7) Advanced Fabrication and Manufacturing, (8) Energy, Health, and Water-Applications of Nano-, Micro-, and Mini-scale Devices, and (9) Advanced Electronics and Photonics, Packaging Materials, and Processing. At the end of the conference, each track chair was invited to recommend two papers from their track for this special section. All the recommended papers are again reviewed and some of them are selected for publication in this special section.

This volume comprises 14 papers broadly focused on microscale heat transfer. There is one paper that focuses on impact mechanical performances of printed wiring board assemblies. These papers exemplify the analysis and exploration of computational models and experiments as well as novel materials and processes to provide invaluable insights into the problems studied and offer design recommendations.

Saenen and Thome presented a novel dynamic model of a microchannel evaporator that can handle the entire spectrum of compressibility. The model is robust with respect to time discretization and is accurate both in time and space. Oprins et al. used an advanced stackable CMOS test chip to study the thermal performance of a three-dimensional (3D) stacked package with two dies. The test chip features 832 individually controllable heater cells to create a programmable power dissipation distribution and uses a 32×32 array of temperature sensors to measure the chip temperature distribution map. Patankar et al. developed a novel approach of using vapor chambers of ultrathin form factor to demonstrate the metrology developed for characterizing the thermal resistance and condenser-side surface temperature uniformity. Comparing the performance of the vapor chamber to a copper heat spreader using the proposed metrics revealed that the vapor chambers may redistribute the condenser-side surface temperature with increasing power, beyond what is possible with heat spreading by conduction alone. Shavik et al. used nonequilibrium molecular dynamics (NEMD) simulations to investigate explosive boiling phenomena for a thin liquid argon layer over nanostructured solid surface for hydrophilic and hydrophobic cases. The heat transfer rate from solid surface to the liquid significantly increases with the increase of the surface wettability. Tollkoetter et al. studied the bubble dispersion and bubbly flow in different orifices and channel modules. This study is very useful for microreactor industry. Schlottig et al. demonstrated the Lid-Integral Silicon Cold Plate topology as a way to bring liquid cooling closer to the heat source intergrated circuit and eliminated one thermal interface material in the system. It also enables to use wafer-level processes and to ease integration in first level packaging. Lee et al. explored extreme heat flux limit of microcooler for GaN-based high-electron mobile transistors that have local power densities exceeding $30\,\mathrm{kW/cm^2}$ using solid conduction simulations and single-phase/two-phase conjugate simulations. Gallandat et al. demonstrated the possibility to tune to the convective heat transfer coefficient by selectively changing the density of micro-hydrofoils to compensate for the change in fluid temperature along a heat exchanger channel. This helps improve the life time of power electronics devices. Fish et al. assessed how the thermal spreading resistance present in arrays of vias in interposers, substrates, and other package components in 3D packaging can be properly incorporated into the numerical modeling of these arrays. Zhang et al. developed a novel thermal test bed with an embedded staggered micropin-fin heat sink. Brunschwiler et al. proposed a cooling topology roadmap for 3D chip stacks. This approach can potentially reduce the number of thermal interface materials or even completely mitigate them. Demetriou et al. took a holistic approach to evaluate the total cost of ownership of IT hardware cooling solutions considering the combined impact of IT cooling hardware, data center hardware, and energy cost. Roy et al. developed a reliable thermal interface material using low-melt alloys containing gallium, indium, bismuth, and tin. In situ thermal performance of these low-melt alloys is conducted.

Meng at al. studied the high-frequency oscillations that arise in printed wiring boards due to secondary impacts. These high-frequency oscillations occur due to stress wave propagation and reflections through the thickness of the multilayer wiring board.

These fine collection of papers will be an excellent resource for the ASME *Journal of Electronic Packaging* readers and subscribers and will help in stimulating new ideas and further their research in this vibrant and multidisciplinary field. Special thanks to the contributors and reviewers of the journal for their trust, patience, and timely revisions.

Satish Chaparala
Corning Inc.,
One Riverfront Plaza,
Corning, NY 14831

Ashish Gupta
Intel Corp.,
2200 Mission College Boulevard,
Santa Clara, CA 95054-1549

Mehdi Asheghi
Department of Mechanical Engineering,
Stanford University,
Stanford, CA 94305

Jeffrey Suhling
Department of Mechanical Engineering,
Auburn University,
Auburn, AL 36849

Toru Ikeda
Department of Mechanical Engineering,
Kagoshima University,
Kagoshima 890-0065, Japan

Xiaobing Luo
School of Energy and Power Engineering,
Huazhong University,
Wuhan 430074, China