Low Temperature Cu–Cu Bonding Technology in Three-Dimensional Integration: An Extensive Review

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1 Introduction

The concealed force behind the successful journey from information technology toward internet of things is the rapid progress in accommodating more functionality with a single silicon chip. This improvement in integrated circuit (IC) performance was primarily achieved by continuously scaling down the device dimensions as per Moore’s law. ICs have essentially remained as a planar platform throughout the period of rigorous scaling, in the sense that the devices and interconnects are in the same planar. Due to the fabrication of billions of transistors in an IC, the problem of interconnect has become more complex. Increase in the number of metal interconnect layers was a viable solution till recent past. Owing to the high density interconnects, their parasitic capacitances started dominating in ICs, and this resulted in an increased interconnect delay which significantly reduces the system performance. Off late, the interconnect delay has become on par with the transistor delay, if not more it has become a bottleneck in further scaling. The need of the hour is to look for an alternative in order to minimize the interconnect delay. One such prominent technology relies on exploring the third dimension, and it is popularly referred to as three-dimensional integrated circuit (3D IC) [1]. The concept of 3D IC integration was first anticipated in the year of 1980s [2]. It offers many benefits for future deep-submicron designs. Such benefits include: (1) resistance–capacitance delay is improved by vertical interconnection between adjacent stacking layers instead of wiring different functional blocks on a planar substrate; (2) interconnect wire length reduction results in enhanced performance and reduction in power consumption ability; (3) improved memory bandwidth leads to handling large amounts of multimedia data between packaged processors and memory; (4) realization of heterogeneous integration results in various new designs of high-end technologies like logic, memory, radio frequency, etc.; and (5) smaller form factor, which results in higher packing density, is also able to provide more functionalities within a smaller footprint which in-turn reduces the size, power consumption, interconnect resistance–capacitance delay, and manufacturing costs [3–7].

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The third dimension can be achieved in various stacking options like wafer-on-wafer bonding, chip-on-chip bonding, and chip-on-wafer bonding [8]. These integration schemes using vertical bonding along with through silicon via (TSV) become the preferred integration technique because of its ability to easily achieve precise alignment [9]. It can be achieved by metal-to-metal bonding, oxide-to-oxide bonding, polymer-to-polymer bonding, hybrid bonding, and flexible substrate-to-flexible substrate bonding [10–12]. Metal-to-Metal bonding is most preferable as it uses metals for stacking wafers, which helps in achieving an excellent electrical conductivity without compromising on the mechanical strength aspects. Among all the suitable materials for bonding medium, Cu is the potential choice due to its impressive electromigration resistance [13]. Besides that, it is a standard complementary metal oxide semiconductor compatible material, and if utilized as a bonding medium it can give enhanced electrical conductivity and ensures solid mechanical strength [14]. Furthermore, Cu–Cu thermocompression bonding is the preferred integration technique, which is simple and most preferable [13,14]. The basic mechanism of bond formation in Cu–Cu thermocompression bonding is the interdiffusion of Cu atoms and grain growth at the bonding interface due to simultaneous application of temperature and pressure [15]. In spite of all these advantages, the main bottleneck of Cu being a suitable bonding material for Cu–Cu is that it is easily reactive with ambient oxygen and hence it gets oxidized. Then, the oxide layer on Cu interconnects act as barrier for interdiffusion of Cu atoms and drastically reduces the contact resistance after bonding. Hence, for enhancing the diffusion of Cu atoms at the interface oxide layer on top of Cu surface needs to be removed prior to bonding. Apart from diffusion, surface roughness of Cu surface is also a critical requirement for high quality Cu–Cu bonding. Uneven Cu surface at the interface leads to void and mechanically unstable grain growth during Cu–Cu bonding. Hence, both the surfaces must be flat enough for intimate contact with mated wafers.

Instantaneous formation of oxide layer on top of Cu surface is one of the main reasons to accomplish high quality Cu–Cu bonding [16–18]. Above 200 °C, the oxide layer on top of the Cu surface becomes thermodynamically unstable and allows Cu atoms to diffuse during thermocompression cycle which leads to successful formation of grain growth at the bonding interface [19]. Furthermore, the impact of postbond annealing at various temperature was analyzed using cross-sectional transmission electron microscopy (XTEM) and high-resolution transmission electron microscopy (HRTEM) to understand the microstructure evolution of Cu–Cu bonding interface.
microscopy (TEM) analysis. The key inference from the postbond annealing enhances the interdiffusion which leads to enlargement of the grain growth up to 500 nm observed (Fig. 1) [19]. The requirement of high temperature and pressure not only enhances grain growth at the interface but also increases the bond strength. However, the need of high temperature and pressure during bonding cycle destructs the delicate Cu interconnects and reduces the IC interconnect performance. Therefore, there is a strong motivation to accomplish Cu–Cu thermocompression bonding at low temperature, and low pressure. This review paper focuses on various attempts made by researchers to achieve low temperature bonding, new methodologies to achieve low temperature and low pressure bonding, mechanism of bond formation, and current trends to achieve Cu–Cu bonding at lower thermocompression cycle.

2 Low Temperature Cu–Cu Bonding Development

2.1 Surface Activated Cu–Cu Bonding. Attempts have been made to prevent/modify the Cu surface in order to passivate from oxidation or remove oxide layer prior to Cu–Cu bonding. Suga and coworkers have proposed a novel technique to modify the Cu surface in order to remove oxide layer prior to room temperature Cu–Cu surface-activated bonding (SAB) [20]. Argon (Ar) bombardment by the use of Ar ion beam on the Cu surface cleans the oxide content on it, and SAB can be performed at lower thermal stress even at room temperature under ultra-high vacuum (UHV) [21]. However, the critical requirement of UHV during SAB makes the process complicated and costly.

In order to overcome these issues, an additional chemical mechanical polishing (CMP) step prior to room temperature Cu–Cu bonding was proposed elsewhere [22,23]. For which the prerequisite is atomically smooth surface and additional CMP step that makes the process complicated and costly.

2.2 Cu–Cu Bonding Based on Chemical Pretreatment. Again, Suga and coworkers suggested an alternative surface activation method to clean/modify the Cu surface using fluorine containing plasma prior to room temperature Cu–Cu bonding [24,25]. In this surface activation technique, O₂ or [O₂ + CF₄ mixture] gas plasma was used to activate Cu surface in a specially designed reactor (Fig. 2) [24]. The major concern of this activation technique is formation of quick oxidation of Cu surface due to

![Cross-sectional TEM images of bonded interfaces at different process conditions of annealing time](image1)

**Fig. 1** Cross-sectional TEM images of bonded interfaces at different process conditions of annealing time [19]

![Plasma reactor for Cu surface pretreatment](image2)

**Fig. 2** Plasma reactor for Cu surface pretreatment [24]
to the presence of oxygen gas for the creation of plasma. Current challenge of this technique is to make industry adoptable for low temperature Cu–Cu bonding.

Some researchers have proposed a technique of removal of native oxide from Cu surface by prebond cleaning step via wet chemistry. Employed chemistry for prebond wet cleaning includes: acetic acid [26,27], citric acid [28], sulfuric acid [29], hydrochloric acid [30,31], and also some other combinations. However, continued immersion of the Cu interconnect sample inside acidic solution may degrade the performance of underneath active devices. Therefore, wet chemical pretreatment may not be an ideal mechanism to clean Cu surface as per the standards of CMOS industry.

Based on the above reports, all the Cu–Cu bonding methodologies described so far have drawbacks. Precise prerequisite of atomically clean Cu surface and the stringent requirement of UHV are the major concerns of SAB. Further, wet chemical treatment of Cu surface is not always suitable for CMOS grade devices. Also requirement of specially designed plasma reactor for Cu surface treatment prior to bonding is more costly and not worthy manufacturing. At the end of the day, the main objective is to explore a simple CMOS compatible low temperature and low pressure Cu–Cu bonding technique.

2.3 Cu–Cu Thermocompression Bonding Using Passivation Mechanisms. The key factor in ensuring successful implementation of 3D IC technology is to explore a simple CMOS compatible low temperature and low pressure Cu–Cu bonding technique. Among all the methods, Cu–Cu thermocompression bonding is highly favored due to feasible postbond low contact resistance, better mechanical strength, and excellent hermetic seal. It can be achieved by properly passivating the Cu surface prior to bonding. The major issue associated with Cu–Cu thermocompression bonding is the formation of oxide layer on Cu surface at ambient condition as well as at higher temperatures. During bonding process, this native oxide acts a barrier and prevents interdiffusion of Cu across the interface, thus necessitating higher temperature and/or pressure for achieving a reliable bonding [32–35]. However, such higher temperature or pressure requirements for achieving quality Cu–Cu bonding may cause performance degradation, damage of underneath sensitive devices, and could potentially lead to reliability issues. Therefore, there is a strong need of low temperature and low pressure Cu–Cu stable and reliable bonding. Various researchers across the globe have suggested several techniques to prevent the Cu surface in order to passivate from oxidation prior to bonding.

2.3.1 Cu–Cu Thermocompression Bonding Using SAM Passivation. The necessary condition to attain reliable low temperature, low pressure Cu–Cu bonding primarily lies in the degree of preventing Cu surface from oxidation. One such technique proposed in the literature is to remove the surface oxide with high
energetic atom bombardment and bond the Cu surface immediately after the bombardment process at ultra-high vacuum at $7.5 \times 10^{-8}$ torr. These stringent requirements make the process complex and costly. Another method for achieving high quality Cu–Cu bonding is by smoothening the surface ($<1$ nm) using CMP. Ensuring such a low roughness every run is a highly demanding task.

Tan et al. proposed a non-UHV and noncorrosive method to passivate the Cu surface with self-assembled monolayer (SAM) of alkane thiol and its subsequent desorption just prior to bonding [36]. SAM is an organic monolayer which not only passivates the Cu surface completely but also enhances the efficiency of passivation [37]. SAM formed by linear alkane-thiol atoms ($\text{CH}_3(\text{CH}_2)_{n-1}\text{SH}$, $n = \text{number of carbon}$) are readily absorbed onto the Cu surface. The thiol (–SH) head bind to Cu and form packed monolayer on the Cu surface. The methyl (–CH$_3$) tail makes the surface hydrophobic. Another advantage of thiol-based SAM is to reduce already oxidized Cu layers to pure Cu along with passivation of the Cu surface from further oxidation. But complete removal of SAM layer may require temperature near to 250°C [38]. This high temperature desorption is a major constraint to use further reduction of bonding temperature. Furthermore, room temperature desorption of SAM was also proposed to achieve bonding at 200°C [39]. Indigenously designed nonthermal plasma reactor was used to create Ar plasma for complete desorption of the SAM just prior to Cu–Cu bonding. Plasma was generated at room temperature under atmospheric pressure. One concern of all SAM-based passivation mechanisms are ex situ and cannot be easily integrated with in-line CMOS process flow.

2.3.2 Cu–Cu Bonding Using Metal Passivation. The search for in-line CMOS flow compatible passivation process that is devoid of any wet processing or surface activation technique has led to the use of suitable metal as passivation layer. Chen et al. proposed co-sputtered Cu/Ti as bonded interconnects for 3D IC integrations [40,41]. Also diffusion mechanism of co-sputtered Cu/Ti-bonded structure was investigated. Ti was mostly found on the sidewalls and near to the substrate surface, after wafer level bonding at 400°C and postbonding annealing at 400°C for 1 h as shown in Fig. 3. However, high bonding temperature with a period of time does not meet the low temperature bonding requirement.

Inspiring from the co-sputtered concept, Chen and coworkers proposed a novel bonding method at 180°C using Ti as the passivation layer on Cu surface [42]. Moreover, the interdiffusion behavior of Cu through Ti passivation layer was explained and demonstrated using Auger electron spectroscopy [43]. Cu is known to have the lower activation energy at the surface and the smaller atomic volume (72 bohr$^3$) compared to Ti vacancy volume (75.48 bohr$^3$) [44,45]. Thus, Cu has a tendency to diffuse toward...
the bonding interface through Ti vacancies. If two wafers having Cu protected by ultra-thin Ti are brought together, the unoxidized copper diffuses through Ti toward the interface resulting in a Cu–Cu bonding. The thickness of Ti plays a key role in the complete process. Although a thicker Ti film can fully cover Cu surface, it may decrease the diffusivity of Cu in Ti thus require increased pressure conditions to achieve the bonding. Alternatively, very thin film may not able to passivate Cu. An optimum

![Modified Kelvin structure fabricated for electrical characterization and performed specific contact resistance curve at room temperature](image1)

![FIB image of two (111) nt-Cu films bonded at 150 °C for 1 h, FIB image of a randomly oriented Cu film bonded with a (111) nt-Cu film at 150 °C for 1 h, FIB image of two (111) nt-Cu films bonded at 200 °C for 30 min, FIB image of a randomly oriented Cu film bonded with a (111) nt-Cu film at 200 °C for 30 min, FIB image of two (111) nt-Cu films bonded at 250 °C for 10 min, and FIB image of a randomly oriented Cu film bonded with a (111) nt-Cu film at 250 °C for 10 min](image2)
2.5 bar [46, 47]. Furthermore, reliability assessments, with superior electrical performance compared to Ti passivation passivation layer thickness on Cu–Cu bonding quality, and subsequent bonding was performed with optimized Ti passivation thickness of 3 nm at 160\degree C and nominal contact pressure of 2.5 bar [46, 47].

Owing to the nature of fast formation of Ti oxides on surface, the contact resistance of Cu-bonded structure with Ti passivation cannot be kept as low as that from pure Cu\times Cu bonding. Therefore, searching for suitable metal species for Cu passivation with same diffusion behavior as Ti atoms becomes important. Chen and coworkers further reported that Cu–Cu bonding with Pd passivation could be demonstrated at low temperature (150\degree C) with superior electrical performance compared to Ti passivation [48, 49], as shown in Fig. 4. Furthermore, reliability assessments, including current stressing, temperature cycling, and unbiased highly accelerated stress test were demonstrated along with interdiffusion behavior [48]. All the metal-based passivation techniques proposed across the globe not only help in reducing the bonding temperature to below 200\degree C but also provides reliable and quality Cu–Cu bonding. While the major concern in the Ti-based passivation technique is its fast formation of oxides on surface, Pd passivation is a better option as metal-based passivation material. The schematic diagram of Cu-based bonding layer with metal passivation is shown in Fig. 5 [48].

2.3.3 Low Temperature Cu–Cu Bonding Using Metal-Alloy Passivation. For the passivation material on Cu surface, it is the best if the physical properties of passivation material can be close to Cu. Recently, authors have reported a novel passivation mechanism in order to passivate the Cu surface using Cu reach metal alloy, Constantan (copper–nickel alloy) and subsequent bonding was performed at sub 150\degree C with nominal contact pressure of 4 bar [50]. The advantage of Constantan is that its density is lower than that of pure Cu (Ni has higher atomic radius of 1.49 Å than Cu (1.41 Å)). Added to this, Cu is known to have lower activation energy at the surface [43]. Thus, under external stimulus such as temperature and pressure, constantan is not a hindrance for Cu diffusion. Mainly, passivation thickness plays major role to achieve high quality reliable bonding at thermal stress. The author has optimized the thickness of alloy on Cu surface and found to be 2 nm for high quality bonding. Furthermore, efficacy of Cu surface passivation using constantan alloy was demonstrated thoroughly. In addition, postbonding microstructure imaging analysis was demonstrated using cross-sectional TEM (XTEM) imaging. Presence of fine, indiffertiable bonding, and disappearance of interface clearly suggests Cu–Cu bonding with optimized constantan metal-alloy passivation is high quality and reliable [50] (Fig. 6).

Besides, specific contact resistance was measured by a modified Kelvin structure in order to reduce possible misalignment during bonding as shown in Fig. 7(a). The metal contact area of the Cu/constantan–constantan/Cu-bonded interface is 40 \mu m \times 40 \mu m with a pitch of 70 \mu m. The average specific contact resistance has been found to be 2 \times 10^{-8} \, \Omega \, cm^2 (Fig. 7(b)). Stability of the passivated Cu-bonded structure was demonstrated using current stressing, temperature cycling test, and relative humidity test, which suggest excellent stable bonding without electrical performance degradation [50].

2.4 Cu–Cu Bonding by Texturing Cu Crystal Orientation. It is reported that Cu surface diffusion coefficient on (111) oriented plane is faster (3–4 orders) as compared to other oriented plane at bonding interface [51]. Recently, Panigrahi et al. demonstrated an optimized Cu rich metal-alloy (Manganin) passivation technique that not only helps in passivate the Cu surface but also inherently enhanced Cu (111) oriented plane at the interface which results in high quality reliable bonding at 140\degree C [52]. Besides, Liu et al. proposed a novel surface modification technique to form nanotwinned Cu surface at the interface in order to enhance the diffusion capability during thermocompression cycle and subsequent bonding was performed at 150 \degree C with a nominal compressive stress of 0.69 MPa [53]. Also, microstructure behavior of the bonded Cu–Cu interface was examined using FIB imaging for different deposition conditions at different bonding conditions and different deposition conditions as shown in Fig. 8. It is very much evident from the figure that bonding time depends on bonding quality which means that bonding time can be further reduced by increasing the bonding temperature.
3 Fine Pitch Cu–Cu Bonding

3.1 General Requirements. In actual multilayer integration, we require copper pad-to-pad bonding with intermetal dielectric instead of simple blanket bonding. On-chip local interconnects require high density interconnects which needs to be realized by vertical bonding. Cu–Cu bonding has a promising scalability, and it can give <20 μm of pitch size. Lannon et al. reported a high density (50 μm pitch) Cu–Cu microbump bonding at 300 °C and 340 MPa of mechanical pressure using flip-chip bonder [54]. The samples were subjected to wet chemical pretreatment using sulfuric acid for surface oxide removal prior to bonding. There is a clear evidence of continuous connectivity between Cu bumps of both the wafers at 300 °C as shown in Fig. 9. They have also compared electrical and mechanical characterizations of both Cu–Cu microbump-bonded structure with Cu–Cu/Sn microbump-bonded structures. It was clearly proven that Cu–Cu bonds possess higher mechanical strength and electrical performance as compared to Cu–Cu/Sn microbump-bonded structures. The key message here is that Cu–Cu bonding is the right direction to proceed for fine pitching bonding as well. Flip chip bonding with bumps may not be an ideal solution due to their high temperature and pressure requirements.

3.2 Modified Tooling. Room temperature high dense bump-less Cu–Cu bonding was demonstrated using modified Flip chip bonder [55] under UHV condition (10⁻⁷ torr) with contact load of 20–25 kgf. Modified flip chip bonder was combined with the SAB process with 0.3 μm alignment accuracy for high dense and smaller pitch Cu–Cu bond pads. Further, Wang et al. explored that using a modified flip chip bonder to complete bonding process, which was performed in two steps using custom made separate chambers for each step [56]. As shown in Fig. 10, initially, Ar plasma pretreatment of the Cu surface was used in order to remove the native oxide in the pretreatment chamber. Subsequently, the samples were transferred into the bonding chamber for flip chip bonding. The complexity in this process is quite obvious and may be scalable to achieve high density interconnects. Moreover, flip chip bonding has a limitation of the number of layers which can be stacked vertically as bumps were used for interconnection [57].

3.3 Surface Passivation. Bump-less Cu–Cu bonding using damascene process flow as illustrated in Fig. 11 using SAM passivation was demonstrated at 350 °C temperature with 6.6–38.5 MPa pressure [16]. Prior to bonding, desorption of the SAM passivation layer was carried out at 250 °C. Finally, demonstration of high density Cu–Cu bonding daisy chain with 15 μm pitch is shown in Fig. 12.

Thermocompression bonding can achieve higher density and has minimal misalignment issues. Thus, achieving Cu–Cu fine pitch bonding using low temperature and low pressure thermocompression bonding is of great value addition. Panigrahi et al. demonstrated a novel optimized Cu rich metal-alloy (Manganin) surface passivation technique to protect the Cu surface from ambient oxygen and subsequent bonding was performed at low temperature (190 °C) and low pressure (4 bar) [58]. The obtained high quality infrared (IR) imaging of the bonded sample signifies good quality bonding between the Cu pads present on both the wafers, as shown in Fig. 13 [58]. Also, stability of the Cu/Manganin–Manganin/Cu pad-to-pad-bonded structure was using modified kelvin structure, and reliability assessment of this bonded structure was investigated under multiple current stressing, temperature cycling test, and the results indicate excellent stability without electrical performance degradation.

3.4 Concave-Pillar Design. Chen and coworkers recently reported a novel design to achieve low temperature Cu–Cu bonding utilizing pillar and concave on silicon substrate with and without polymer layer [59]. As shown in Fig. 14, during bonding, Cu pillar and Cu concave initially align and then first contact only at a tiny area, resulting in plastic deformation of the Cu structure. After the plastic deformation starts, bonding involved processes, such as recrystallization and grain growth happen until the whole bonded structure achieves a well-bonded and stable one. As shown in Fig. 15, this approach can successfully implement at sub 200 °C under atmospheric pressure. The latest published results from Chen and coworkers have demonstrated this structure can be
achieved by Cu–Cu bonding at 100 °C for a short time of 10 min [60].

4 Applications and Outlook for Low Temperature Ultra-Fine-Pitch Cu–Cu Bonding

Table 1 summarizes various Cu–Cu bonding technologies proposed/adopted by researchers and engineers. Current trend of Cu–Cu bonding is to decrease the pitch and the interconnect sizing for future 3D IC and heterogeneous integration technology. The target envisioned is to achieve the fine-pitch bonding for feature sizes less than 10 μm. Fine tuning of the entire process may be required to achieve low temperature and low pressure Cu–Cu bond having excellent electrical characteristics. One of the critical studies at that juncture would be to look at electromigration in addition to all the reliability tests. All the metal/metal-alloy-based passivation techniques may be extended to achieve wafer level ultra-fine-pitch Cu–Cu bonding with through silicon via integration. Again the process may need a fine or coarse tuning depending on the methodology adopted for TSV formation. The requirements and constraints of the both the technologies ought to be understood thoroughly before applying the proposed methodology for achieving vertical integration. In addition, a good alignment approach is important to achieve fine pitch Cu–Cu bonding [61]. Recently, for example, Sony has successfully fabricated a CMOS image sensor using Cu–Cu bonding technology [62]. The Cu–Cu-bonded vias are 3.0 μm wide and have a 14-μm pitch in the peripheral regions. Furthermore, Tezzaron semiconductor fabricated a next generation memory device, DiRAM4TM 3D memory which uses die-to-wafer Cu thermal diffusion bonding technology [63,64]. The 3D memory is low leakage, and very high density which makes memory device to operate much faster speed with lower power consumption in high performance logic process [65]. The above-mentioned applications using Cu–Cu bonding technology enables the benefits of small form factor, high-density pixels, and heterogeneous integration. It is believed that these goals will be the future trend of Cu–Cu bonding technology development as well.

5 Conclusions

In conclusion, this review paper describes the need for low temperature Cu–Cu bonding, new methodologies to achieve low temperature bonding, and current research trends to achieve low temperature Cu–Cu bonding for 3D IC and heterogeneous integration applications. Various techniques, such as surface passivation, surface cleaning, crystal orientation modification, and structural design, for low temperature Cu–Cu bonding blanket, and patterned structures are discussed. This review paper also discusses the current development trend and applications of Cu–Cu
Table 1 Comparison among various Cu–Cu bonding technologies

<table>
<thead>
<tr>
<th>Reference paper</th>
<th>Bonding temperature</th>
<th>Bonding pressure</th>
<th>Bonding vacuum</th>
<th>Approach</th>
<th>Short-comings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Takagi et al. [20]</td>
<td>Room temperature</td>
<td>1 MPa</td>
<td>$2 \times 10^{-6}$ Pa</td>
<td>SAB</td>
<td>Complex process and not manufacturing worthy; atomically smooth surface required</td>
</tr>
<tr>
<td>Tan and coworkers [26]</td>
<td>250°C</td>
<td>0.6 MPa</td>
<td>$1.8 \times 10^{-4}$ torr</td>
<td>Acetic acid wet prebond cleaning</td>
<td>Non-CMOS compatible and prolonged immersion can etch the Cu layer</td>
</tr>
<tr>
<td>Jang et al. [27]</td>
<td>350°C</td>
<td>2.5 MPa</td>
<td>$10^{-3}$ torr</td>
<td>Acetic acid wet prebond cleaning</td>
<td>Non-CMOS compatible, high pressure degrade the underneath device performance</td>
</tr>
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<td>Swinnen et al. [28]</td>
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<td>Not mentioned</td>
<td>—</td>
<td>Citric acid wet prebond cleaning</td>
<td>Non-CMOS compatible</td>
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<tr>
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<td>Not mentioned</td>
<td>—</td>
<td>Sulfuric acid wet prebond cleaning</td>
<td>Non-CMOS compatible</td>
</tr>
<tr>
<td>Chen et al. [30]</td>
<td>400°C</td>
<td>0.4 MPa</td>
<td>$10^{-3}$ torr</td>
<td>HCl prebond cleaning</td>
<td>Non-CMOS compatible and prolonged immersion may corrode the Cu layer</td>
</tr>
<tr>
<td>Chen et al. [31]</td>
<td>400°C</td>
<td>0.4 MPa</td>
<td>$10^{-3}$ torr</td>
<td>Native oxide clean by HCl</td>
<td>High temperature and pressure can have a detrimental effect on active devices also may cause performance degradation</td>
</tr>
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<td>Peng et al. [32]</td>
<td>350°C</td>
<td>200 KPa</td>
<td>Not mentioned</td>
<td>Diffusion</td>
<td>High temperature can damage the underneath CMOS devices</td>
</tr>
<tr>
<td>Saeidi et al. [33]</td>
<td>450°C</td>
<td>1.55 MPa</td>
<td>$10^{-1}$ mbar</td>
<td>Formic gas in situ preprocessing</td>
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<td>Diffusion</td>
<td>Excessive high pressure</td>
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<td>Tan et al. [36,37]</td>
<td>250°C</td>
<td>0.25 MPa</td>
<td>$7.5 \times 10^{-5}$ torr</td>
<td>SAM temporary Passivation</td>
<td>High temperature process may cause damage to active devices during multilayer integration</td>
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<td>Ghosh et al. [39]</td>
<td>200°C</td>
<td>0.45 MPa</td>
<td>$5 \times 10^{-6}$ mbar</td>
<td>Nonthermal plasma-based desorption of SAM</td>
<td>Residues of monolayer still observed</td>
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<td>Permanent passivation using Ti</td>
<td>High contact resistance</td>
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<td>$5 \times 10^{-5}$ torr</td>
<td>Engineered Permanent ultra-thin Ti passivation</td>
<td>Patterning using conventional etching technique (plasma etcher) and damascene process is difficult during real multilayer 3D IC integration</td>
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<tr>
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<td>Not mentioned</td>
<td>Permanent passivation using Pd</td>
<td>Comparable low contact resistance than Ti; Limited Applications</td>
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<td>$5 \times 10^{-5}$ torr</td>
<td>Engineered metal alloy (Constantan)</td>
<td>Very low contact resistance; Need more study prior to heterogamous</td>
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<td>$5 \times 10^{-3}$ torr</td>
<td>Engineered metal alloy (Manganin) surface passivation</td>
<td>Low temperature process; need more study prior to heterogamous integration applications</td>
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<td>Suga et al. [55]</td>
<td>Room temperature</td>
<td>2.45 MPa</td>
<td>$10^{-3}$ torr</td>
<td>Modified Flip chip bonder Fine-pitch bonding</td>
<td>Flip chip bonding approach</td>
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<td>6.6–38.5 MPa</td>
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<td>Ultra-fine-pitch bonding; SAM passivation</td>
<td>High temperature and high pressure process may cause damage to active devices during multilayer integration</td>
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<td>Chen and coworkers [59,60]</td>
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<td>Atmospheric pressure</td>
<td>Concave-pillar design prior to diffusion bonding</td>
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bonding. The implementation of Cu–Cu bonding using techniques described in this review paper could have a promising impact on existing 3D IC and heterogeneous integration.

References


