Electrical Demonstration of TSV Interconnects and Multilevel Metallization for 3D Si Interposer Applications

Erik Vick, Scott Goodwin, and Dorota Temple

RTI International
3040 Cornwallis Road, Research Triangle Park, NC 27709

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Abstract

A TSV test vehicle lot and 3D interposer demonstration lot were successfully fabricated and tested. Fabrication of the TSV test vehicle was accomplished using three process (mask) levels – front-side metal, backside TSV, and backside metal. The TSVs were formed using a vias-last approach with a nominal TSV size of 100µm, and an aspect ratio of 6:1. DRIE bottom clear process conditions were tested which produced 100% yield on TSV contact chains with up to 540 vias. In addition, optimum process conditions resulted in a TSV resistance of 29 mΩ, and sufficient TSV isolation resistance (> 1MΩ) for the target application. The interposer demonstration lot incorporated five front-side metal levels, one TSV level, and two backside metal levels. The first four metal layers (M1-M4), utilized 2µm Cu and 2µm oxide layers. Metal layers M2-M4 were fabricated using a self-aligned dual damascene process. Each wafer in the demonstration lot had 4 MLM contact chain test structures, with 26400 vias per structure. On two wafers, 100% yield was achieved on the MLM contact chains. For the dual damascene levels, average contact resistance per via was 4 mΩ. Functional testing was performed on two die from the demonstration lot (die size = 4 cm X 3.7 cm). Over 99% of the functional nets (circuit paths) passed. Yield on large area test capacitors, tested at wafer level, exceeded 80%.

Introduction

Relative to traditional chip-to-PCB packaging, solutions utilizing 3D Si interposers can have significantly higher I/O densities, resulting in reduced size, lower power consumption, and higher functionality [1]. One example of an advanced packaging application enabled by 3D Si interposers is an embedded computer module (ECM). The ECM utilizes a 3D Si interposer, or Si circuit board (SiCB), which enables mounting of bare die. Benefits of this advanced packing approach include (1) reduction in subsystem size by a factor of 2-3, (2) reduction in system power, and (3) elimination of on-die termination resistors due to the high impedance of the SiCB wiring. [2-3]

Advanced Si interposers require the integration of multi-level metallization (MLM), through-Si vias (TSVs), and backside metallization. For this implementation, TSVs were formed using a vias-last approach – TSVs formed from the backside of the substrate following completion of the front-side processing.

This paper will describe the process technology used to fabricate a 3D Si interposer designed for the above ECM/SiCB application. Additionally, electrical test results for TSV interconnect and MLM structures will be reported. Finally, functional test results from the ECM/SiCB demonstration lot will be presented.

Table 1:
3D Si Interposer Demonstration Process Flow

Side	Name	Film	Thickness
FRONTSIDE	M1	Ti/Cu/Ti	500A/2um/250A
	VIA 1	Si3N4/SiO2	7500A/2um
	TRENCH 1 (M2)	Ti/Cu	1000A/2um
	CAP 1	Ti	250A
	VIA 2	Si3N4/SiO2	7500A/2um
	TRENCH 2 (M3)	Ti/Cu	1000A/2um
	CAP 2	Ti	250A
	VIA 3	Si3N4/SiO2	7500A/2um
	TRENCH 3 (M4)	Ti/Cu	1000A/2um
	CAP 3	Ti	250A
	PASSIVATION	SiO2	1um
	FRONT UBM (M5)	Ni/Au	1.5um/3000A
BACK	TSV		
	BACK UBM	Ni/Au	1.5um/3000A
	BM1	Cu	4um

Experimental

For the above ECM/SiCB application, an electrical demonstration lot was fabricated and tested. The process technology for this demonstration integrated (1) five front-side metal levels, (2) one TSV level, and (3) two backside metal levels. A

brief description of the process flow is provided in Table 1.

Three of the metal layers, M2-M4 (see Table 1), were fabricated using a self-aligned dual damascene process. For M1-M4, the thick metal (2µm Cu) and dielectric (2µm SiO_2) layers were required to enable the design of signal lines with characteristic impedances (Z_0) of 50Ω. Figure 1 shows a cross-sectional scanning electron microscope (SEM) image of the completed front-side MLM stack.

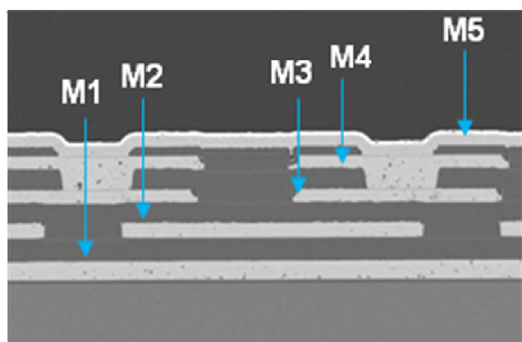

Figure 1:
SEM Image of 3D Si Interposer Front-side MLM

After completion of the front-side MLM fabrication, TSV and backside metal processing was completed. Figure 2 shows a cross-sectional SEM image of the fully fabricated 3D Si interposer.

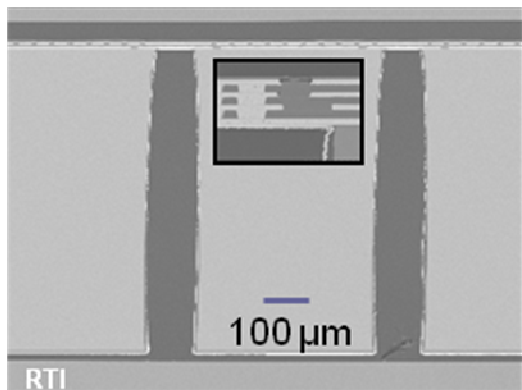

Figure 2:
SEM Image of Fully Fabricated 3D Si Interposer

As previously stated, TSVs shown in Figure 2 were formed using a vias-last approach, shown schematically in Figure 3. This approach enabled front-side processing on a standard, full-thickness substrate and elimination of wafer-thinning processes, which typically involve the use of carrier wafer technologies and techniques [4]. However, the vias-last approach does present some challenges, including (1) lower thermal budget for TSV/backside processing and (2) TSV bottom clear etch development. Also, forming vias in a full thickness wafer inevitably requires larger TSV dimensions due to aspect ratio (AR) limitations of the subsequent deposition and etch processes. However, when used in combination with wafer thinning, it has been shown that a vias-last process can support small (≤ 4µm) TSV dimensions [5-6].

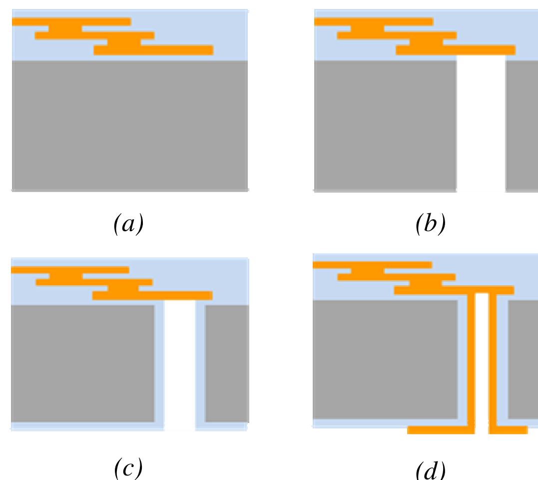

Figure 3:
Vias-Last Process Sequence – *(a) Front-side MLM, (b) TSV DRIE and SiO_2 Bottom Clear, (c) TSV Passivation and Bottom Clear, (d) TSV/Backside Metallization*

Since all steps used for backside processing were compatible with the lower thermal budget (<250ºC), the primary challenge was successful development and demonstration of the required TSV bottom clear etches. Bottom clear etches are required to remove dielectric/passivation films from the underside of the lower-most front-side metal (M1), which becomes the contact surface for the TSV metal. Two critical TSV bottom clear etches are used in the process flow shown in Table 1: (1) removal of the oxide layer under M1 and (2) subsequent removal of the TSV passivation layer from the backside of M1.

As shown in Figure 3, formation of a low resistance TSV interconnect requires complete removal of the SiO_2 and TSV passivation layer from the M1 surface. Clearing the SiO_2 from the bottom of the TSV was performed after the Si etch. Since the SiO_2 bottom clear process is highly selective to Si and extremely directional, longer over etch times can be used. Consequently, previously developed

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process conditions could be applied without further experimentation. However, process optimization of the TSV passivation bottom clear is critical. The TSV passivation bottom clear is performed after conformal deposition of the TSV passivation layer, as shown in Figure 3 (c). So, in addition to completely removing the TSV passivation layer from the M1 surface, it is equally important to minimize erosion (thickness loss) of the passivation layer from the TSV sidewall.

Particularly for the TSV passivation bottom clear, a highly directional (anisotropic) deep-reactive-ion-etch (DRIE) process is required. An isotropic (less directional) DRIE process will cause undesirable erosion of the sidewall passivation layer. One process parameter which can affect etch directionality is pressure. Also, since most DRIE processes have some lateral (isotropic) etch component, total etch time will affect the remaining thickness of the TSV sidewall passivation. Consequently, optimization of the DRIE process pressure and time is required to achieve the best possible electrical performance of the TSV interconnect. In order to optimize these DRIE process conditions, a short-flow TSV test vehicle was designed and fabricated.

Fabrication of the TSV test vehicle was accomplished using three process (mask) levels – (1) front-side metal (M1), (2) backside TSV, and (3) backside metal. The TSVs were formed using the vias-last approach shown in Figure 3, with a nominal TSV size of 100µm. The resulting TSV aspect ratio (AR) was 6:1, reflecting the use of a full thickness (625µm) 150mm substrate. The subsequent 3D Si interposer demonstration lot utilized the same TSV size and AR.

The abbreviated process sequence of the TSV test vehicle significantly reduced the fabrication cost and cycle time, while enabling process optimization using specifically designed TSV test structures. A more complete description of the justification and benefits of 3D (TSV) test vehicles can be found in reference [7].

For the TSV test vehicle, test structures included individual 4-wire TSV resistance structures, 2-wire TSV isolation structures, and 2-wire TSV contact chains (or TSV stitch strings using M1 and the backside metal as stitches). Versions of these test structures are shown in Figure 4. Test die included permutations of each structure with different TSV overlays of the front-side metal (M1) and backside metal. For these tests, the TSV size was fixed at 100µm.

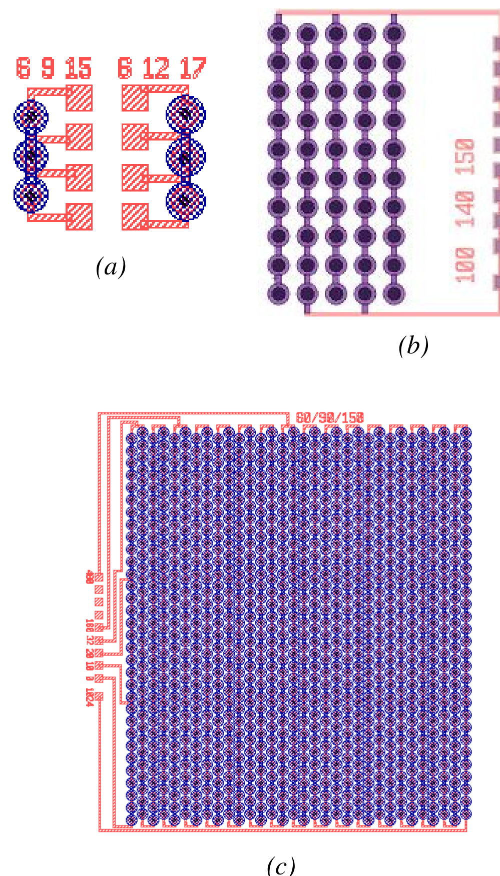

Figure 4:
Electrical Test Structures – *(a) Individual 4-wire TSV Resistance Structure, (b) 2-wire TSV Isolation Structure, (c) 2-wire TSV Contact Chain*

The experimental design of the TSV test vehicle lot is shown in Table 2. The design includes three process variables. One variable was the DRIE Si process. The DRIE Si etch was performed using a Bosch-type process [8]. Variation of the etch parameters was performed to attempt to alter the sidewall shape, leading to better electrical performance. Two DRIE Si etch processes were tested, labeled P1 and P2 in Table 2.

As previously discussed, for the TSV passivation bottom clear, process pressure and time were varied. The values (levels) of the bottom clear etch variables were selected based on past results, with the standard process conditions denoted as Std. Arrows pointing up (↑) indicate increases in the process value relative to the standard (Std) value. Alternatively, arrows pointing down (↓) indicate decreases in the process value relative to the standard.

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Table 2:
TSV Test Vehicle Experimental/Results Summary

Split		Process Description			TSV Electrical Characterization			TSV Chain Yield						
					I-V	I-V	4-wire	Yield vs. # TSV in Contact Chain						
Wafer #	Trial	DRIE Si	DRIE Bottom Clear Pressure	DRIE Bottom Clear Time	I @ 5V (A)	R @ 5V (Ohm)	Contact Resistance (Ohm)	10	20	42	126	210	378	540
V1	1	P1	Std	Std	1.0E-6	5.0E+6	0.051	100%	100%	100%	100%	80%	80%	80%
	2	P1	Std	↑	3.6E-6	1.4E+6	0.029	100%	100%	100%	100%	100%	100%	100%
V2	3	P1	↑	↓↓	2.1E-6	2.4E+6	0.050	100%	100%	100%	50%	50%	50%	25%
	4	P1	↑	↓	3.0E-5	1.7E+5	0.036	100%	100%	100%	100%	100%	100%	75%
V3	5	P2	Std	Std	9.8E-7	5.1E+6	0.049	25%	100%	75%	75%	75%	100%	75%
	6	P2	Std	↑	2.4E-6	2.1E+6	0.033	100%	100%	100%	100%	100%	100%	75%
V4	7	P2	↑	↓↓	1.0E-6	5E+6	0.060	75%	50%	25%	25%	25%	25%	25%
	8	P2	↑	↓	5.0E-6	1.0E+6	0.032	100%	25%	25%	25%	25%	25%	25%

Relative deviation from the standard value scales with the number of arrows shown. As shown in Table 2, two process time trials were performed on each wafer. This was accomplished by masking half of the wafer, while the other half of the wafer was processed for additional time.

Results and Discussion

The TSV test vehicle lot was successfully fabricated and tested. TSV leakage current was measured using the TSV isolation structures shown in Figure 4(b), but with 140 interpenetrating TSVs versus 50 as shown in Figure 4(b). Figure 5 shows the variation of TSV leakage (isolation) current for different passivation bottom clear processes. Also, the leakage current at 5V (maximum sweep voltage) is recorded in Table 2 in the column labeled “I-V I@5V” for all trials. The adjacent column to the right is simply the calculated isolation resistance at 5V.

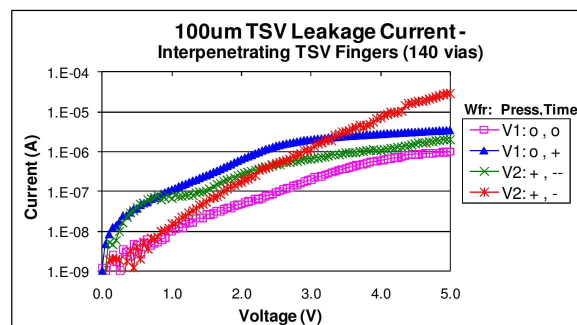

Figure 5:
TSV Leakage Current

In Figure 5, the notation of process variable levels has been modified: o denotes the standard (Std) level, + replaces the up arrow (↑), and – replaces the down arrow (↓). For simplicity, only the results from the P1 DRIE Si process split are shown in Figure 5, as the same correlation between process time and leakage current was observed for the P2 split. As can be seen in Figure 5, for a given pressure, leakage (isolation) current is higher for longer passivation bottom clear times.

The positive correlation between passivation bottom clear time and TSV leakage current has been observed on previous TSV test vehicle lots. As previously discussed, this correlation is attributed to increased loss of TSV sidewall passivation with increased etch times. Figure 5 also shows that higher pressures result in higher leakage current relative to the standard process. This occurs despite the relatively large drop in process time (--). When combined with the forthcoming yield analysis, this result tends to suggest that the loss in anisotropy due to increasing pressure is larger than increase in bottom clear etch rate. Nevertheless, for the target 3D Si interposer application, the leakage current for all trials shown in Figure 5 was considered sufficient. On-going efforts to improve TSV isolation will be discussed in the conclusion section.

Using the individual test structures shown in Figure 4(a), 4-wire TSV resistances were measured and the results summarized in Table 2 (labeled “4-wire Contact Resistance”). The DRIE Si etch split (P1/P2) was not significant. However, for a given pressure, the passivation bottom clear time had a statistically significant (p-value = 0.000111) effect on TSV resistance, with longer times resulting in lower TSV resistances. The average TSV resistance for all the trials with longer times was 33 mΩ, while the average TSV resistance for all trials with shorter times was 53 mΩ. Thus, independent of pressure (within the pressure range considered), longer passivation layer bottom clear times result in lower resistance TSV contacts. The longer times likely

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result in more complete clearing of the passivation layer from the front-side metal surface.

In general, higher pressure trials resulted in similar contact resistances, but lower yield, relative to the lower pressure trials. Also, increasing the time for the higher pressure trials resulted in higher leakage currents relative to the lower pressure trials, comparing V2:+,- to V1:o,+ in Figure 5.

In order to calculate yields using the data from the 2-wire contact chains, an equivalent circuit model was developed. The model is described in Figure 6.

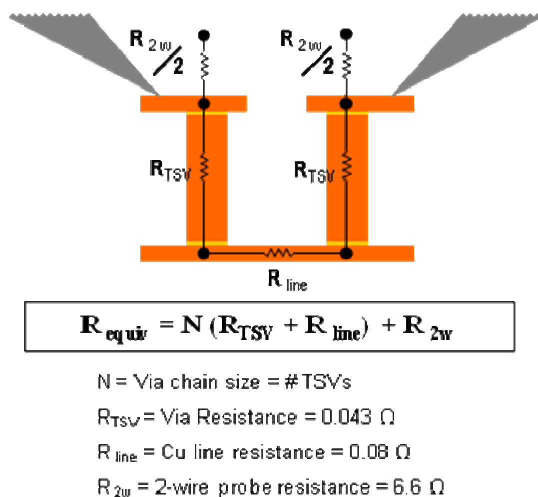

Figure 6:
TSV Equivalent Circuit Model

For this version of the TSV test vehicle, a full TSV contact chain had 540 TSVs, or a chain length of 540 (N = 540). As shown in Figure 4(c), TSV contact chains have taps at various intervals of the full contact chain. The contact chains include front-side wiring (including pads), front-side links, TSVs, and backside links. Figure 7 shows a plot of the 2-wire chain resistances versus the number of TSVs (N). Resistance plots are shown for the equivalent circuit model, **R** (equiv), and several actual TSV chains. The model and the plot show that the front-side wiring and links are the dominate resistance for small TSV chains. This result is consistent with previously reported results for TSV contact chains [9-10]. As shown in Figure 7, some chains closely approximate the TSV equivalent circuit model.

In order to generate TSV chain yields, an acceptable percentage deviation from the model was selected. This percentage is shown as error bars on the plot of **R** (equiv) in Figure 7. TSV resistances outside of this range were considered non-yielding. The results of this yield analysis are shown in Table 2. 100% yield on all TSV chains tested was achieved for the increased time trial on wafer #V1, or Trial 2. For Trial 5, the yield summary shows some anomalous values, with yield increasing from 25% to 100% from the first tap (N = 10) to the second (N = 20), respectively. Another increase is observed between N = 210 and N = 378. These anomalies are due to the resistance measurements on one die (#D). It is likely that these results were caused by process issues which affected the tap routing lines. The yield on #V4 was low due to the same problem, with a larger number of die affected.

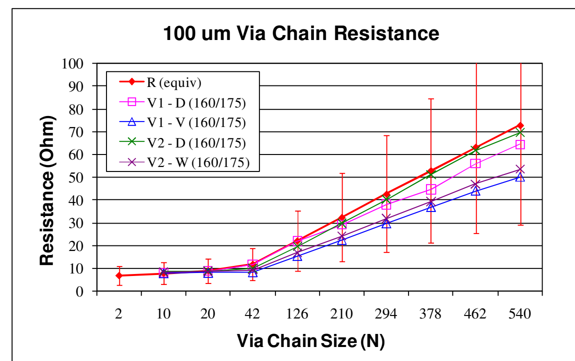

Figure 7:
TSV Chain Resistances Versus Size (N)

For choosing an optimum bottom clear process, leakage (isolation) current, resistance, and yield must be considered. As shown, TSV leakage current and yield have a positive correlation with process time, while TSV contact resistance has a negative correlation. For the process conditions tested, Trial 2 appears to result in the best overall combination of low TSV contact resistance, low TSV leakage current and high yield. The optimum bottom clear process conditions (Trial 2) identified by this experiment result in a TSV contact resistance of 29 mΩ.

These results closely approximate the 22 mΩ achieved on similar annular TSVs fabricated using a vias-first process [9-10]. Those structures had an annulus which was approximately 80μm with a constant annular width of 4μm. The vias were passivated with SiO_2, filled with chemically deposited tungsten, and thinned to thicknesses of 70-90μm.

The barrel-type TSVs fabricated for this test have some similarities to the annular TSVs described above. The 29 mΩ achieved on the vias-last process using full thickness wafers approaches the 22 mΩ achieved for similarly-sized annular TSVs fabricated

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using a vias-first process. This comparison suggests that vias-first and vias-last processes may be used interchangeably as dictated by the constraints and requirements of the target application.

Test die from wafer #V1 were subjected to temperature cycling tests designed to replicate the packaging (solder reflow) conditions required for the 3D interposer demonstration lot. The reflow cycling conditions used had a peak temperature of 225ºC for a maximum time of 75 sec. The temperature ramp was approximately 2-3ºC/sec. Figure 8 and Figure 9 show the results of the reflow temperature cycling tests on TSV contact resistance and TSV isolation resistance, respectively.

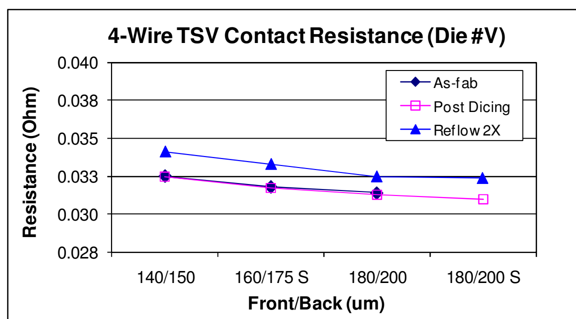

Figure 8: Reflow Cycling Test Results – Contact Resistance

On average, 4-wire TSV contact resistance increases approximately 0.6 mΩ per reflow cycle. TSV isolation resistance increases slightly with increasing number of reflow cycles. Additionally, for up to three reflow cycles, no TSV via chain yield loss was observed.

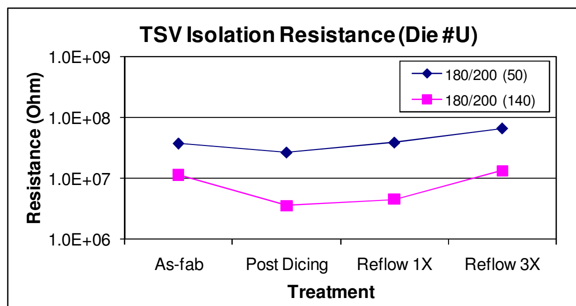

Figure 9: Reflow Cycling Test Results – Isolation Resistance

Subsequently, a 3D interposer demonstration lot was fabricated following the process sequence shown in Table 1. The 3D interposer demonstration lot used the best known processes from the TSV test vehicle lot and previous MLM short-flow development lots. Metal levels M2, M3 and M4 were fabricated using a self-aligned dual damascene process flow. One of the inherent benefits of the dual damascene approach is the ability to stack vias, as shown in Figure 1. Secondly, relative to oxide polishing, Cu chemical-mechanical-polishing (CMP) offers improved control of the dielectric thicknesses due to its higher selectivity (to underlying films) and more accurate endpoint. Finally, the dual damascene approach proved to have a higher tolerance to killer defects/particles, as will be shown.

Figure 10 shows the comparative yields for large area capacitors for several lots, all which incorporated at least two front-side metal levels. For reference, a theoretical yield curve is shown in Figure 9. The theoretical curve is based on a negative binomial model assuming a clustering parameter of 1 (a = 1) and a killer defect density of 0.1 defects/cm^2 [11].

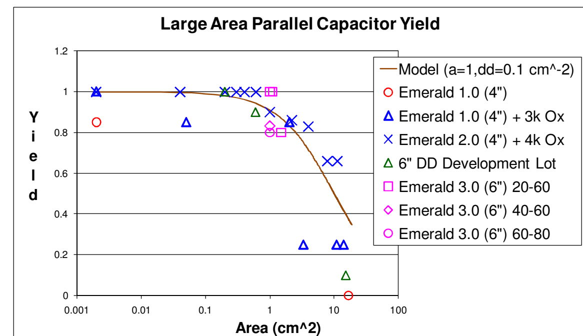

Figure 10: MLM Capacitor Yield

Capacitor yield on Emerald 1.0 (previous demonstration lot) was very low, even for the smallest capacitors. Emerald 1.0 utilized an oxide CMP planarization process. Killer defects from the underlying metal layer extended beyond the final thickness of the polished oxide, thereby resulting in shorts between the capacitor planes. An additional PECVD oxide layer was applied after oxide CMP which significantly improved the large area capacitor yields, as shown by data series labeled (1) Emerald 1.0 + 3kA Ox and (2) Emerald 2.0 + 4kA Ox. However, the oxide CMP process still resulted in excessively non-uniform oxide thicknesses, locally (within die) and globally (within wafer). Consequently, a self-aligned dual damascene short-flow process development lot (6" DD Development Lot) was fabricated and tested. The yield on this lot, which used 150mm instead of 100mm substrates, was comparable to that achieved with the oxide CMP with oxide overcoat process. With acceptable yield and improved control of dielectric thicknesses, the

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self-aligned dual damascene approach was chosen for the 3D interposer demonstration lot – Emerald 3.0.

As shown in Figure 10, large area capacitor yield for subsequent metal layers was approximately 80%. Some capacitors were designed using M2 (Level 20) and M5 (Level 60). These capacitors effectively had two inter-level dielectric layers (ILD) and yielded 100% on the device wafers (80% yield data point was a monitor wafer).

As shown in Table 1, the dual damascene metal layers (M2-M4) had a metal cap layer. For previous development lots, the polished Cu surface became significantly oxidized by the subsequent PECVD deposition step. The trench etch, which simultaneously opens the vias, can further oxidize the contact surface. Visual inspection showed that H_2 plasma treatments could be used to reduce the level of Cu oxidation at the contact interface. Despite the improved appearance of the Cu contact surface, contact chain yield was very low (7%), and contact resistance was high (for yielding chains).

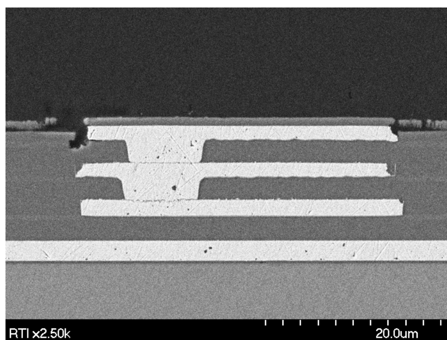

Figure 11: Cross-sectional SEM Image of Dual Damascene Contact With Cap Layer

In order to improve the quality of the contact surface, a cap layer was tested and implemented. Figure 11 and Figure 12 show cross-sectional SEM micrographs of dual damascene layers with and without the cap layer, respectively.

Comparing Figures 11 and 12, the Cu interface between dual damascene layers (top 2 layers in both cases) is significantly rougher without the cap layer (Figure 12). Results from a short-flow test run indicated better yield and lower resistance from MLM contact chains with the cap, versus without the cap. Accordingly, the cap process was implemented on the 3D interposer demonstration lot.

For the 3D interposer demonstration lot, each wafer had four MLM contact chain test structures, with 26400 vias per structure. The four structures correspond to contact chains between subsequent metal layers – M1-M2, M2-M3, M3-M4 and M4-M5. Total yield for the lot (5 wafers) was 70% for the contact chains. Two wafers accounted for 83% of the yield loss, which was attributed to an incomplete etch at the via level between M3 and M4. For two wafers, 100% yield for the MLM contact chains was achieved. For the lot, the average contact resistance per via was 4 mΩ.

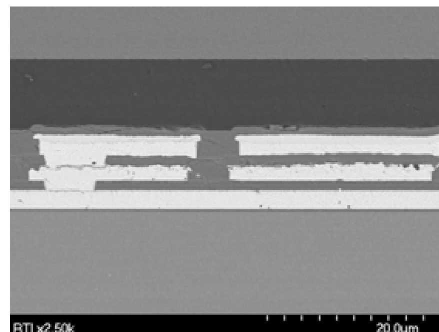

Figure 12: Cross-sectional SEM Image of Dual Damascene Contact Without Cap Layer

In addition to the previously described test structures, the 3D interposer demonstration lot had 5 functional die per wafer. The die size was approximately 4 cm X 3.7 cm. Functionality testing was performed on two die from the demonstration lot. Testing for continuity and isolation was performed simultaneously on the front-side and backside of the unpackaged die. For the two die tested, 9523 measurements were taken on 2067 nets. A net was defined as a metal line, or interconnect path, connecting different parts of the circuit. An example of a net would be the output of an FPGA to a pad. Many of the FPGA connections (nets) included a TSV.

On the first sample, 99.1% of the functional nets passed, showing acceptable continuity and isolation. Of the failures, 9 were opens and 10 were shorts to ground. On the second sample, 99.6% of the functional nets passed. In this case, all the failures were shorts to ground – no opens. Since the demonstration lot represented the first integrated lot with dual damascene MLM, backside TSVs, and backside metal, the yield results were considered relatively good. Additionally, the failures were largely consistent with known issues on the samples tested.

Conclusion

A TSV test vehicle lot utilizing a vias-last process with a 100µm nominal TSV diameter was successfully fabricated and tested. Bottom clear process conditions were tested which produced 100%

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yield on TSV contact chains with up to 540 vias, which was the maximum chain size designed. Average TSV resistance was 43 mΩ, with the optimum process conditions resulting in a TSV resistance of 29 mΩ. Also, it was shown that TSV leakage current and yield have a positive correlation with bottom clear process time, while contact resistance has a negative correlation.

For the TSV test vehicle, TSV isolation was sufficient (> 1 MΩ), but could likely be improved. On-going work includes optimization of the TSV profile (Si DRIE process) and evaluation of a thicker TSV passivation layer. Also, additional TSV test structures could be added to the next test lot design which may facilitate continued process optimization.

A 3D interposer demonstration lot was successfully fabricated and tested. The interposer demonstration lot incorporated (1) five front-side metal levels, (2) one TSV level, and (3) two backside metal levels. The first four metal layers (M1-M4), utilized 2μm Cu and 2μm oxide layers. Metal layers M2-M4 were fabricated using a self-aligned dual damascene process. On two wafers, 100% yield was achieved on four sets of MLM contact chains with 26400 vias – each set connecting subsequent metal levels. For the dual damascene levels, average contact resistance per via was 4 mΩ.

The 3D interposer demonstration lot had five functional die per wafer, approximately 4 cm X 3.7 cm. Functional testing was performed on two die, with over 99% of the functional nets (circuit paths) passing. Yield on large area test capacitors, tested at wafer level, exceeded 80%. While this yield was considered acceptable for the demonstration lot, continuous process improvement and defect reduction should lead to improved yield.

Acknowledgments

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