Low Temperature Direct Bond Technology for 3D Microelectronics Integration and Wafer Scale Packaging

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3D microelectronics integration and wafer scale packaging promise improvements in functional density and cost compared to conventional 2D microelectronics and packaging technologies. The realization of these improvements will require further adoption of 3D volume manufacturing process technologies. These process technologies will likely include through silicon via (TSV) and die or wafer bonding with and without 3D interconnect. Low temperature direct bond technologies have a number of inherent performance and cost advantages compared to other bonding technologies. This paper describes low temperature direct oxide bond technologies with and without a scalable 3D interconnect developed by Ziptronix and cost savings, performance and applications that will be enabled by adoption of these technologies. Enabled cost savings and performance include system or network-on-chip, system in package, and TSVs. Enabled applications include backside illuminated image sensors, micron-scale pitch vertically integrated image sensor arrays, 3D system-on-chip and 3D network-on-chip.

Key words: low temperature oxide bonding, 3D integration, DBI®, metal direct bonding, backside illuminated image sensors

1.0 Introduction

Continued improvement in the cost and functional density of semiconductor products relying on conventional 2D Moore's Law scaling [1] is reaching physical and economic limits [2]. Physical limits include transistor feature size approaching atomic dimensions and interconnect parasitics exceeding transistor drive capability. Economic limits are associated with the investment required to achieve these feature sizes and increasing cost of CMOS design and verification. 3D has emerged as a key technology to overcome traditional scaling limits and enable continued improvement in cost and functional density to meet customer requirements.

3D fabrication technology includes a variety of components like bonding, thinning, and through silicon vias (TSVs) that can be realized in different parts of the supply chain. The early embodiment of 3D technology has leveraged conventional die packaging technology. Examples include adhesives for die stacking [3], wirebonding for die interconnect [3], and flip-chip [4] and ball grid array for package-on-package (PoP) [5].

The dominant use of packaging technologies to implement 3D has led to System-in-Package (SiP) designation dominant in 3D technology roadmaps and inclusion of 3D in the Assembly and Packaging chapter of the International Technology Roadmap for Semiconductors [2]. Accordingly, 3D is typically characterized as an SiP, stacked die chip scale package, PoP, or package in package technology implemented downstream from CMOS wafer foundry fabrication. Unfortunately, this can result in neglecting some very interesting applications of 3D technology that improve cost and performance of conventional System-on-Chip (SoC) technology, i.e., 3D SoCs [6].

3D technology roadmaps have recognized the limitation of relying on evolving conventional packaging technology in fulfilling the potential of 3D technology [2]. For example, the need to develop and implement TSV or through silicon stacking (TSS) technology to achieve a high density, high bandwidth electrical interconnection through a silicon interposer or CMOS device(s) is well known. A significant level-of-effort has been expended throughout the industry in exploring a variety of different TSV types differentiated by where they are built in the supply chain and how they will be etched, isolated, and filled. Although some simple types of TSVs have made it into production in image sensors and MEMS, significantly more work is needed to establish industry standards for TSVs that include specification of bandwidth, crosstalk, power delivery, transistor proximity, stress/strain transistor effects, etc. and allow development of process design kits

that will allow optimum incorporation of TSVs in 3D products.

The bonding component of 3D technology has relied predominantly on adhesives for a mechanical connection and bumping for an electrical connection. Limitations of these technologies with regard to stress, distortion, interconnect pitch and post-bond fabrication compatibility will preclude realizing the full potential of 3D technology without general availability of an alternate bonding technology. This paper describes a low temperature direct bond technology developed by Ziptronix that overcomes these limitations and will enable the full potential of 3D technology to be realized. The description includes two different types of low temperature direct bond technology, a homogeneous bond that delivers a mechanical connection with minimum stress and distortion and a heterogeneous bond that further incorporates a submicron scalable 3D interconnect pitch. Variations of these direct bond types that will facilitate adoption in diverse manufacturing scenarios are included. Applications enabled by these attributes and the post-bond compatibility of this technology with CMOS wafer fabrication, assembly and packaging technology that will drive volume manufacturing adoption including backside illuminated image sensors, 3D SoC, 3D network-on-Chip (NoC), SiP, stacked die chip scale packages, and wafer level packaging are also discussed.

2.0 Low Temperature Direct Bonding

Low temperature (LT) direct bonding is an elegant bonding technology that allows two surfaces to be bonded together by simply placing them into contact without the use of an intervening material like an adhesive or solder. It is distinct from other types of direct bonding in that high temperature [7, 8], pressure [9, 10], or vacuum [11, 12] are not required to obtain high bond strength, suitable post-bond fabrication capability and final device reliability. Direct bonding can be implemented with a variety of material surfaces including silicon, silicon oxide, silicon nitride, or metal. Direct bonding can be homogeneous or heterogeneous. A homogeneous direct bond uses a surface with a single type of material and a heterogeneous direct bond uses a surface with multiple types of materials. Use of an insulating material surface like silicon oxide or nitride can be combined with via etch and metallization after a homogeneous direct bond to implement a 3D interconnect. Alternatively, a heterogeneous direct bond can deliver a high density of interconnections across the bond interface after alignment and placement of heterogeneous surfaces with photolithographically defined contact structures embedded in a dielectric matrix to each other [13]. This heterogeneous direct bond enables a scalable 3D interconnect density limited only by the accuracy with which these surfaces can be aligned and placed together. These attributes qualify this technology as a manufacturable solution to the limitations of adhesive and bump technology. These low temperature direct bond technologies are covered by a number of patents [e.g., 14-24] and patent applications. A detailed description of these technologies and how they can be manufactured is given below.

2.1 Homogeneous LT Direct Bonding

A homogeneous direct bonding with high bond strength can be achieved at low temperature with appropriate activation and termination of a bond surface prior to contact with another bond surface [25-30]. This stabilizes the bond surface prior to contact and enhances the kinetics of direct bond formation between the two surfaces after contact. Surfaces that can be bonded include insulators like silicon oxide, nitride, or oxynitride and semiconductors like silicon. Insulators can be of a variety of types including thermal, plasma enhanced chemical vapor deposition, and physical vapor deposition. The termination is effective in stabilizing the surface prior to contact such that surfaces can be placed together in a manufacturing ambient as opposed to requiring a specific environment for example vacuum. Adequate bond energies can be achieved by exposing only one surface if desired to minimize the cost of ownership of the process.

The primary requirements of the process are a low surface roughness, typically less than 0.5 nm, and low particulate contamination of the surface prior to contact that may otherwise prevent the surfaces from coming into intimate contact over the desired bond area. This surface roughness is well within the capability of industry standard chemo-mechanical polishing tools. Wafer-to-wafer implementation may be easier to implement than die-to-wafer or die-to-die implementations due to the lack of particles generated from die singulation and transport.

A variety of surface activation and terminations are possible. The optimum process depends on the pair of surface materials to be bonded and the post-bond fabrication and product requirements. A common material combination pairing is silicon to silicon oxide or silicon oxide to silicon oxide, where the silicon typically has a native oxide with thickness on the order of a few nm. A nitrogen plasma activation and termination process is particularly effective for these bond pairings. A wide variety of plasma conditions are possible including a very slight etching of the surface and avoiding a

significant increase in surface roughness. Note that although other plasma process gases like argon and oxygen can be used, a nitrogen termination will typically result from residual air or nitrogen in the plasma chamber when the plasma is initiated. This has been verified with secondary ion mass spectroscopy (SIMS) profiles of nitrogen at the bond interface for these types of bond pairs and a variety of plasma processes and pump down times. An example of detecting nitrogen bond surface termination with a SIMS profile is given in Figure 1 for a silicon oxide to silicon oxide bond. Note verification of the bond interface location with a boron signal expected from pre-bond boron surface contamination [31].

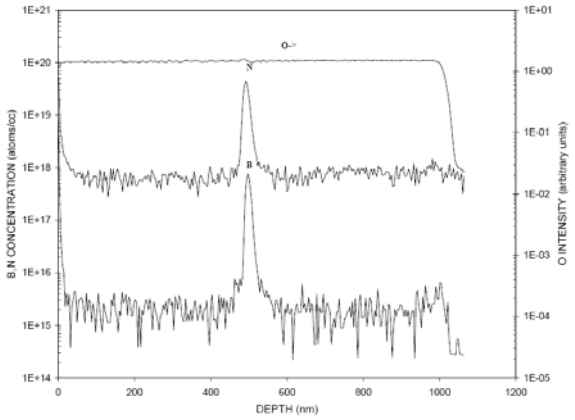

Figure 1 – SIMS measurements of nitrogen and boron concentration at a silicon oxide to silicon oxide low temperature direct bond interface indicating a nitrogen terminated surface prior to bonding.

Bond energies in excess of the 2.5 J/m^2 silicon fracture energy can readily be obtained at low temperatures, for example 100°C, with this type of process. 1 J/m^2 at room temperature can also be routinely achieved. This high bond energy at low temperature performance is critical for applications that require bonding of materials with high coefficient of thermal expansion mismatch [25], a low stress bond, or low thermal budget to minimize degradation of strain engineering. An assortment of tools are available to implement this process in a volume manufacturing environment including tools for plasma activation and/or termination, cleaning and/or termination, and aligning/placing a prepared bond surface to another (prepared) bond surface, in discrete and cluster [32, 33] configurations.

2.2 Heterogeneous LT Direct Bonding

Heterogeneous LT direct bonding includes at least two different types of bond components [26-30, 34]. The first bond component is insulating and can be of the homogeneous type described above, for example silicon oxide to silicon oxide or silicon nitride to silicon nitride. The second bond component is conducting and can be any one of a variety of types including direct, fused, alloyed, or soldered. A direct conductive bond is a low temperature bond where two materials, for example metals like nickel, copper, gold, etc., are placed into direct contact resulting in a direct bond and an electrical connection. A fused bond is a similar to a direct conductive bond except that sufficient heat is applied after contact to cause fusing, melting, grain growth, etc. of the opposed metals. Likewise, an alloyed or soldered bond is one where an alloy or solder, respectively, is used to form the conductive bond and electrical connection. The first insulating bond component may also include a bond between an insulator and conductor, for example silicon oxide to metal, that arises from a misalignment after placing two surfaces together, one with a particular silicon oxide and metal pattern and the second with its mirror image.

Key attributes of this heterogeneous bond are high bond strength between both conducting and insulating components and eradication of an external pressure requirement to obtain the heterogeneous direct bond with a scalable 3D interconnect. This provides significant cost of ownership (CoO) manufacturing and performance advantages compared to other bond technologies like copper thermo-compression (CuTC) [9, 10]. For example, a CuTC bond requires a long temperature and pressure cycle in an expensive single wafer tool that can be a significant CoO expense. Furthermore, a patterned CuTC bond has copper raised above the bond surface to facilitate generating adequate pressure at the copper-copper bond interface when external pressure is applied during the bond cycle. This results in a lack of surface contact and bonding in places where copper on one surface is not opposed to copper on the other surface. This causes a significant reduction in bond area, and corresponding reduction in bond strength, compared to the heterogeneous low temperature direct bond with bond area over the entire surface.

This reduction in bond area for CuTC is particularly severe when bonding very fine pitch features to build, for example, a scalable 3D interconnect. For example, Figure 4 shows the reduction in bond area for a CuTC bond relative to unity for a heterogeneous direct bond assuming an array of copper posts with a half-pitch diameter and 1, 2 and 3 micron pitch. This figure indicates that even with perfect alignment, CuTC is at an 80% or factor of five bond area disadvantage compared to heterogeneous low temperature direct bonding.

Furthermore, very slight misalignments significantly increase this reduction, with much greater sensitivity at smaller pitches.

This heterogeneous LT direct bond can be built by preparing a heterogeneous surface consisting of dielectric, for example silicon oxide, silicon nitride, or silicon oxynitrides, and metal, for example, copper, nickel, tungsten, aluminum, or gold. This surface can be prepared in a variety of ways. Two of these methods, post planarization and damascene, are outlined below.

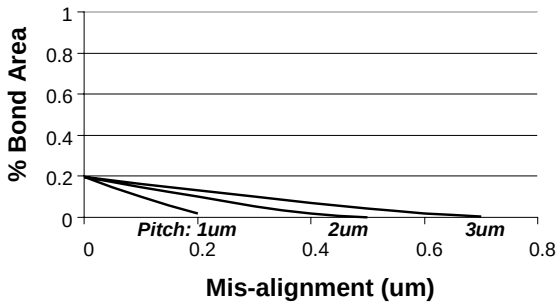

Figure 4 – Percent bond area relative to the entire surface for a CuTC bond of an array of 0.5, 1, and 1.5 micron diameter copper posts on a 1, 2, and 3 micron pitch, respectively, as a function of misalignment between copper posts on respective bond surfaces.

The key steps for the post planarization method are forming a DBI® metal post, for example by patterned electroplating on a seed layer using a photoresist mask, followed by isolation of the DBI® posts by etching the seed, followed by dielectric deposition and CMP of the oxide and metal. The key steps for the damascene method are deposition of the dielectric, cut to last metal, followed by conductive barrier deposition, metal fill and CMP. Details of the CMP specification for these processes including dielectric and metal surface roughness and dielectric to metal planarity are available from Ziptronix [35]. Industry standard CMP pads and slurries have been used to meet this specification with these methods for a variety of dielectric and metal combinations including silicon oxide with nickel and silicon nitride with copper. The silicon nitride with copper combination provides reliable encapsulation of the copper with a barrier including bond misalignment as shown in Figure 5.

The conducting component(s) can be planar, recessed, or raised relative to the insulating component(s). The non-planarity that can be accommodated depends on parameters of the material being bonded, for example thickness and Young's modulus, and can be on the order of 10 nm. When the conducting component is recessed or dished below the surface of the insulating component, a 3D interconnect may not be realized spontaneously after aligning and placing heterogeneous surfaces into contact. If necessary, application of a low temperature increment may be used to expand the conducting component relative to the insulating component, effectively extruding the conducting components and creating sufficient internal pressure at opposed conducting components resulting in a direct conducting bond. The internal pressure required depends on parameters of the conducting components including Young's modulus and residual native oxide, if any. A high bond energy at low temperature direct bond insulating component will prevent expansion of the conducting component from separating the insulating components without application of external pressure and result in a reliable conductive bond.

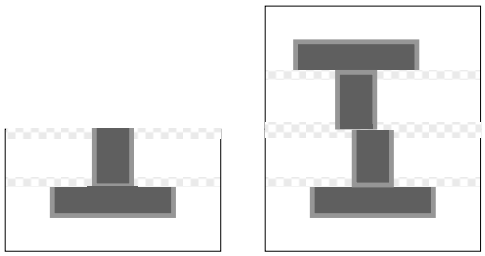

Figure 5 – Cross-section schematic of copper DBI® a) before and b) after bonding with misalignment showing copper fully enclosed by a conducting or insulating barrier.

The nomenclature of this heterogeneous low temperature direct bond technology has predominantly been referred to as Direct Bond Interconnect and has been registered with the United States Patent and Trademark Office as DBI®. It has also been referred to as metal/silicon oxide hybrid bonding [30], and metal direct bonding [36]. It will be referred to as DBI® for the rest of this paper.

3.0 Volume Manufacturing Adoption

There are a number of requirements for a new technology to be adopted for volume manufacturing. These relate to the cost, ability to manufacture, expected lifetime, and compatibility with other technology elements. The satisfaction of these requirements by DBI® and low temperature oxide bond technology are described below.

3.1 Tool Set

The tool set required to implement these technologies is essentially what has been used for BEOL manufacturing for a number of years. The

primary exception has been tools to align and place wafers or die together with sufficient accuracy to achieve a desired 3D interconnection pitch. Recent announcements by tool vendors of better than 0.5 micron, 3σ accuracy on 300mm wafers [32, 33] indicate availability of all tools required to build a 3D interconnect with a micron scale pitch.

3.2 Scalability

The superior planarity of DBI® compared to other 3D interconnect bond technologies enables scaling to micron scale interconnect pitch [28] and below without an unacceptable drop in bond strength as indicated in Figure 4. Adoption of DBI® thus has the potential to render competitive technologies obsolete and last for many years once adopted.

3.3 Reliability

The potential reliability of DBI® has been demonstrated with serial connection test structures of up to 1,000,000 3D interconnections and connection pitch down to 8 microns that have passed JEDEC temperature cycling and HAST tests [26, 28]. Reliability results from a variety of CMOS prototypes and test vehicles are pending.

5.0 Compatibility with other Technologies

DBI® is fully compatible with CMOS and other 3D technologies including aluminum and copper BEOL, TSVs and die or wafer bonding configurations as described below.

5.1 BEOL Compatibility and Integration

DBI® is fully compatible with both aluminum and copper back-end-of-line (BEOL) used in CMOS manufacturing. An example of copper/low k compatibility is given by the SEM cross-section micrograph in Figure 6 which shows 10 micron pitch nickel/silicon oxide DBI® of a silicon test wafer to a 65 nm, 12 level metal, copper/low k BEOL field programmable gate array (FPGA) wafer. Comparison of on-wafer test before and after DBI® indicated no FPGA degradation as a result of DBI®.

The reliance of both CMOS BEOL and DBI® planarization on CMP suggests DBI® surface planarization can be easily adopted into the CMOS BEOL. This will enable a low CoO by leveraging the substantial CMOS BEOL planarization investment. It would further result in a very low CoO for subsequent downstream DBI® bonding requiring only surface preparation, alignment and placement. For example, this cost has been calculated to be only $12 for DBI® bonding compared to about half that for adhesive bonding and a factor of five less than CuTC bonding [37]. An example of straightforward adoption of DBI® planarization into aluminum BEOL is terminating the BEOL with a "last via" layer where the traditional tungsten plug CMP is replaced with a nickel plug CMP. An example of straightforward adoption of DBI® planarization into copper BEOL is terminating the BEOL with a copper single damascene shown in Figure 5.

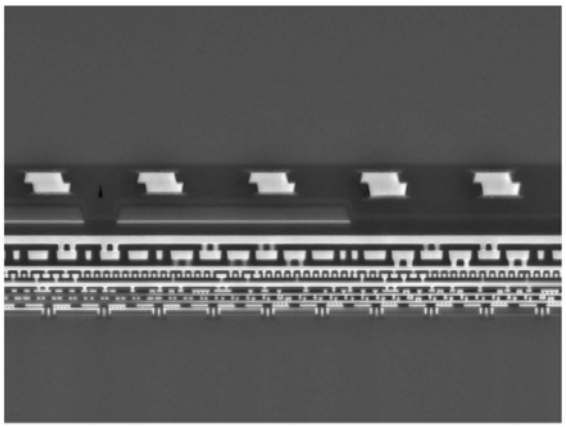

Figure 6 – Scanning electron micrograph cross-section of 10 micron pitch nickel DBI® 3D interconnecting 65nm, 12-level metal, copper/low-k FPGA CMOS wafer to silicon test wafer.

5.2 TSV Compatibility

DBI® is also fully compatible with the wide variety of TSV technologies in development throughout the industry. This includes TSVs fabricated before and after bonding, TSVs filled with copper, tungsten or nickel, TSVs isolated with organic or inorganic dielectrics, and TSVs exposed from the BEOL and/or substrate side of the CMOS. Various attributes of DBI® enable this compatibility. For example, the ability to use an industry standard BEOL dielectric to obtain high bond energy at low temperature simplifies TSV etch and fill through the bond interface. The low temperature capability is further compatible with organic TSV isolation. Furthermore, the flexibility of using various metals for the DBI® conducting bond facilitates compatibility with various TSV metals. Finally, the DBI® planarization specification is compatible with thinning technologies used to reveal TSVs built into the silicon substrate by the CMOS foundry prior to BEOL fabrication, also known as "vias first" or "vias middle" [38]. Note that this type of TSV does not extend through all BEOL metal layers, resulting in a shorter TSV and minimizing BEOL routing exclusion for lowest TSV CoO and highest performance [26].

5.3 Die vs. Wafer Bonding Compatibility

The low temperature DBI® and direct oxide bond technologies are compatible with bonding wafers and/or die. For example, wafer-to-wafer, die-

to-die, and die-to-wafer configurations are possible. This flexibility is an advantage because different applications will require different configurations. For example, applications wherein a 3D architecture benefits from a 3D partitioning into two or more layers where the die areas in the layers are similar, the yield of these die areas is high, and the wafer size of these layers is the same may benefit from wafer-to-wafer bonding. Conversely, applications wherein the 3D layers have significantly different die size, utilize different wafer sizes, or have low yield may require die-to-wafer or die-to-die bonding.

Die-to-wafer or die-to-die bonding is accommodated by singulation between planarization and alignment/placement. The low temperature surface activation/termination can be implemented before or after singulation.

6.0 Applications

There are a variety of applications for the DBI® and direct oxide bond technologies. In general, these applications can be implemented in a wafer-to-wafer, die-to-wafer, or die-to-die configuration. However, various aspects of these applications will likely dictate a preference for a particular configuration. Applications are thus categorized as wafer or die bonding, however these applications are not limited to this categorization.

6.1 Wafer Bonding

Applications in which bonding wafers have various advantages over bonding die include image sensors, 3D SoC/NoC, TSV aspect ratio reduction, and wafer scale packaging.

6.1.1 Image Sensors

CMOS image sensors are typically comprised of a 2D array of pixels surrounded by control circuitry. Scaling of the pixel pitch is important for mobile applications like cell phones where higher megapixel counts for improved resolution at minimum cost are desired without increasing the form factor or socket size of the device. Scaling of conventional frontside illuminated image sensors is problematic below the 1.7 or 1.4 micron node due to limitations associated with illuminating through the multi-level BEOL interconnect. A solution is to bond the frontside of the image sensor wafer to a silicon handle wafer then thin the CMOS substrate to enable illumination directly on the silicon detectors from the backside. This backside illuminated sensor (BIS) configuration will enable pixel scaling to submicron pitch in addition to improved low light sensitivity.

Conventional adhesive bonding has been used for BIS in applications like camcorders and digital still cameras where low light sensitivity is a larger driver than pixel scaling. However, for applications like cell phones where pixel scaling is paramount, the adhesive cure cycle adds stress and distorts pixels precluding adequate stepper alignment for color filter array fabrication after backside thinning. The high bond strength at low temperature capability of low temperature direct oxide bonding eliminates this stress induced distortion and enables submicron pixel scaling.

Image sensors with higher megapixel counts and reduced die size and cost than BIS bonded to a silicon handle wafer are possible using a 3D architecture with a pixel layer DBI® bonded to a control circuitry layer. This can result in die size reduction up to 50% subject to relative pixel and control circuitry areas. Significant cost savings is also enabled due to smaller die size in the constituent layers and use of less expensive CMOS for separate pixel and control circuitry layers compared to a complex pixel/control circuitry process. The inherent scalability of DBI® will enable these advantages to be realized while scaling to submicron pixel pitch.

6.1.2 3D SoC and NoC

Conventional SoC or network-on-chip (NoC) add mask layers and increase die size to achieve system or network level functionality. This results in increased cost due to more process steps and lower yields. A 3D SoC/NoC achieves improved 2D interconnect at significantly reduced die size and potentially lower cost, by partitioning the design into multiple layers that can be built in different CMOS nodes and then 3D interconnected with DBI®. The potential for reduced process cost is dependent on yield curve and process cost of the partitioned process nodes compared to the conventional SoC/NoC. Image sensors are an example of a simple SoC that can benefit from this partitioning as described above. More complex SoCs and NoCs may have a greater benefit, especially at large die size, subject to thermal limitations.

6.1.3 TSV Aspect Ratio Reduction

TSVs are a key component of 3D technology. Unfortunately, they have a number of characteristics that complicate adoption. For example, a high aspect ratio is preferred to minimize exclusion and impact on silicon strain engineering. In addition, TSV parasitics can limit critical signal path bandwidth. These TSV liabilities can be alleviated with some bonding configurations, for example wafer frontside to wafer frontside. Examples of applications suitable for this configuration are image sensors and SoC/NoCs described above. This configuration can utilize the

high density, low parasitic DBI® interconnect from the lower wafer BEOL to the upper wafer BEOL. The upper wafer can then be thinned to a thickness limited by the upper wafer active silicon, followed by a pad cut and wirebond or underbump metallization and bumping prior to packaging. TSV interconnections between the two wafers are thus eliminated and the only TSV connections are between the upper wafer and the package. The number and pitch of these TSVs will generally be much less than the connections between the wafers. The TSVs can also be built with a less expensive, lower aspect ratio, unfilled TSV with low parasitics.

6.1.4 Wafer Scale Packaging

Wafer scale packaging or wafer level chip scale packaging (WLCSP) offers reduced package cost by packaging all die on a wafer in a single process with a minimum package footprint slightly larger than the die size. WLCSP can require bonding cavities in a wafer or bonding in vacuum for applications like MEMS.

Low temperature oxide bonding and DBI® are compatible with many WLCSP applications. For example, low temperature oxide bonding has been shown to be MIL-883E compliant [25]. DBI® has the potential of more stringent hermetic performance with a metal bond. DBI® can also easily support the increasing demand for finer pitch package interconnects.

6.2 Die Bonding

The primary application discussed in this paper where bonding die is advantageous is SiP.

6.2.1 SiP

A SiP application is one in which a variety of die of various functions are thinned, bonded, and interconnected with the goal of achieving the highest functional density at the lowest possible power and cost, for example mobile phones. Die-to-die or die-to-wafer is preferred for this application due to disparate die size and supply chain considerations like implementing known good die strategies and management of multiple vendors supplying the SiP.

Early SiP solutions were implemented with conventional thinning, adhesive die stacking, wire bonding, and bumping. Further optimization of the SiP will require incorporation of TSVs in aggressively thinned die to enable improved architectures with increased number of connections and bandwidth of these connections between die with minimum thickness. These TSVs can be built, for example, by the CMOS wafer foundry into the substrate before the BEOL, subsequently interconnected to Metal 1 of the BEOL, and subsequently revealed by die thinning, or downstream of the foundry after the die are thinned. The die are typically thinned in wafer form when mounted to a temporary handle wafer to allow aggressive thinning without breakage.

A variety of conventional non-planar interconnect technologies including bumping and copper pillar have been explored to build an areal interconnect on these exposed TSVs that can then be used to interconnect to other die when stacking. The fabrication steps for these interconnect schemes may be built with the temporary handle wafer to minimize breakage which is removed prior to singulation and die stacking to allow reuse of the handle wafer. Die stacking of the resulting die can be problematic due to stress in the thinned, singulated die that induces significant warping. Non-planarity of bumps, copper pillar, or other conventional interconnect further complicates achieving high yield, reliable stacking with a minimum die thickness due to a lack of uniform support over the entire die area.

DBI® die-to-die or die-to-wafer technology avoids these limitations with a planar surface that provides a uniform bond with adequate strength to avoid warping when placed on another die. DBI® compatibility with various TSVs and low planarization thermal budget allows DBI® planarization after revealing TSVs with thinning or building TSVs into thinned die while temporarily bonded to a handle wafer.

7.0 Summary

Homogeneous and DBI® low temperature direct bonding have numerous advantages including reliable low temperature bond energy, scalable 3D interconnections and low CoO. These technologies are compatible with CMOS and other 3D technologies and are well suited for manufacturing adoption. Adoption of these technologies will deliver performance and cost advantages in image sensor, SoC/NoC, and SiP applications.

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