Reliability Modeling to Enable Damage Assessments for Plated Through Holes

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Abstract:

A modeling approach to assess the reliability characteristics of the copper used in printed circuit boards (PCBs) is presented. Plated Through Holes (PTHs) for electrical connections across PCBs are formed by drilling the PCB and electroplating the hole, often using a copper (Cu) finish. Although the mechanical strain on the Cu in the center of the PTH may be insignificant to disrupt circuit functioning in a single reflow soldering cycle, more substantial damage accrues over multiple reflow cycles. Loads applied after the reflow cycles are shown to contribute to subsequent mechanical disconnects.

Efforts to quantify the damage to the Cu are hindered by the difficulties of measuring direct strain or displacement inside a PTH and extrapolating the damage to the Cu in the first three reflow cycles.

The assessment of damage to the Cu is enabled by finite element analysis. The authors' finite element model is defined as a single load system based on PTHs with flanges on every side of the laminate board connected by a hollow cylinder, a configuration treated as symmetric from the center of the board. The critical area of focus is the inner ring of the PTH. Stress and strain measurements in the region of interest are obtained using numerical simulations. The two-dimensional axi-symmetric model is validated against a three-dimensional full model and several test cases.

Reliability assessments relying on undamaged circuits are shown to be less accurate than estimates incorporating Cu damage following three reflow cycles. An increased probability of intermittent connection for the PTH's remaining use is suggested. Accordingly, the authors propose that damage assessments of copper finishes be incorporated into models of PCB reliability.

Key words: Plated Through Hole (PTH), Printed Circuit Board (PCB), reliability, hysteresis, reflow cycles, lead-free electronics, finite element modeling

Introduction:

Electronic assemblies are complex systems composed of many parts. Each part of an assembly introduces potential failure modes and alters the overall reliability of the system. The effect of any single component on the overall reliability of a system is dependent on the location of the component in the chain of use. The reliability of Plated Through Holes (PTHs) has a direct effect on the aggregate calculation of board-level reliability because PTHs are incorporated into the Printed Circuit Board (PCBs) before any components are soldered to the board.

The reliability of PTHs is also critical because it is infeasible to replace them upon failure; a failure may result in the entire board being scrapped or discarded. One of the failure modes for PTH results from thermal cycles due to a mismatch between the Coefficients of Thermal Expansion (CTEs) of the copper and the board laminate. A board may undergo several reflow cycles before it is installed in a system and begins regular use. A reliability model must account for the damage in the PTH in order to be comprehensive and accurate. The objective of this study is to model the system and provide a framework for modifying the reliability assessment of electronics assemblies by incorporating these damage considerations.

Investigation:

Attempts to produce a comprehensive reliability assessment of PTHs confront several mechanical issues that are best explored analytically. For example, it is impossible to take direct stress and strain measurements inside the copper of the PTHs. Additionally, the characteristics of PTHs vary widely depending on the intended application of the PCBs to which they are incorporated. The copper metallization can have several thicknesses, lengths, radii, and flange sizes. Various materials are used for

the PCBs, each of which has its own thermal properties, including CTE.

A high degree of variability exists in the temperature of the board during both assembly and subsequent use over its lifecycle. The reflow process will heat up the entire board assembly to the same temperature and each PTH is exposed to the same temperature cycle. In regular use, the board will experience varying temperatures and mechanical stresses at different locations. The assumption that the board starts with no damage to any of its components—and the inference that such damage need not be addressed in a reliability model— is therefore valid only if each component has not undergone mechanical work during the process of assembly. During the assembly, and even after the hole has been plated, there are several processes that may potentially weaken the plating and impair functionality. Similarly, the assumption that all the components on a board experience the same conditions while in regular use is valid if global conditions, rather than localized ones, affect the board. Most applications will not have global loading; rather, they will be subjected to source loading such as clamps, resistive heating, and base excitation. In these cases, the reliability model needs to account for the entire chain of possible failure.

The components on a PCB experience disparate impacts during the course of multiple assembly processes. Indications that a particular component experiences mechanical work during one or more of these processes are suggestive of the need to include a damage assessment of that component in the overall reliability model. One way to determine whether work is done on a PTH before the board even enters its regular lifecycle use is to plot a hysteresis curve for the reflow cycles. The hysteresis curve will be different for varying reflow profiles; typically the extent of variation may be correlated to the type of solder. It has been established that PTHs can fail due to thermal cycling in regular use and that there can be different failure modes as shown below. The copper material is shown in grey and the PCB material is in black.

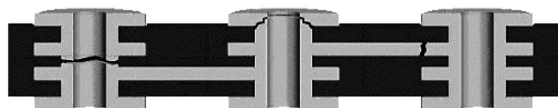

Figure 1: PTH failures. Barrel fracture, shoulder fracture and inner layer separation (from left to right)
Source: Olson, Jack; www.frontdoor.biz/HowToPCB

The failures occur due to the expansion of the PCB with a corresponding increase in temperature. In recent years, the legislation that has mandated the microelectronics industry to use lead-free solder [4] has resulted in manufacturers changing the reflow cycle temperature from approximately 180°C to 230°C-260°C. This increase means that the expansion is larger than was typical previously and also that in some boards the glass transition temperature is low enough to precipitate a change in the modulus of elasticity and the CTE. The corresponding failures are increasingly detrimental as the PCB thickness increases. Other contributing factors include the thickness of the plating, the barrel length, the surface treatment of the board, and the diameter of the barrel. On a board of a given thickness, there may be different barrel lengths as shown below. The difference in barrel lengths and specific geometry may make a specific PTH more susceptible to a given type of failure.

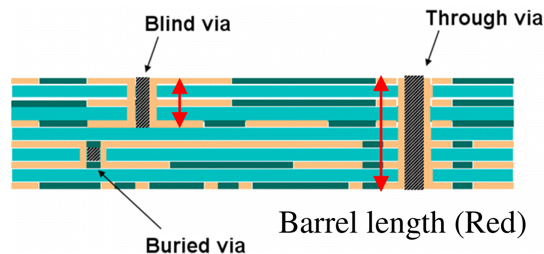

Figure 2: Different barrel lengths of vias on the same board
Source: The University of Bolton; www.ami.ac.uk/courses/ami4931_pcd/u01/

The red arrows show the different via lengths. The green color shows the multiple layers of the PCB with orange representing copper layers and vias. A representative geometry for a PTH or "through via" is shown in the following figure. This cross section image was taken of a multi layered board with the copper layers visible in bright orange. The through via is empty in the middle and the PCB material is shown in grey on either side. This PTH goes through the entire board therefore the barrel length would be the board thickness. The flanges are electroplated with the barrel but the layer interconnects are built into the PCB. After manufacturing the whole board with all the layers, the hole is drilled and the copper is plated to create the connection with the layers. There is a difference in the mechanical connection strength between the flange and the barrel (purple) and the layer interconnect and the barrel (red).

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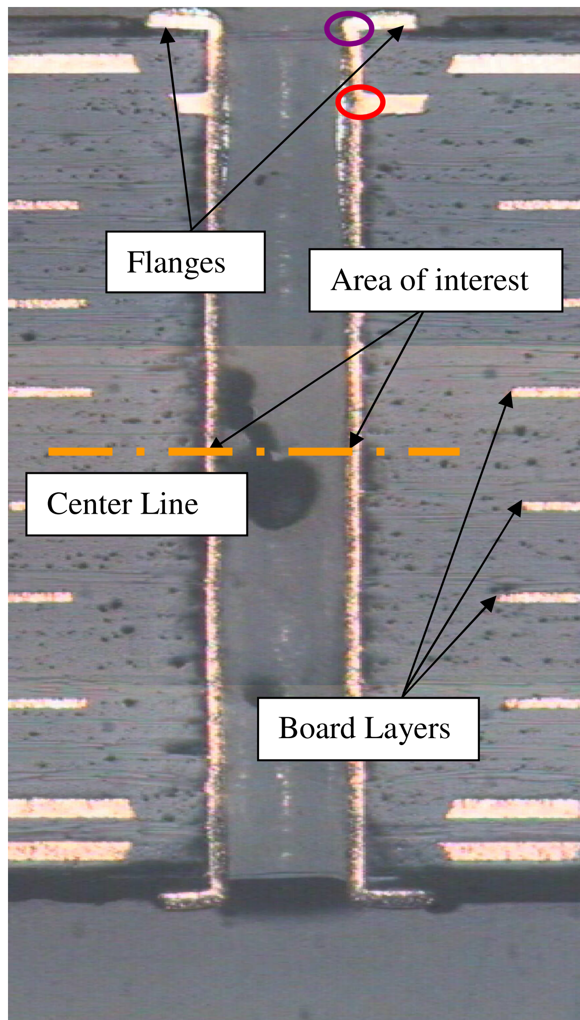

Figure 3: Cross section of a Long barreled PTH showing several layers of the board

A convenient method for exploring the work done on PTHs in reflow cycles is to concentrate on a specific type of failure and to plot the hysteresis curve at the area of interest. Barrel fracture failures were studied in this preliminary investigation. Barrel fractures occur in the copper material along the hoop and cause disconnect from one side of the board to another. The barrel is pulled by the flanges as the PCB is expanding. The mathematical model developed treats this configuration as symmetric and two-dimensional. The maximum effect of the mechanical work is assumed to occur in the center of the barrel exactly at the midpoint of the PCB thickness due to the symmetrical nature of the geometry used in the calculations. These assumptions are made in order to concentrate on the expansion of the board and the stress in the copper alone. This model is then used to illustrate the need for existing and future reliability models to include the reliability of the PTHs in the system over the course of the product lifecycle.

The reliability model of a system is the calculation of the probability of success of the system to perform a certain task. The metrics for success may be defined in numerous ways that may be general or application specific. Probabilistic calculations may be highly complex, depending on the amount of redundancy, the number of components, logical structure, the system architecture, and additional factors. In a simple system with no redundancy as shown below, the calculation is straightforward.

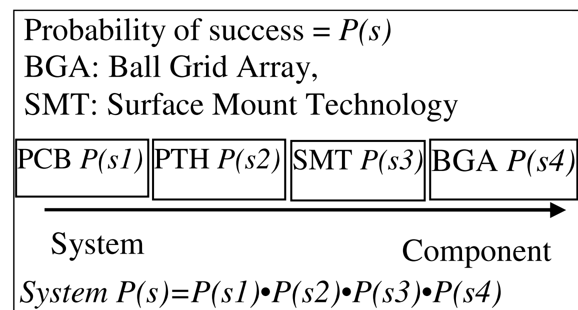

Figure 4: An example of an elementary reliability calculation for a system on a PCB

The calculations to find the individual probabilities quickly become non-trivial depending on the number of components in each system level and the extent of internal redundancy. It is frequently feasible to design a system where a parallel structure can make several branches in the reliability model. It can be seen here that even in a simple system, the assessment of the reliability of a component may be attempted. The probability metric in this instance is defined as the likelihood of the PTH performing its intended function over the system lifecycle under all loading to which it is exposed. The probability of success of a PTH should assume that some damage exists at the beginning of regular use. The amount of damage should be calculated for each individual PTH that is present on the board because each will likely accrue a different amount of damage depending on its unique exposure conditions and configuration.

Although all PTHs in a reflow cycle go through the same temperature change, in regular use each one has a different load profile. The individual load profile is affected by several different factors. The higher levels of board integration, higher power usage, and the smaller board sizes reflective of increased miniaturization correspond to each part of the board having a different thermal load. In the past, each part of an electronic system was on a separate board. In recent years, boards have become more integrated and increasingly complex, with PCBs

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possessing more layers, vias, and higher component density. The PTHs that are positioned more closely to high power components will experience larger temperature differences in regular operation and these PTH will be more likely to fail during operation.

Interpretation:

It is not possible to make an over arching statement about the effect of the reflow cycle on PTHs: there are too many different types of PTH, solders, processes, and laminates to produce an accurate model for a comprehensive reliability assessment. However, there are a few factors that can be considered as contributors to the amount of damage before regular operation that can and should be considered for a PTH in a given system whose attributes are defined.

The coefficient of thermal expansion (CTE) of the electroplated copper of the PTH is lower than the laminate's. Finding a laminate that has a lower CTE in the direction of the PTH barrel will result in lower stresses during the reflow cycle[7]. Some laminates exhibit a raised CTE as the temperature increases and causes elevated stress levels.

The temperature cycles during reflow are becoming increasingly detrimental to PTHs with the adoption of lead-free solders. The solders to which manufacturers are currently turning are processed at higher temperatures. A common reflow cycle is shown in Figure 5, reaching a peak temperature of 230ºC. In this profile, there is a cool-down from the maximum temperature of 6ºC/sec to room temperature.

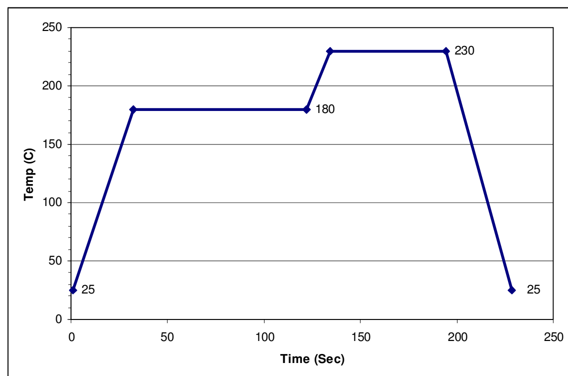

Figure 5: Solder reflow temperature profile

These high temperatures not only increase the amount of expansion in the board, as expected, but also change the board properties themselves. In some laminate materials, the CTE changes as the temperature increases. In Figure 6, the CTE of the PCB material used for the purpose of this analysis is shown.

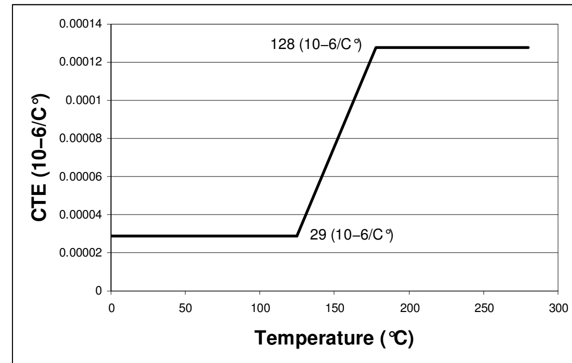

Figure 6: Coefficient of thermal expansion of the PCB[3]

At around 150ºC the CTE increases from 29 to 128 (10^{-6}/ ºC), the values used in this analysis. These values come from a direct test performed on a particular batch of boards. Subsequent analyses using different boards necessitate that these values be obtained for each type of board. These measurements will be important to determine because the CTE mismatch is the key mechanical load as a result of the temperature change.

Board expansion contributes to a 'stretching' of the copper material. The following figure shows the Stress-Strain curve used in the analysis, showing elastic and plastic behavior. The plastic region in the material is necessary for hysteresis to be modeled.

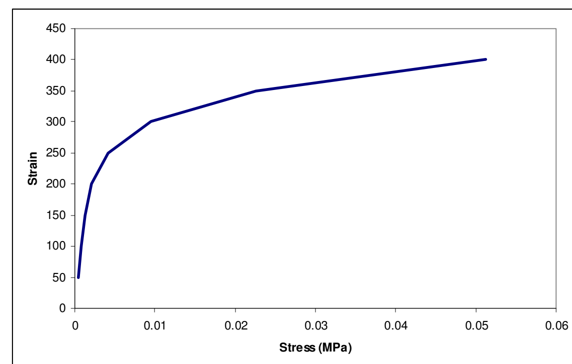

Figure 7: Copper material properties (Stress-Strain curve)

Once the reflow temperature profile, the CTE properties of the laminate and the plasticity in the copper have been accounted for, along with any additional parameters, a generalized hysteresis curve can be estimated using a finite element model. Three cycles of reflow are solved and plotted in a smoothed curve, as shown in Figure 8. Three cycles are plotted, and as expected, the first cycle has the

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greatest effect on the extent of mechanical work because it imparts the initial load. Each following load cycle follows roughly the same curve. It may be inferred that an increased number of cycles would correspond to more work being done on the copper material and to more damage being accumulated.

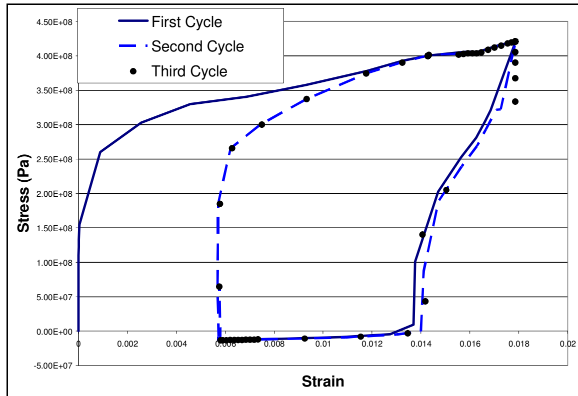

Figure 8: Effective hysteresis loops for the first three reflow cycles.

This model is representative of what any embedded copper via may experience, whether it is electroplated or deposited. Because it has been shown that copper vias will have intermittent failures in some instances, it may be reasoned that the vias will reconnect when the temperature is decreased. This analysis shows that it is inadvisable to assume without verification that a PTH or via has zero damage when it begins regular operation, especially at elevated temperatures.

As noted, the consequences of lowered reliability due to PTH or via failure are significant. An entire board may need to be replaced due to the vias failing. It can become extremely expensive to replace a board due to via failure, especially in critical reliability systems. There are substantial ramifications for cost effectiveness and even product liability, including the development of warranties that are predicated on accurate product reliability assessments.

Model and Geometry Notes

The model used in this analysis is two dimensional, axisymmetric multiple layer PCB with PTH geometry that runs from one side of the board to the other. The geometry was measured using the cross section shown in Figure 9 without the layer interconnects. The purple material is the PCB and the copper is shown in black. The area of interest is identified in the middle of the PTH with a red mark.

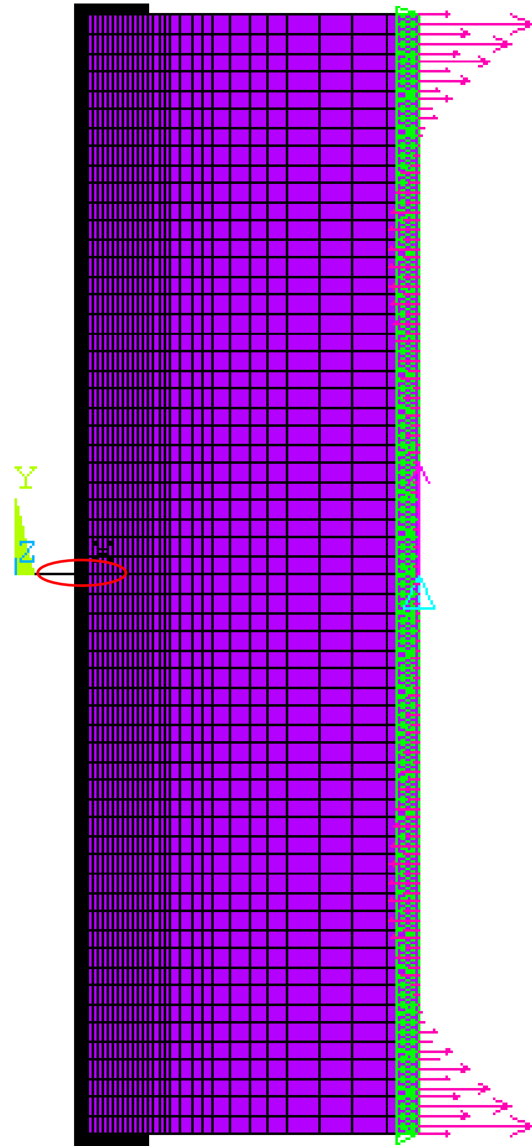

Figure 9: 2D Finite element model showing the area of interest

This is the final model used for calculations, but there were several other finite element cases used to validate its assumptions. A 3D model (not shown) was used to find out if there were ant effects in multiple dimensions that can not be calculated using a simpler model. A mesh convergence study was performed and it was found that five elements across the thickness of the copper were enough. An eight node element is used which translates to eleven node calculations across the thickness.

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Figure 10: Different geometries of PTH Flanges[3]

If a shoulder failure is looked at, the geometry of the flange must be adapted to the actual cross section as shown above. Each one of the flanges may have a different geometry even on the same PTH. From the test cases explored, the different flange geometry did not affect the behavior of the copper in the area of interest because the geometric singularities have a local effect only in this model. It is therefore safe to use the hard edged geometry in this model as long as only the barrel failure is studied.

The finite element model was solved using a non-linear analysis with fifty substeps between each temperature change. The final cool-down to room temperature from reflow temperature used two hundred substeps. When more reflow cycles were modeled, the hysteresis loops continued to overlap. It is possible to insert another level of complexity by modeling time dependent material properties in order to find out if the work in the copper continues the trend. Only three cycles were modeled because that is the common number of cycles a board may experience.

Conclusion:

The determining factor in a reliability analysis may a small component that is hard to find and a failure that is difficult to see. Plated through holes are integral to printed circuit boards and are difficult to track once they are manufactured. Despite these challenges, the effect of the reflow cycles on the PTH can be calculated. The total damage to the PTH before it begins regular operation depends on the specific history of the board. As expected, the first reflow cycle causes the most amount of damage and the greatest initial plastic deformation. Every subsequent reflow cycle will cause more damage to the copper. The effect on an eventual barrel fracture can be calculated. This calculation can be used to modify the reliability model. In multi-layered boards, an inner layer separation failure also needs to be addressed.

Each plated through hole has distinct reliability characteristics, even on the same board. The various geometries, board materials, and load cycles necessitate a separate reliability calculation for each PTH on the board. It is possible to employ several different models to account for the damage in the PTH. Although overdesign of PTHs to prevent the damage may seem desirable, in most cases it will be infeasible to change the manufacturing process or the process by which the PTH is connected to the inner layers. Ignoring the problem is unwise because the miscalculation of the reliability of a system carries serious implications. Each system manufacturer will need to assess the importance of including the PTH in its reliability assumptions.

Additionally, it is possible to create a library of test cases for PTH failures. Such a library can give a quantitative solution for many applications. It is also beneficial for a system design team to have the geometry of every via and expected loading condition for its anticipated application.

As board design becomes more tightly integrated, the complexity of identifying and modeling on-board component failures increases. It is important to monitor and record seemingly isolated instances of failures because they may indicate the need to modify the materials and components on a particular PCB.

Because the board assembly process imposes mechanical work on vias and PTHs, the assumption that they exist in an undamaged state at the start of regular use needs to be modified. The amount of damage already undergone by the board should be calculated depending on its unique history to improve the accuracy of reliability assessments.

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Biography:

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