Ferro-Electrically Enhanced Proximity Communication.

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Abstract

Capacitively-coupled communication between chips, commonly known as PxC, represents a new class of I-O signaling that offers substantially improved off-chip bandwidth density. However, this form of communication presents a challenge from a packaging perspective, since tight chip alignment tolerances are required to maintain high signal fidelity and avoid cross coupling between neighboring channels. To mitigate the packaging constraints, capacitive coupling between the communication pads can be enhanced with materials that have high dielectric coefficients. Here, ferroelectrics hold promise over contemporary low- and high-k dielectrics, however their processing conditions need to be better understood and the compatibility with CMOS circuitry has to be established during integration with a back end of the line process module. In this paper we present experimental results on microfabrication modules for various families of ferroelectrics when monolithically deposited on Silicon. Additionally, we report their associated dielectric properties as extracted by measured capacitance enhancements in our fabricated devices. In this work Strontium Titanate and Barium Strontium Titanate films are sputter deposited on platinum atop Silicon. Capacitive measurements were accomplished by microfabricating electrodes atop these structures in geometries that are size and shape dependant. Dielectric coefficients as high as 400 times that of air are measured.

1. Introduction.

"Proximity communication" represents the general application for face-to-face integrated circuits communicating by capacitive coupling between chips. Very high communication signal density can be achieved when compared to wire-bonding or solder-ball connections that are used today for contemporary conductive signaling between chips [1]. In addition, in the capacitive case, off-chip circuits need drive only a small, high-impedance, capacitive pad much akin to the gate of a transistor. The electrical pad pitch may be on the order of 20 μm. Each pad can drive signals at line rates of 2.5–5 Gbps or higher. This provides a potential communication density in excess of 1.25 petabits per second per square centimeter (Pbps/cm^2). Experimental capacitive proximity communication circuits have yielded aerial densities up to 43 Tbps/cm^2 to date. In the case of capacitive proximity communication, the engineering limits to signal density will result from the area and power of the transmitter and receiver circuits. Ultimately, proximity communication provides an off-chip signaling bandwidth that can scale with the feature size and frequency of on-chip wires. More critically, there are alignment constraints required for this form of communication to be effective. The chips are

required to face each other with their active sides abutting, and to maintain strict alignment between the chips. Exploiting this enormous bandwidth effectively requires a reliable, manufacturable and economical means for positioning the chips precisely relative to all six degrees of freedom (x and y in-plane, perpendicular z separation, tip, tilt, and rotation). In theory, satisfactory communication requires that any misalignment to be under half of the pad pitch; this is often less than the error experienced during dicing of the chips or positioning with pick and place tooling. In practice, the alignment requirements are generally much more stringent. Reducing misalignment improves communication performance between the chips and lowers power consumption. Unfortunately, it is not a simple matter to align the chips properly using existing manufacturing platforms, such as those used for conventional single-chip modules or conventional multi-chip modules.

One way to overcome the alignment constraint problem for PxC is to improve the capacitive signal strength by use of higher dielectric strength materials between chips. The capacitive signal strength is directly proportional to the pad area and dielectric constant while inversely proportional to the chip gap. This follows from a simple parallel plate approximation for the capacitive signal. A number of materials possess extremely high dielectric coefficients such as the ferroelectric family based on titanates. These materials can have huge dielectric coefficients approaching 25000 times that of air. However, this may be an overly simplistic view of the problem as we describe below.

2. Proximity signaling.

High fidelity PxC signaling requires high capacitative coupling between the pads when the chips face each other. To illustrate the capacitive signal strength in real PxC applications we show measured strengths versus gap for a variety of pad geometries. Plotting capacitance versus the airgap using experimental measurements are shown in Figure 1. In this experiment [9], there were array of pads of dimension 8μm x 8μm with a pitch (center to center distance between pads) of 9 μm. Each pad has a passivation SiN_x layer of 1 μm (ε_r=7) and 1 μm SiO_2 layer (ε_r=4.1). Capacitance from other pad sizes are also shown, Additionally, Figure 1 presents results obtained on silicon in a CMOS based process using a 180 nm node. The top level metal is aluminum and its pad is covered with described passivation layers. As can be seen in Figure 1 coupling capacitance is of order 10 ff.

The data in Figure 1 has been modeled with an analytic expression for the signal capacitance derived from classical electromagnetic theory. Even though the modeling is comprehensive in extent and additionally provides a good fit to the measurement it has the added benefit that it is a closed form analytic solution. Furthermore, it is known that the one dimensional parallel plate model provides values in reasonable agreement with this analytic expression. However, the measured values in Figure 1 are very different form a parallel plate expression using the pad geometry given in Figure 1 along with the associated stack up parameters. This is because of stray capacitance between the top metal pad and the rest of the CMOS stack up as well to the substrate. The latter effect makes the signal capacitance strength between the pads essentially 10x smaller.

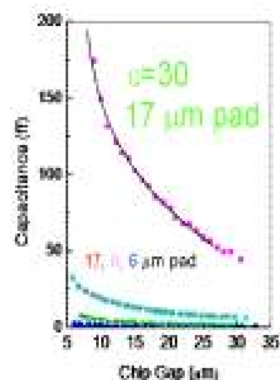

Figure 1. The three lower curves are measured capacitances vs. chip gap for different pad sizes. The upper curve is calculated capacitance vs. chip gap when the space is filled with a dielectric coefficient of 30.

Significantly stronger signal strength capacitance is observed when filling the gap with a dielectric material over an air gap as depicted in Figure 1. Here a material with ε_r=30 is calculated using our analytic expressions reported in reference [4].

A graphical representation of the problem is shown in Figure 2 as indicated by a parallel plate model that corresponds to a three configurations of face to face PxC capacitive signal strength. The three cases consist of signal capacitance between chips either with an air gap having no ferroelectric, with 10 μm ferroelectric (ε_r=1000) over the pads or with the gap between chips is filled fully with ferroelectric (ε_r=1000). The dotted horizontal line shows the noise floor limit as to when the signal strength degrades to the extent communication between chips has become compromised. The dotted vertical line represents a

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physical limit where pick and place tooling falls within tolerance for chip assembly. We seek solutions to the problem that lie to the upper right of the intersection of the dotted lines in Figure 2.

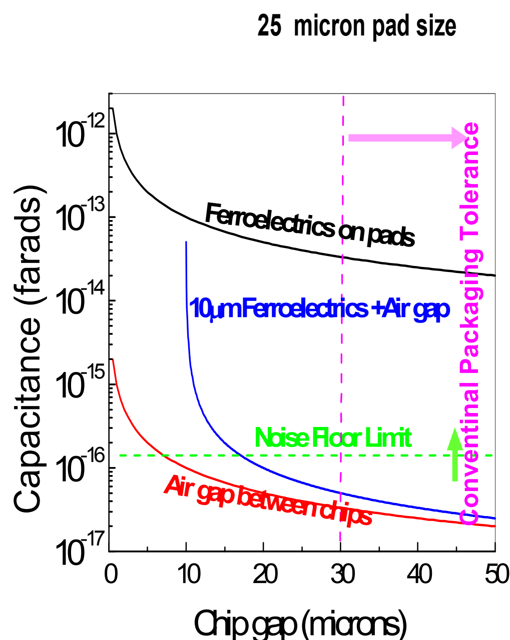

Figure 2. Graphical representation of the ferroelectric advantage for PxC.

2. Material background and experimental considerations.

In this effort we study the $Ba_xSr_{1-x}TiO3$ (BSTO) solid solutions that belong to the family of ferroelectric perovskites. In the paraelectric phase, they have a cubic unit cell (space group Pm3m). In the ferroelectric phase below the Curie temperature (T_C = 30ºC for $Ba_{0.8}Sr_{0.2}TiO_3$), they condense into a tetragonal unit cell (space group P4mm). One important property of these materials is that the unit lattice has a strong internal dipole moment that spontaneously self aligns into large domains at temperatures below the Curie points provided their internal corressive fields are minimal. This material can provide very high dielectric coefficients for capacitive enhancements and are well known in the thin film capacitor industry. Less is known about monolithically integrating them for CMOS applications.

Our investigation of materials suitable for the enhancement of the proximity chip-to-chip communication, PxC, thus begins with strontium titanate ($SrTiO_3$ or STO) and barium strontium titanate ($SrBaTiO_3$ or BSTO) ferroelectrics. Both could be shaped into the sputtering targets and subsequently sputtered with argon in the presence of DC or RF applied fields. It is expected from reports already published that BSTO possesses higher resulting dielectric properties although its thin film fabrication and following integration with CMOS circuitry may be more complicated relative to $SrTiO_3$ given its more complex elemental composition. The proper choice of this composition, or relative proportion of Sr to Ba, may need to be well controlled during the film fabrication to result in repeatable material properties. Our main emphasis initially was, therefore, on experimentation with the simpler perskovite family of strontium titanate in order to first identify the tooling for ferroelectric material sputtering, baseline for the test structure deposition and fabrication parameters as well as establish the data taking experimental setup and to validate measured data. The ultimate goal is to develop a post-process for integration of the high dielectric constant ferroelectric films with CMOS PxC circuitry. Such integration requires using the CMOS compatible set of tools, process conditions and chemistry. Accordingly the ferroelectric film thermal budget has to be kept at 500ºC or below and scale down correspondingly with CMOS node size [5].

3. Ferroelectrics microfabrication.

For deposition substrates we deploy four inch silicon wafers that have been pre-coated with titanium layer 100 nm thick followed by a 150 nm thick platinum layer. Platinum later functions as a seed layer for the growth of the ferroelectric materials. Titanium is used as a diffusion barrier to prevent formation of the platinum silicide. Platinum silicide would form at a moderate 250ºC temperature which is lower than the deposition temperature or RTA post-processing temperature for STO or BSTO. Upon silicidation the resulting interface would become rough and non-suitable for high quality ferroelectric deposition therefore it is best to prevent platinum/silicon interfacial mixing by inserting the titanium barrier of sufficient thickness. Titanium is not known to react with silicon till above 600ºC which is within our CMOS compatible thermal budget.

Ferroelectric films could be deposited by spin coating, in the CVD environment or with sputtering. Spin coating results in the very thin material layer, too thin to work with PxC packaging requirements. CVD deposition entails access to a dedicated expensive system. Sputtering

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is a proven versatile technique, STO and BSTO could be acquired in the variety of sizes and shapes. For high quality ferroelectric film the deposition technique parameters are expected to be appropriately tailored to maintain material stoichiometry.

The STO three inch target has been acquired and installed into an AJA International ATC Series Thin Film Sputtering Deposition System. The system is built around an AJA Stiletto Series magnetron sputtering source which features in-situ source head tilting allowing precise and repeatable con-focal, direct, and off-axis deposition. The system has a load lock and an ultra high vacuum turbo pumped deposition chamber. The substrate may be heated up to 800ºC and RF bias may be applied to the sample before and during deposition.

The resulting sputtered material properties are sensitive to the deposition conditions such as the substrate temperature, sputtering argon gas chamber pressure, RF sputtering power, lack or presence of oxygen in the chamber. Generally the higher substrate temperature results in better quality material so this parameter would need be optimized while keeping it within the limits acceptable to CMOS circuitry. A post-deposition thermal anneal could also be used after the sputtering. A small amount of oxygen partial pressure could be added if the deposited material may elementally decompose. Argon pressure and the RF power would set the deposition rate.

The process flow is shown schematically in the Figure 3. A described seed layer is formed on the epi ready four inch silicon substrate. Ferro-electric film of strontium titanate was then sputtered onto it at different conditions. The obtained wafers were either annealed or not annealed at different temperatures and rates. Upper electrodes (Ti (15nm)/Au (150nm)) were formed on the wafer with a NR-9 resist lift-off process.

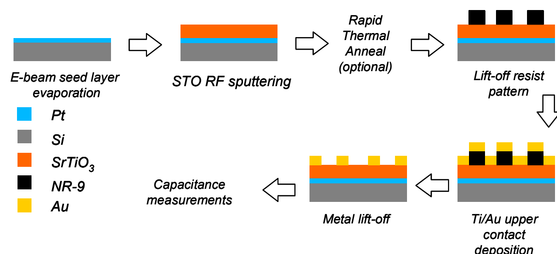

Figure 3. Schematic process flow for the STO characterization.

Near DC capacitance of the obtained structures was measured and a corresponding dielectric constant of the film was deduced as a function of the processing conditions. Additionally the ferroelectric film thickness and the optical refractive index have also been measured. The refractive index is another important parameter in the material metrology that would indicate how close the deposited thin film material properties are to its bulk tabulated values.

The described fabrication sequence yields a set of measurable capacitive structures that all share the same continuous ferroelectric film and the same bottom electrode or ground plane. The eventual PxC capacitive structures have to be fully isolated in these levels in order to minimize the cross-talk between neighboring structures and their corresponding communication channels. A particular patterning technique would need to be developed for a ferroelectric film and applied before or after the sputtering. The earlier mentioned lift-off approach with resist can not be implemented due to high temperature that the substrate is elevated to during the film deposition. The lift-off photoresist would harden and deteriorate at these conditions. The dry or wet etch subtractive patterning chemistry is not immediately available in the CMOS fabrication environment, the approach of choice is the argon milling [6] which is a slow process with poor selectivity and high developmental cost. Alternatively, we have prepared a shadow mask in order to fabricate discrete isolated ferroelectric regions on the test substrate. The shadow mask is fabricated from a 250 µm thin four inch silicon substrate with deep dry etched through openings of varying shape and dimensions. The shadow mask complements the upper metal contact mask, its layout is shown in Figure 4.

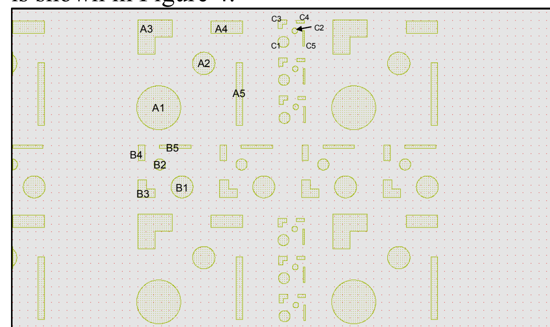

Figure 4. A layout for the capacitive test structures. Deep dry etched silicon shadow mask and the corresponding upper metal electrode mask have been fabricated according to this layout. The capacitance is measured by directly simultaneously applying probes to the upper metal surface and the common ground plane.

Therefore the ferroelectric film can be sputtered through the shadow mask down onto the substrate

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resulting in patterned structures for isolation. A similar technique could be developed for the ferroelectric patterned PxC pad deposition.

The fabricated test capacitive structures have been made in sets with either constant area but scaled perimeter or constant perimeter but scaled area in order to track the origin of the possible leakage current. The leakage current could be dominated by either mesa sidewall or its bulk and would indicate inadequate ferroelectric material quality. The test features' dimensions have also been scaled from approximately 2.2 mm down to 0.1 mm which to demonstrate the linear relationship of capacitance with area. With these dimensions the fabricated structures are expected to have large appreciable capacitance in the nF range that our standard measurement equipment would be sensitive to with sufficient resolution.

4. Process flow and deposition.

Table 1 summarized a set of experiments performed with sputtered strontium titanate. The deposition rate was found to be maximized at r=2.9nm/min. As expected it is sensitive to the sputtering conditions and the substrate temperature. From the CMOS compatibility standpoint the substrate temperature in this back end processing is to be maintained sufficiently low to ensure reliability of the interlayer dielectrics (ILD) and metal interconnects. The long process duration needed in this case in order to deposit an appreciable material thickness is an extra challenge to be addressed. The thermal budgets are in fact becoming even stricter as industry continues shrinking the transistor gate size. The novel low-k ILDs are especially prone to failure given their reduced interlayer adhesion strength and brittleness. We have dialed the substrate temperature down to 200ºC for prolonged material sputter deposition. The deposition rate could conceivably be increased several times with a larger applied RF power to the target. Our system power supply was limited to the tabulated 400W. The deposited material quality could be improved with a post deposition rapid annealing cycle without compromising the CMOS integrity as long as the exposure to high temperature is substantially short or delivered in the form of a pulse.

Table 1. $SrTiO_3$ film process conditions.

Sample	RF Sputtering							Annealing		Metrology Tools
	Pressure [mT]	Time [min]	Temp [C]	Gas Flow [sccm]	Power [W]	Thick. [nm]	Deposition rate [nm/min]	Temp [C]	Time [sec]	
1	5	50	20		200	30	0.6	N/A		Dektak, SEM
2	5	50	20		300	70	1.4	N/A		Dektak, SEM
3	25	154	200	10 Ar	400	180	1.2	300, 400, 500, 600	300	Dektak, SEM, EDAX
4	8	570	200		400	1500	2.6	N/A		Dektak, Capacitance
5	8	232	500		400	620	2.7	N/A		Dektak
6	6	180	350	6 Ar 0.2 O2	400	530	2.9	500, 600	300	Dektak, Filmetrics, SEM
7	6	270	500	10 Ar 0.4 O2	400	270	1.0	N/A		Dektak, Filmetrics Capacitance
8	6	270	500	10 Ar	400	660	2.4	N/A		Dektak Filmetrics
9	6	270	200	10 Ar	400	730	2.7	400, 500	50	Dektak, Filmetrics Capacitance

The sputtering of the multi element compounds requires a proper balance of conditions in order to keep the material composition intact upon the deposition. The resulting material could be richer in one element and depleted of the other therefore its properties would differ from the bulk targeted values. Energy-dispersive X-ray spectroscopy (EDAX) is a good initial material characterization technique to

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validate the material composition is in order. Figure 5 displays such an EDAX spectrum for our sputter deposited STO film at 200ºC. The deduced proportion of oxygen, strontium and titanium is well corresponding to the STO bulk values demonstrating no elemental loss in the deposited film. Optical refractive indices as measured by Filmetrics were consistently about n=2.42-2.45 at the wavelength of λ=632nm for all of the samples in the Table 1. These values correlate very well with the reported bulk values for STO [7]. This data though does not describe the crystalline quality of the deposited material which could be separately established by X-ray diffraction and measurements on the dielectric permittivity. Nonetheless the compositional integrity is manifested through these tests.

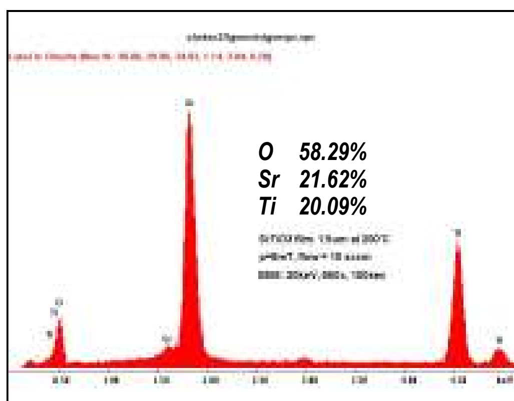

Figure 5. EDAX obtained elemental spectrum of the sputter deposited STO film.

As stated it is advantageous for the CMOS integrity to deposit ferroelectric films at moderate temperatures. We have shown that STO films deposited at 200ºC are compositionally identical to the bulk STO crystals. In order to improve the crystalline quality of the films and enhance therefore the dielectric permittivity the temperature could be elevated during the RTA cycles. We have experimented with post deposition RTA conditions. Figure 6 contains a set of images showing a surface of the 180nm thin STO film sputter deposited at 200ºC and later annealed at 500 and 600ºC for 300 seconds in flowing oxygen or forming gas (95% N_2, 5% H_2) atmosphere. The corresponding defect density varies depending on the RTA conditions and is minimal at the highest temperature of 600ºC with the presence of oxygen which indicates an improving longer order crystallization of the sputtered film.

5. Dielectric enhancement from capacitance measurements

A DC capacitance measurements were performed using digital multimeter with a resolution of 1pF. A well known formulae linking the structure capacitance to its geometry and material parameters has been followed

$$C = (\varepsilon_r \varepsilon_0)\left(\frac{A}{d}\right) \qquad (1)$$

Where A and d are the contact area and the thickness of the ferroelectric film forming the capacitor, ε_r is the relative material dielectric constant, which is the parameter of interest to be calculated from the measured data.

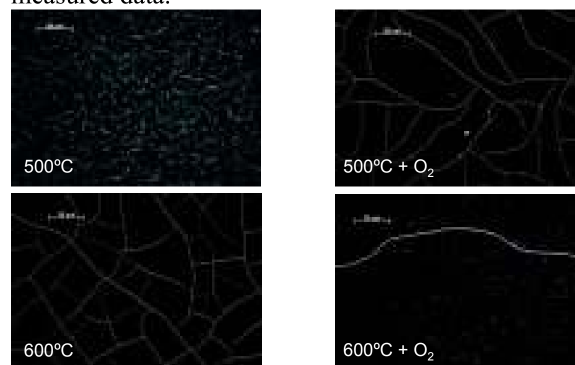

Figure 6. Micrographs of the STO surface originally sputter deposited at 200ºC and further annealed at the described temperature with and without flowing oxygen.

Additionally even with an increased titanium diffusion barrier (to 100nm) and avoided silicide formation the ferroelectric films would fissure at high process temperature (Fig. 6) due to the large thermal expansion coefficient mismatch between the STO and its silicon substrate (α_{STO}=9.4e-6 K^{-1}, α_{Si}=2.6e-6 K^{-1}). The density of these fissures is too high for the upper metal contacts to be patterned without yield reduction. Ultimately the capacitive measurements have been carried out on the samples that have been coated with thick 100nm titanium barrier between silicon and platinum interfaces and samples with no or little fissuring upon deposition and annealing.

Table 2 contains the measurement parameters, data and results for the fully processed samples. The structures in the table correspond to those identified correspondingly in Figure 4 which depicts their layout schematics. It is observed therefore that in the presence of oxygen not only the STO films are more stable at high temperature (Fig. 6) but they also exhibit higher dielectric constant. As deposited at 200ºC STO measures a relatively modest constant of ε_r=26.2, after a moderate anneal at 400ºC for 50 seconds this value does not appreciably change, leading to a conclusion that the deposition itself is mainly a process setting up the further material properties and anneal would have to be carried out at higher temperature in order to improve

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STO quality and increase its dielectric constant. If sputtered with added oxygen into the argon mix, the STO's properties are much improved. The dielectric constant is measured at ε_r=174.5 for these sputter run. As mentioned films grown without oxygen at the same temperature could not be tested due to their excessive fissuring. The resistance of each of these measured structures was measured well in the megaohms range ensuring their truly capacitive nature without material defectivity that could cause unwanted leakage of either sidewall or bulk origin.

Table 2. Experimental data. Measured capacitive values and corresponding dielectric constants.

Structure	Area um2	Capacitance nF	Thickness um	Dielectric constant	Capacitance nF	Thickness um	Dielectric constant	Capacitance nF	Thickness um	Dielectric constant
		Deposition at 200C. No RTA. No O2.			Deposition at 200C. RTA at 400C. No O2			Deposition at 500C with O2. No RTA.		
A1	6160000	2.25	0.73	29.1	1.80	0.73	23.1	33.60	0.27	165.2
A2	1610000	0.53	0.73	26.1	0.57	0.73	25.5	9.42	0.27	177.1
A3	3630000	1.18	0.73	25.9	1.35	0.73	29.0	20.00	0.27	167.5
A4	1600000	0.64	0.73	29.3	0.54	0.73	24.0	9.41	0.27	178.0
A5	1600000	0.58	0.73	26.0	0.64	0.73	29.2	9.53	0.27	180.2
B1	1540000	0.61	0.73	28.9	0.55	0.73	25.5	8.98	0.27	176.3
B2	402500	0.19	0.73	24.6	0.18	0.73	22.3	2.38	0.27	174.4
B3	907500	0.35	0.73	24.9	0.32	0.73	22.4	5.34	0.27	177.0
B4	400000	0.19	0.73	24.4	0.18	0.73	21.1	2.39	0.27	176.6
B5	400000	0.20	0.73	25.0	0.19	0.73	22.9	2.39	0.27	176.5
C1	385000		0.73		0.17	0.73	20.8	2.30	0.27	176.2
C2	100625	0.11	0.73	26.0	0.10	0.73	20.7	0.63	0.27	169.9
C3	226875	0.14	0.73	23.5	0.13	0.73	20.0	1.37	0.27	173.9
C4	100000	0.11	0.73	25.6	0.10	0.73	21.2	0.64	0.27	171.2
C5	100000	0.11	0.73	27.0	0.10	0.73	21.9	0.64	0.27	173.7
		Average		***26.2±1.8***	Average		***23.3±2.8***	Average		***174.5±4.1***

6. Barium Strontium Titanate experiments.

Another promising ferroelectric material is barium strontium titanate ($SrBaTiO_3$). As reported BSTO exhibits stronger dielectric and magnetic properties relative to STO so its deposition setup in our RF magnetron sputterer had to be specifically adjusted.

The resulting sputtered material properties are sensitive to the deposition conditions such that the substrate temperature, sputtering argon gas chamber pressure, RF sputtering power, lack or presence of oxygen in the chamber. In the BSTO experiments reported here the deposition parameters have been optimized while working with STO material to maximize the deposition rate (Table 3):

Table 3. BSTO sputter deposition parameters.

Pressure, mT	Argon flow, sccm	Power, W	Deposition rate, nm/min
6	10	400	3.3

Near DC capacitance of the obtained structures was measured and a corresponding dielectric constant of the film was deduced as a function of the processing conditions. Optical refractive indices as measured by Filmetrics were consistently about n=2.3-2.33 at the wavelength of λ=632nm. These values correlate very well with the reported bulk values for BSTO.

Table 4 contains the measurement parameters, data and results for the fully processed samples. No tests have been performed with oxygen ambient, neither during the sputter deposition, nor during the RTA. Different ramp up rates have been applied to the sputtered films during the RTA steps in order to find conditions possibly minimizing the film cracking. RTA performed at 400ºC does not introduce cracks into the BSTO films while at 500ºC films would crack similarly with 1/100µm resulting density regardless of the RTA ramp up rate (50ºC/sec or 3ºC/sec) stating that the temperature itself and the resulting mismatch in material (substrate to ferroelectric) thermal expansion are a leading cause effecting the films' integrity. The maximum dielectric constant is measured at ε_r=421 for the film grown at 200ºC and further annealed at 400ºC for 50 seconds. It is a substantial improvement with respect to the previously reported values for dielectric constants measured with STO films.

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Table 4. Measured capacititances and corresponding BSTO dielectric constants.

Structure	Area	BSTO, deposited at 200C. RTA 500C/100sec. No oxygen. Fast ramp up R=50'C/sec.			BSTO, deposited at 200C. RTA 400C/50sec. No oxygen. Fast ramp up.			BSTO, deposited at 200C. RTA 500C/50sec. No oxygen. Slow ramp up R=3'C/sec.			BSTO, deposited at 450C. No RTA. No oxygen.		
	um2	Capacitance, nF	Thickness um	Dielectric Constant	Capacitance, nF	Thickness um	Dielectric Constant	Capacitance, nF	Thickness um	Dielectric Constant	Capacitance, nF	Thickness um	Dielectric Constant
A1	6.16E+06	8.79	0.88	140.6	26.70	0.88	430	15.30	0.88	246		0.58	
A2	1.61E+06	2.54	0.88	152.0	7.86	0.88	481	3.64	0.88	220	4.210	0.58	168
A3	3.63E+06	6.70	0.88	181.5	19.93	0.88	544	7.46	0.88	202		0.58	
A4	1.60E+06	2.59	0.88	156.1	7.90	0.88	486	3.60	0.88	219	4.945	0.58	200
A5	1.60E+06	2.30	0.88	138.3	7.38	0.88	454	3.74	0.88	228		0.58	
B1	1.54E+06	2.45	0.88	153.1	8.34	0.88	533	4.46	0.88	283	3.910	0.58	163
B2	4.03E+05	0.48	0.88	99.5	1.92	0.88	456	0.70	0.88	155	1.260	0.58	193
B3	9.08E+05	0.95	0.88	96.5	4.81	0.88	519	2.47	0.88	263	2.695	0.58	189
B4	4.00E+05	0.47	0.88	98.9	2.07	0.88	496	0.67	0.88	148	1.325	0.58	205
B5	4.00E+05	0.45	0.88	92.4	2.01	0.88	481	0.70	0.88	156	1.485	0.58	231
C1	3.85E+05	0.46	0.88	98.6	1.62	0.88	399	0.62	0.88	142	1.171	0.58	187
C2	1.01E+05	0.17	0.88	97.1	0.33	0.88	254	0.22	0.88	143	0.401	0.58	213
C3	2.27E+05	0.30	0.88	97.0	0.67	0.88	262	0.39	0.88	139	0.776	0.58	203
C4	1.00E+05	0.17	0.88	97.7	0.33	0.88	258	0.22	0.88	146	0.425	0.58	230
C5	1.00E+05	0.17	0.88	100.2	0.33	0.88	256	0.22	0.88	149	0.523	0.58	294
Average dielectric constant				**120.0**			**421**			**189**			**206**

A direct comparison of both materials, BSTO and STO, is plotted in Figure 8. The modest temperature for the film deposition (200ºC) as well as the minimal stressing conditions during a subsequent RTA step (400ºC for 50 seconds) provide evidence that these conditions can be compatible with current CMOS technologies. We intend to verify this in future work by applying these conditions to CMOS circuits and testing their response.

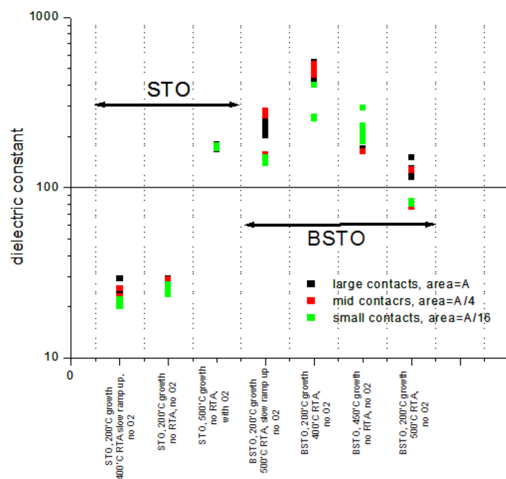

Figure 8. Measured dielectric constants for both STO and BSTO sputter deposited.

7. Conclusions.

We have conducted a series of experiments in order to characterize STO and BSTO ferroelectric materials with applications in proximity communication. The sputtering conditions have been carefully selected to keep the deposition process within the compatibility window with current and future CMOS generations. The highest obtained deposition rate of 3.3 nm/min (BSTO) may be found too low (4.5 hours to obtain 880 nm thick film) which would slow down the manufacturing line if introduced into a foundry. The deposition rate for a sputter process could be increased with a different higher power tool. The sputtering rate would be linearly increased with power upwards of currently applied 400 W). Tools with 1000 W or higher power supplies are a norm in the manufacturing. The rate could also be further increased with an optimized chamber configuration or, rather, reduced distance between the target and the wafer (down to about a cm from currently fixed one inch of this distance). It is not unrealistic to extrapolate the sputter deposition rate could be increased to about ~10nm/min. It may be a fundamental upper limit for sputtering process. If a several micron thick ferroelectric film is needed the overall cycle time would amount to still several hours which may be found inadequate and too long in the manufacturing environment. We are currently also studying other alternative approaches for ferroelectric film deposition in the CMOS compatible manner. Ferroelectric aerosol deposition might be a possible solution capable of high, ~30 µm/min, deposition rates. Deposition of several ferroelectrics has been demonstrated with this technique.

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