Improved Design of a High Density 3D Multichip Module for Class I Medical Devices

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Abstract

Today's powerful DSP based hearing instruments demand both high density and low cost microelectronic packaging solutions. In turn, this demand drives innovation and substantial collaboration among design and manufacturing personnel and suppliers. Conventional design and process envelopes are challenged and new problems arise. Rapid failure analysis and root cause identification are essential in this global, fast-paced development arena. Here we introduce a novel high density multichip module designed for placement onto a flexible, folded hearing aid SMD assembly and discuss the challenges faced by the design team. Delamination, electrochemical migration, and thermal stress failure mechanisms identified during design verification testing are examined, along with the techniques and tools of failure analysis and problem solutions.

Key Words: multichip module, high density flex circuit, electrochemical migration, XPS (X-ray photoelectron spectroscopy), SEM/EDS (scanning electron microscopy/energy dispersive x-ray spectroscopy, finite element analysis.

Introduction

The size of the human ear canal and the available space around the ear constrains the size of today's hearing instruments, yet customers demand greater functionality. In other words, we must devise new ways to pack more electronics into a small volume. This demand in turn drives innovation in the design of the microelectronic packaging utilized in these modern DSP based devices. With the packaging innovation come new design hurdles that must be cleared. This paper describes an innovative, mixed technology packaging solution and how several problems were identified and remedied.

Background

The global nature of today's new product development arena is evident in our situation. Our ICs come from around the globe. We have an established, in-house thick film and surface mount manufacturing operation at our Asian facility. Our Minnesota microelectronic design team works closely with select external flex circuits suppliers to develop a variety of flex substrates. The final hearing device is assembled and distributed at yet another of our North American facilities. Collaboration among design, manufacturing, logistics, and external supplier personnel is essential. This is particularly true during the iterative find-and-fix cycles inherent in the new product development process.

The microelectronic package examined here consists of two primary parts; a thick film multichip BGA module and the next level assembly it goes into: a flexible SMD circuit. The thick film module, and slight variations of it, is used in several different instrument models, while the flexible substrate is designed specifically for some models. Verification activities happen during each design segment. The focus of this paper is the failure mechanisms induced in the microelectronic package by thermal stress and accelerated aging tests and our solutions.

Microelectronic Package Design Description

The final SMD assembly, as shown in Figure 1, consists of a flex circuit substrate populated with a ceramic thick film multichip BGA module and other standard SMT devices.

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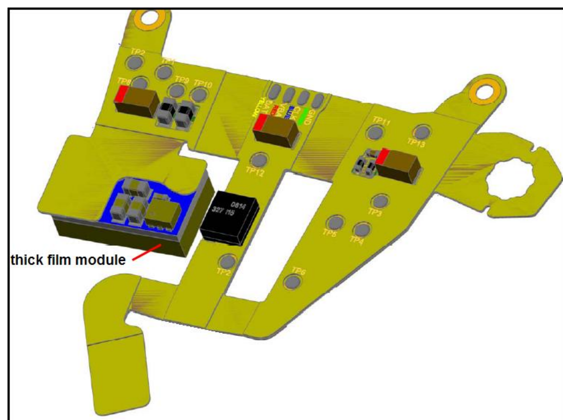

Figure 1: Flex SMD assembly prior to folding.

The flex substrate is a 5” x 5” panel consisting of 20 individual circuits with a 25 µm thick polyimide core and adhesive layers, 3 copper conductor layers, and photoimageable solder mask. Total stack thickness is 203 µm, 127 µm thick in the bend areas.

The thick film modules (Figures 2-3) are assembled on a base alumina 3” x 3” substrate that is 375 µm thick with 80 circuits per substrate. The module, shown in Figures 2 & 3, contains a DSP IC (IC1), two memory IC’s (IC2 & IC3), a 6 pin SMT specialty IC, and 8 passive chip components (5 0201, 3 0402). The module is a variant of the popular chip-on-flip-chip style packages developed for hearing aids and described by Dzarnoski et. al.[1]. This module is more aptly called a module-on-flip-chip. First the DSP IC is flip chip attached to the ceramic substrate, along with 4 0201 chip components. Next a spacer is placed atop the DSP followed by placement of a memory module atop the spacer. The memory module is two EEPROM IC’s flip chip attached to a 250 µm thick alumina substrate -a rigid PCB substrate is an option. The memory subassembly is wire bonded to the DSP substrate while all flip chip and passive component connections are made using convection reflowed solder. Flip chip ICs are secured with underfill epoxy that is automatically dispensed using jetting technology. The spacer and memory module are secured with standard, screen printed die attach epoxy. The module is encapsulated with 83% silica filled epoxy using an automatic rotary displacement pump process. Each module is individually tested and finally sawn from the panel into final form. The BGA module is then populated onto the flex substrate along with other surface mount components to achieve the final flex SMD assembly.

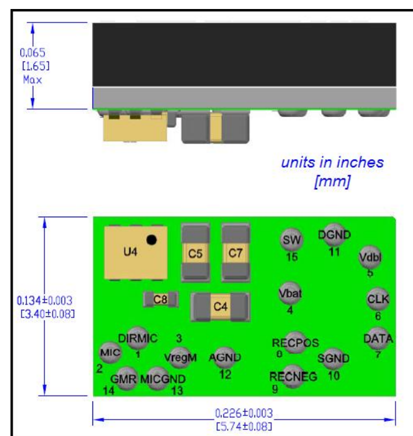

Figure 2: Thick film module side and bottom view.

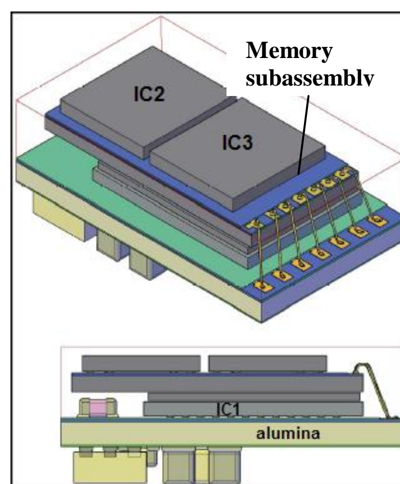

Figure 3: Thick film module internal view. Encapsulation and BGA bumps are not shown.

Test Protocol

Designing appropriate reliability tests for hearing aid components and assemblies is a continually evolving process, not to mention a challenging one. Our customers typically do not specify test requirements; rather we must develop and refine meaningful tests that can be depended upon to guide the design team. Table 1 shows the primary design verification tests (DVT) we used to evaluate the prototypes.

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Table 1: Microelectronic DVT Matrix

Description	Purpose	Conditions
Solder Stress	Determine how well module endures the rigors of subsequent soldering operations; resistance to delamination.	3x convection solder reflows at module level. Parametric electrical test before and after, followed by ink penetration test to identify delamination.
Accelerated Aging	Establish an estimated mean time-to-failure in the field and determine if circuit is resistant to electromigration.	85˚C, 85% Rh, bias applied for 8 days. Quiescent current monitored continually. Parametric electrical test before and after.
Ink Penetration	Qualitative understanding of the modules' resistance to delamination.	Destructive test typically performed after solder stress test. Apply red ink to external surfaces. Cleave part open and examine internal surfaces.
Bend Cycle Testing	Determine if SMD assembly will survive folding installation and rework during final device assembly.	IPC 6013. Performed at the raw flex circuit level and the populated SMD assembly level.

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The mantra was "test early and often" during development, however, it required a considerable effort to manage and execute. DVT was performed both by design and process/quality personnel to help transfer knowledge about new products to the quality and process engineers early in the development cycle. Prototypes were built by engineers and technicians using production equipment and tested at various points during the prototype assembly process. Test sample sizes generally were 20-40 circuits per test. Each time a change was made to the design layout, materials, or assembly method, a new batch of prototype circuits was built and retested – each of these new batches is referred to as a spin.

Spin 1 Result: Delamination

The solder stress test was the first reliability test performed on BGA modules following electrical parametric testing. The solder stress test consists of subjecting the circuits to 3 successive convection oven reflow cycles and a post electrical test. This test simulates the rigors of the manufacturing process including rework and is an indicator of circuit robustness. Nearly 100% of the modules failed the post electrical test. Ink penetration testing of the failed circuits revealed that severe delamination occurred between the underfill epoxy layer and the top dielectric layer of the alumina substrate. The delamination caused electrical failure due primarily to fractured solder joints and cracked microvias within the dielectric structure. A thorough review the BGA assembly process revealed a primary suspect: underfill variation as shown in Figure 4. Anecdotal evidence suggested that insufficient underfill would cause delamination – but a better understanding of underfill's role in the hybrid's thermo mechanical performance was needed.

To accomplish this we turned to Finite Element Analysis (FEA) – a powerful tool that enabled engineers to study the effects of multiple factors on hybrid thermo mechanical behavior without having to build and test many prototypes.[2] FEA enabled us to study how underfill amount and location affected the interfacial stress present at the underfill-dielectric interface during the solder reflow process. Different underfill materials were also characterized. Figure 5 shows a snapshot from one of the many stress animations that were run. This type of FEA output was useful because it provided a simple visual representation of complex behavior. Insight into the difference between adequate underfill and insufficient underfill was attained. This led to a better definition of underfill jetting requirements.

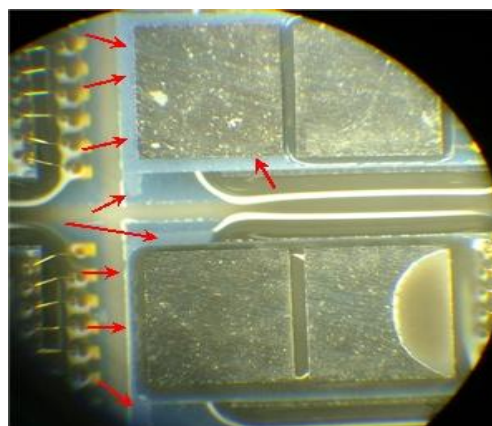

Figure 4: This photo shows typical variation in the amount of wet underfill epoxy observed immediately after jetting on a spin 1 prototype. The red arrows indicate regions where underfill is missing.

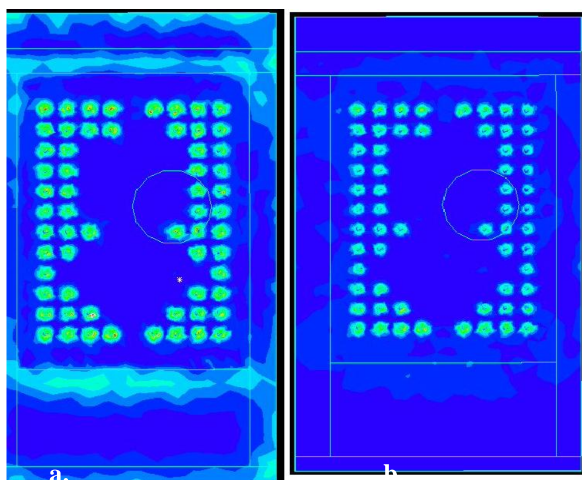

Figure 5: Snap shots from FEA stress animations showing effects of a) insufficient underfill, and b) adequate underfill. Light blue and yellow colors show areas of higher stress that accumulates during the reflow solder process. The plane shown is the interface between the DSP flip chip solder bumps and the ceramic substrate within the BGA module.

Through the use of FEA analysis it became clear that the price of insufficient underfill was higher stress along the edge of the BGA package. We also learned that an FR4 memory PCB would perform better than a ceramic memory substrate, however, FR4 substrates were not readily available so the option was saved for later if necessary. Once the underfill process was optimized we were able to continue by building a batch of improved BGA modules with uniform underfill and continuing with the evaluation process. The spin 2 parts passed the solder stress test and were then subjected to the remaining DVT tests.

Spins 2-6: 85/85 Test Results

The next hurdles the team encountered came after the improved BGA modules were populated onto flex circuit assemblies and subjected to the accelerated aging test, aka. "85/85" test. The purpose of this test is to gain an understanding of how well the microelectronic package will survive in the field. An accelerated aging equation based on the Arrhenius equation was used to calculate an acceleration factor as follows:

$$\alpha = e^{\{Ea/k * (1/T1 - 1/T2) + B * (1/U1 - 1/U2)\}}$$

Where α is the acceleration factor, Ea = 0.65 eV is the activation energy for silver, k = Boltzman's constant, T1 = 303˚K is the device average working temperature, U1 = 0.5 is the average working humidity level, T2 = 358˚K is the test temperature, U2 = 0.85 is the test humidity, and B = 0.288 is a unit-less humidity constant. The acceleration factor is therefore 57.9, and since hearing instruments are used about 16 hours per day, we estimate that the complete 8 day test simulates nearly 2 years (23 .1 months) of actual use. There are a number of reasons why this equation may not predict reality, a primary one being that it assumes constant Ea with temperature which is usually not true due to multiple failure mechanisms. Given these short comings, we prefer to use the equation to make a relative comparison of new circuit performance to that of an established product for which both 85/85 data and field performance data are available.

Just as there are complications regarding 85/85 theory, the practical matter of test execution is not without problems. It is imperative that the samples be prepared for test carefully to avoid introduction of contamination. The test chamber must be very clean. The voltage supply to each circuit must be uninterrupted; we use a 100 Ω resistor in series with each circuit to reduced likelihood of dendrites forming and then breaking due to fusing action.

The test goal for new circuits is zero failures after 8 days at 85C/85% Rh, with nominal supply voltage applied during test – typically 1.3 Vdc. The circuit must be free of abnormal drain current fluctuations during test (< 25 µA changes) and pass parametric electrical test before and after 85/85.

Multiple failure mechanisms were identified during the 85/85 test phase which required a number of fix and retest cycles. The graph in Figure 6 shows the 85/85 results for each successive spin. Following is a discussion of the findings and corrective actions taken for each of these design spins.

Spin 2 Results – Silver and Copper Dendrites

12 of 19 circuits failed due to highly variable drain current observed during the 85/85 test. Experience suggested that metal migration was probably responsible for drain current fluctuations so we searched for dendrite shorts between different electrical nodes. The circuits were removed from the biased test, visually examined (no obvious failure mechanism found), and then subjected to parametric electrical test. Destructive failure analysis (FA) was carried out by carefully microsectioning the module and stopping frequently for high magnification microscopy and continuity testing using a manual microprobe station and multimeter. The primary problem cause was traced to silver dendrites that had grown vertically between metal 2 and metal 3

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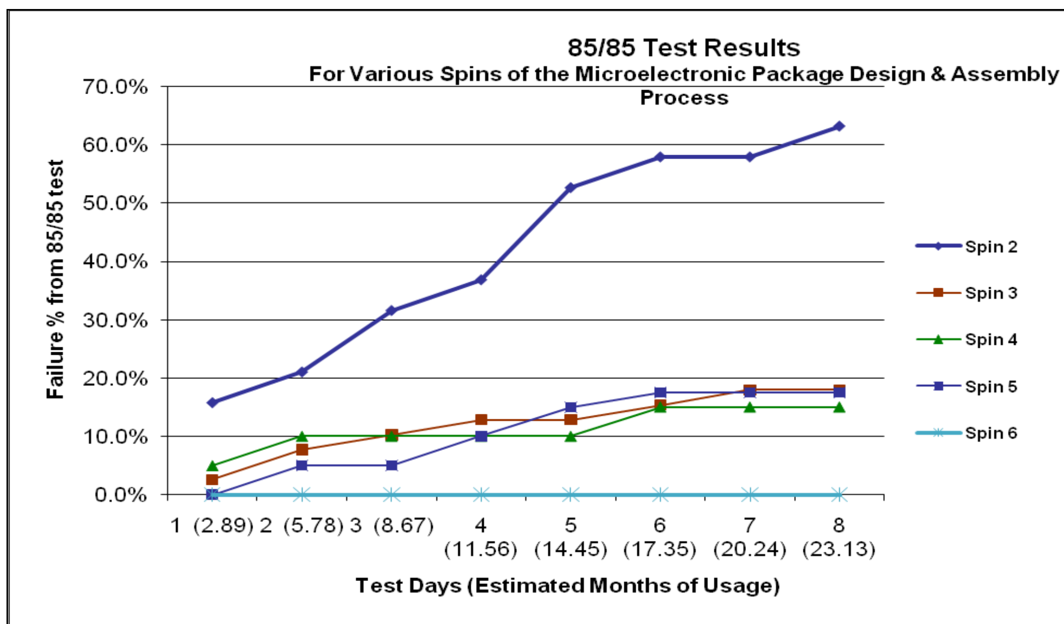

Figure 6: Graph showing % failure from the 85/85 test results for successive prototype builds.

layers within the thick film BGA dielectric structure as shown in Figure 7. Water and electrical potential are the only two ingredients required to initiate silver migration between silver thick film conductors as described by K. Vu [3]. Many of the dendrites grew from a ground trace in metal-layer 3 to microvias in metal- layer 2 with an electrical potential of about 1.3 VDC between them and separated by as little as 1-5 microns of dielectric in the worst case areas. Typical dielectric separation is ~ 20 microns. The microsections revealed that the thick film microvias were printed too high which reduced the dielectric thickness, enabling silver to migrate through this precariously thin dielectric. These dendrites tended to be clustered along the circuit edge, we assumed, because moisture more readily penetrated these areas. Several copper dendrites were also found growing between solder bumps on the flex underneath the BGA module. This was caused by poor solder mask registration (which exposed copper) and was readily corrected by the flex supplier. Recalling the earlier FEA results, we decided to replace the ceramic memory substrate with an FR4 PCB substrate to further reduce thermal stress making it less likely for the dielectric to crack. The other remedies included reducing the amount of via fill during the thick film printing process and modifying the thick film module layout slightly by moving buried vias further away from the diced edge.

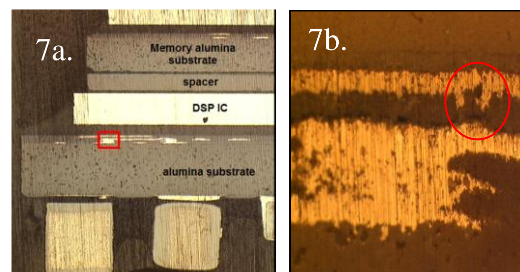

Figure 7: a) Photograph of a defective BGA module in cross section at 50x magnification. The red box shows the dendrite area. b) Dendrite area at 1000x magnification. Silver migration is visible within the red circle.

Spin 3 Results- Copper Dendrites on Memory Substrate

Spin 3 circuits showed a notable improvement in 85/85 testing, but as Figure 6 shows several failures still occurred – again with symptoms of fluctuating drain current and shorts between nodes. Following the same FA process, faults were isolated to two primary locations where again dendrites were found. But this time the dendrites were copper! They had grown between adjacent bond pads on the memory PCB substrate (Figure 8).

Why had copper dendrites grown on the PCB substrate when it was completely encapsulated within the BGA module? Raw memory PCB's were scrutinized with an optical microscope, but no clues were found; neither contamination nor exposed copper was present. The mystery was solved by

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SEM/EDS analysis which revealed that the bond pad edges were totally free of the specified nickel/gold plating, exposing copper along this surface. In this application two adjacent bond pads supply 2 V DC to the memory module. With a spacing of 100 μm between pads, the effective electric field strength is 500V per inch, making these pads vulnerable to copper migration. So we hypothesized that copper migration could readily occur between bond pads due to the exposed edge copper. A simple water drop test was conducted to test this hypothesis following the method outline in IPC Test Method 2.6.13 [4]. A bare PCB as received from the supplier (with exposed copper along the bond pad edges) was tested against a thick film ceramic substrate. The bond pads of the ceramic substrate were made of conventional thick film gold at a fired thickness of ~10 μm with size and pitch similar to the PCB.

A drop of deionized water was placed atop adjacent bond pads which were energized with a 2VDC potential via a probe station while the pads were observed through the probe station's optical microscope. To our surprise copper dendrites grew from the negative pad to the positive pad within 7-30 seconds! See Figure 8b. In contrast, no metal migration occurred on the thick film substrate after 30 minutes with water and voltage applied. We even tested a slightly different PCB design from another supplier and found that no dendrites formed after 30 minutes between bond pads – the only difference being that the gold plating coverage on the bond pads was uniform. Here is a good point for a more detailed explanation of the copper migration failure mechanism.

Copper (Cu) migration failure mechanism is similar to silver (Ag) migration and is an electrochemical process. When copper is in the presence of an electric field in a high humidity condition on an insulator, it will re-deposit at a different copper location through iconic transport. This mechanism can be broken down into 3 steps of a chemical reaction:

- Electrodissolution
- Ion transport
- Electrodeposition

Application of voltage in a humid condition yields the following reactions: (Electrodissolution)

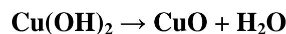
$$Cu(s) \rightarrow Cu^{2+}(aq) + 2e^-$$

$$H_2O \rightarrow H^+ + OH^-$$

Hydroxide (OH^-) moves towards the anode as the Cu^{2+} ion moves away from the anode. OH^- encounters the Cu^{2+} and reacts: (Ion transport)

$$\mathbf{Cu^{2+} + 2OH^- \rightarrow Cu(OH)_2}$$

$Cu(OH)_2$ is unstable and decomposes on the cathode: (Electrodeposition)



$$\mathbf{Cu(OH)_2 \rightarrow CuO + H_2O}$$

$$\mathbf{CuO + H_2O \rightarrow Cu(OH)_2 \rightarrow Cu^{2+} + 2OH^-}$$

It was obvious that a memory PCB with exposed copper along the bond pads was unacceptable even though the PCB was fully encapsulated; in other words exposed copper was the only culprit – or so we thought. We hypothesized that moisture vapor diffused through the diced edge of the encapsulation and onto the bond pads of the memory PCB providing the electrolyte necessary for copper migration. Unfortunately, the PCB supplier was unable to implement timely corrective action so the design team chose to revert back to the ceramic memory substrate instead of the PCB. With renewed confidence we proceeded to build what we thought would be the last prototype batch, unaware that we had missed a subtle, but ultimately important, contributing factor.

Spin 4 Results: Silver dendrites on memory substrate.

As the graph in figure 6 shows, the spin 4 test results with the ceramic memory substrate were disappointing and about the same as spin 3. This time dendrites were found between the gold wire bond pads of the thick film memory substrate. They were confirmed by carefully lapping down through the BGA's encapsulation and stopping just above the bond pads so as not to disturb the fragile dendrites that were only several microns below. See Figure 9.

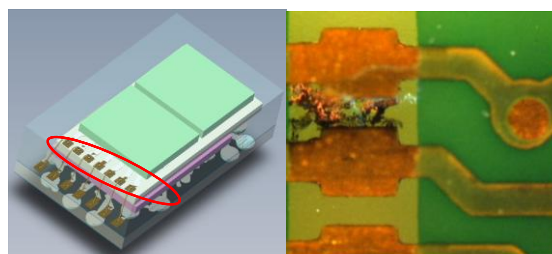


Figure 8a. **Figure 8b.**

Figure 8: a) Internal view of BGA design showing the wire bond pads of the memory module where dendrites formed. b) A copper dendrite that grew between wire bond pads on the bare memory PCB during a water drop test.

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SEM/EDS analysis confirmed the dendrite composition was primarily silver and gold. The silver had migrated from the nearby overlap region between the gold bond pad and connecting palladium silver trace. Memory module subassemblies were removed from the build area, just prior to assembly into the BGA module, and examined both optically and using XPS [5]. Optical inspection revealed a thin, oily film on the bond pads; the film was believed to be compounds that had bled out from the underfill fillet. XPS revealed high concentrations of sodium chloride and organic compounds on the thick film memory substrate; particularly around the gold wire bond pads. Had this condition also existed in the samples of the prior spin when dendrites formed on the PCB memory substrate? Quick examination of the prior spin 3 samples gave us the answer: yes, we had missed this contamination. We identified several possible ways the oily film might aid silver migration: a) by behaving as an electrolyte, b) interfering with encapsulation adhesion allowing moisture to penetrate, c) trapping ionic contamination, or d) a combination of these three.

The sodium chloride contamination was traced to the dicing saw which had been plumbed improperly to a water conditioner. The problem was corrected by fixing the plumbing and modifying the rinse method. The organic material on the pads was traced to "bleed out" from the underfill epoxy fillet as expected – the underfill fillet had extended too close to the bond pads. A new underfill material was found to produce better results due to the smaller fillet it produced and its color which made it easier to inspect.

Added design margin was achieved by increasing the spacing between the power supply pads to 200 µm. Again another prototype batch was produced with these modifications and with hope that this would be the last prototype run.

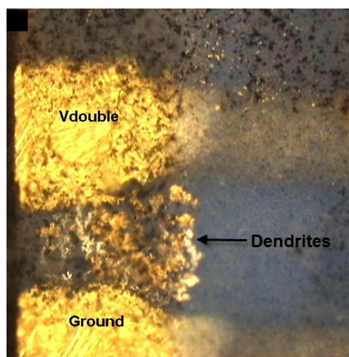

Figure 9: 85/85 test failure with dendritic growth visible between bond pads on the ceramic memory substrate. 200X.

Spin 5 results: Interlayer silver dendrites

The spin 5 circuits suffered a similar fate to the previous runs. The results were better during the first several days of test, but by the end of the 8 day test 7 of 40 circuits had failed as shown in Figure 6. This time an electrical short was traced to one specific location within the BGA dielectric structure. Silver migration had again occurred between layers, from a metal 3 ground trace down to a metal 2-3 via at a 1.3V DC potential difference. This time however there was an added complication. Small cracks were visible in the dielectric layer along the externally diced edge near the dendrite site. These cracks were believed to be the entry point for water vapor during the 85/85 test. It was an interesting coincidence that cracks were found in samples with thicker underfill bond lines as shown in Figure 10. The prior FEA work had shown that thicker underfill tended to induce higher localized stress so we decided to reduce the underfill thickness to 25-50 µm by further tuning of the underfill jetting process. Also, the dicing saw feed rate was reduced slightly as a preventive measure.

Finally, Spin 6 and two successive batches of prototypes passed the 85/85 test bringing a successful conclusion to the design verification phase.

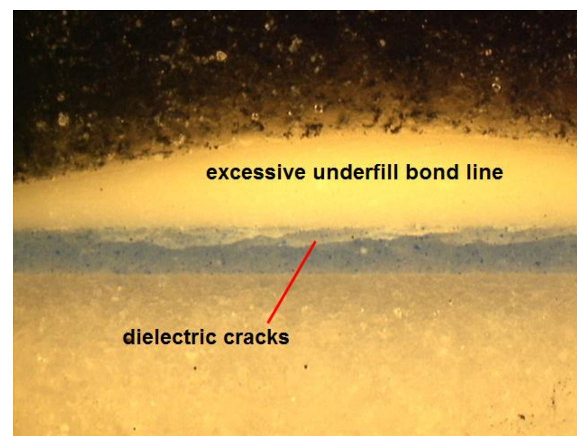

Figure 10: External side view of module showing cracks in the blue dielectric of an 85/85 test failure at 200x. Silver migration was found inside the component near this cracked region. Underfill bond line of 100-125 microns was deemed excessive.

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Conclusion and Lessons Learned

A novel thick film multichip module-on- flex microelectronic package was described. A detailed account was given of the design verification tests, FA findings, and corrective actions implemented to achieve a robust package.

The FA process was challenging due to time constraints and the logistics involved with designing, building, and evaluating a new product in facilities across the globe. There was much learning on the fly along with a few ventures down the wrong path. Several samples were ruined during the cross sectioning process before the location of the fault was found. High resolution real time X-ray proved ineffective because the dendrites were too small to be resolved amidst the closely packed routings, vias, and connection pads within the circuit. Also during the FA process we sometimes missed other secondary failure mechanisms as we focused on the primary faults. Time constraints sometimes prevented us from performing follow up experiments to answer unresolved questions. Solving this problem took the combined knowledge of the system and test engineers, circuit designers, process engineers, and quality assurance FA experts–all dedicated resources within our company. We also collaborated with an outside failure analysis lab – this proved to be an invaluable partnership. They provided the SEM/EDS and XPS tools and expertise, while we provided the product knowledge and investigation details. Together we asked many questions along the way. Following is a list of the essential lessons learned from this development project:

1. Scrutinize the product before and after critical assembly operations (such as thick film via printing and underfill dispensing) during initial prototype builds to help identify issues sooner. Do not assume that design details are entirely understood. Question variation when it is observed and follow up with analysis to determine if the variation is problematic.
2. Conduct FEA as soon as possible in the development process, preferably before building prototypes. Use this tool to help answer questions about anticipated problems or variations (such as underfill voids and excess underfill).
3. Conduct design reviews and include QA and failure analysis experts in these activities. They can provide useful suggestions for avoiding problems and they become more familiar with the product before crunch time later when prototypes are built and fail.
4. Take care to specify complete gold (or suitable alternative plating) coverage for bond pads and other connection pads on flex and rigid PCBs even if the PCB is designed to be fully encapsulated at a later operation. No exposed copper! Discuss this with the PCB supplier and verify complete plating coverage with SEM/EDS or other analytical technique upon receipt of the PCBs. Do not rely on standard optical inspection.
5. Perform a water drop test for dendrites on raw PCBs or ceramic substrates. If possible, repeat this test on partially assembled parts at key steps in the build process. This test is rather simple and fast. It is very difficult to identify contamination and its source later on during destructive analysis.
6. Have two options available when possible. Developing two memory substrates (PCB vs. ceramic) and having two underfill types (old vs. new) proved to be a prudent move.
7. Consider using a DOE approach rather than the 'one factor at time' approach we followed here. We likely would have come to the final product revision sooner had we followed a structured DOE methodology.

Acknowledgements

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