High Yield, Near Void-Free Assembly Process of a Flip Chip in Package Using No-Flow Underfill

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Abstract

The advanced assembly process for a flip chip in package (FCIP) using no-flow underfill material presents challenges with high I/O density (over 3000 I/O) and fine-pitch (down to 150 µm) interconnect applications because it has narrowed the feasible assembly process window for achieving robust interconnect yield.

In spite of such challenges, a high yield, nearly void-free assembly process has been achieved in the past research using commercial no-flow underfill material with a high I/O, fine pitch FCIP. The initial void area (approximately 7%) could cause early failures such solders fatigue cracking or solder bridging in thermal reliability. Therefore, this study reviewed a classical bubble nucleation theory to predict the conditions of underfill void nucleation in the no flow assembly process. Based on the models prediction, systematic experiments were designed to eliminate underfill voiding using parametric studies. First, a void formation study investigated the effect of reflow parameter on underfill voiding and found process conditions of void-free assembly with robust interconnections. Second, a void formation characterization validated the determined reflow conditions to achieve a high yield and void-free assembly process, and the stability of assembly process using a large scale of assemblies respectively.

This paper presents systematic studies into void formation study and void formation characterization through the use of structured experimentation which was designed to achieve a high yield, void-free assembly process leveraging a void formation model based on classical bubble nucleation theory. Indeed, the theoretical models were in good agreement with experimental results.

Key words:
Void nucleation, Flip chip, fine pitch, high I/O density, no-flow underfill, void formation

1. INTRODUCTION

Increasing demands on high performance devices has drawn attention on the Flip Chip in Package (FCIP) technology in electronics packaging industry. The advanced electrical, thermal, and form fact performance of Flip chip in package (FCIP) technology enables it to be widely used in high performance device packaging solutions such as microprocessors, graphic devices, and high speed memory applications with high I/O density (over 3500 I/O) and fine pitch (down to 150 µm) with a full area array of interconnect structures. In spite of such challenges comprising high-lead solder bumps with eutectic lead-tin solder interconnects, an assembly process was recently developed using no-flow underfill material in our previous research [1-3]. The no-flow underfill material can achieve metallurgical solder interconnects and underfill curing simultaneously during a single reflow process as illustrated in Fig. 1 [4, 5]. Indeed, the illustrated no-flow assembly process accomplished the high, stable yield with the high I/O, fine pitch FCIP. Meanwhile, a large number of voids were observed, that could cause critical defects such as solder bridges and solder joint cracks possibly resulting early failure in thermal reliability [6-10]. The underfill voiding among solder joints was observed using an optical micrograph of a cross section of FCIP structures in Fig. 2-(a) and (b). In addition, a C-mode Scanning Acoustic Microscopy (C-SAM) in-plane view confirms multiple void areas in the underfill between the test ASIC and substrate as shown in Fig. 2-(c).

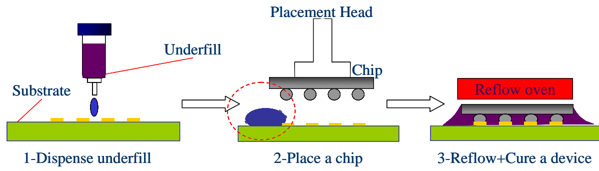
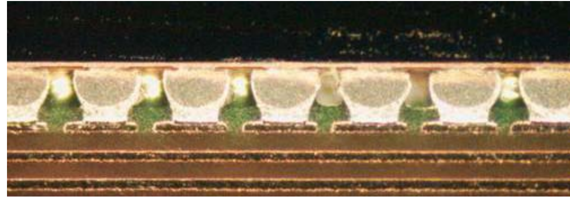
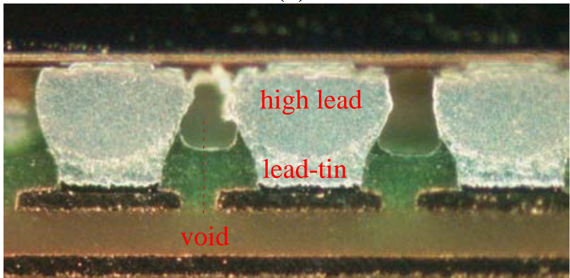


Fig. 1 Flip chip assembly process using a no-flow underfill[17]



(a)



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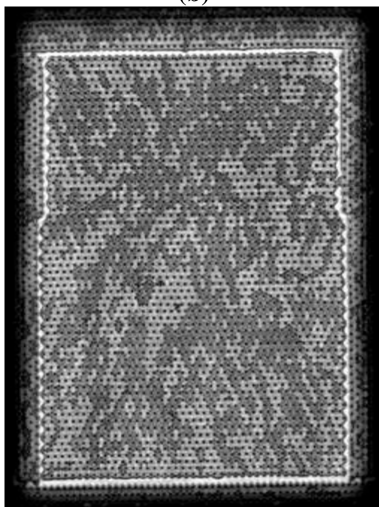

(c)

Fig. 2 Micrographs of FCIP built using no-flow underfill material under the reflow conditions of ramp rate: 2.1 °C/s, reflow time: 70sec, peak temp: 225 °C; (a) cross-sectional view of flip chip solders joints (magnification: 100X), (b) Cross-sectional view of flip chip solders joints(magnification: 200X), and (c) C-SAM analysis[17]

Actually, a large number of researches have been thoroughly identified the causes of void formation in flip chip assemblies. Mainly the causes of void formation can be classified into thermally-induced voids and non-thermally induced voids [4, 11-16]. Among them, previous our study investigated the plausible sources of void formation for the current large number of underfill voiding patterns by focusing on thermal effects from the reflow process. Moreover, the mechanism of underfill voiding was suggested[17]. The study explained that the fluxing agent in no-flow underfill is exposed to temperatures above its boiling point during soak zone for fluxing activation in the reflow process, causing underfill voiding. Namely, the voids were induced by chemical reactions between solder wetting and underfill curing. Furthermore, a general void formation mechanism was suggested to explain the current large amount of no-flow underfill voiding with a high I/O, fine pitch flip chip. Besides, the presented chemical models identified the soak zone was the significant factor on the underfill voids. Afterwards, a study was conducted to investigate the effect of soak temperature and soak time on voiding using a statistical analysis [7, 18]. The analysis found the low soak temperature and high soak time could decrease underfill voiding from 64% to 7% [2, 3, 7, 17, 18]. However, the 7% void could prevent from achieving a void-free process for high reliability performances. Therefore, this study was conducted to investigate the effect of plausible dominant factor, peak temperature on underfill voiding and solder wetting on the classical nucleation theory using parametric studies. Thus studies could predict a reflow process condition to improve voiding characteristics with robust wettability. Eventually, this novel research achieved the high, stable yield and void-free assembly with a good agreement between experimental results and theoretical models

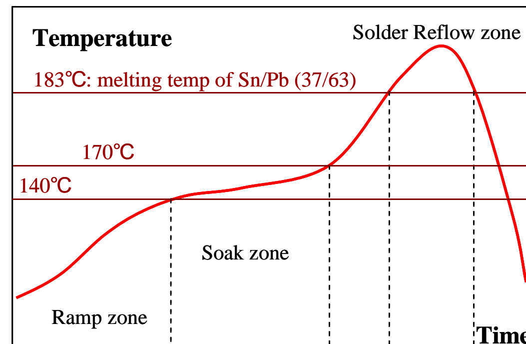

Fig. 3 A typical no-flow underfill reflow profile

2. HETEROGENEOUS VOID NUCLEATION THEORY

The mechanism of voiding in FCIP will be modeled on the classical nucleation theory [19-23]. The Nucleation means the formation of fluctuations in phase transitions. After the critical nucleus is formed by the phase transitions, one becomes so large that it is stable and the nucleus will grow to

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macroscopic dimensions. A schematic of void nucleation during the reflow process is illustrated in Fig. 4. In general, the formation of a void has an associated excess energy equal to the Gibbs free energy of void formation. The change in Gibbs free energy during a gas formation is given by the energy associated with forming a new interface the among solder, the no-flow underfill, and the void plus the volumetric work performed to produce the volume of a void. This energy change in Gibbs free energy for the application of FCIP happens on the smooth surface of hot molten solder as illustrated in Fig. 4 under heterogeneous nucleation, assuming a reversible, isothermal thermodynamic process. The heterogeneous nucleation accounts for void nucleation on the smooth solder surface, given by equation (1).

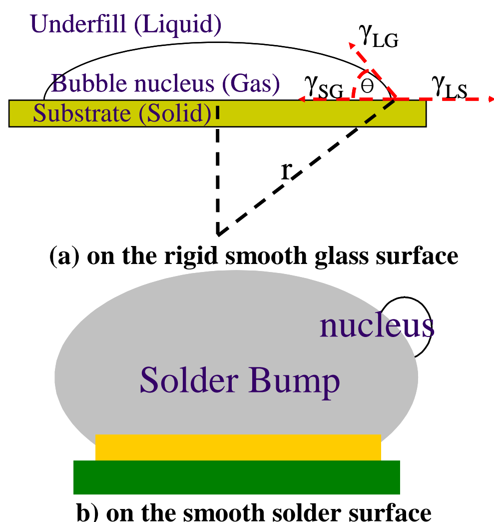

Fig. 4 The schematic of heterogeneous bubble nucleation on smooth surface

$$\Delta G_{het} = -V_G \Delta P + \gamma_{LG} A_{LG} + \gamma_{SG} A_{SG} - \gamma_{LS} A_{LS} \quad (1)$$

$$A_{LG} = 2\pi(1-\cos\theta)r^2 \quad A_{SG} = \pi(\sin^2\theta)r^2$$

$$A_{LS} = \frac{\pi}{3}(2 - 3\cos\theta + \cos^3\theta)r^2$$

where V_G is the volume of the void, ΔP is the difference in the pressure of the gas in the void and the environmental nucleation pressure, γ is interfacial surface energy between liquid and gas (LG) or solid and gas (SG) or liquid and solid (LS), and r is a spherical void of radius on the solder bump. Thus, equation (1) can be written as

$$\Delta G_{het} = \left[-\frac{4\pi r^3}{3}\Delta P + 4\pi r^2 \gamma_{LG} \right] S(\theta) \quad (1)$$

where $$S(\theta) = \frac{(2+\cos\theta)(1-\cos\theta)^2}{4}. \quad (2)$$

The equation (2) determines the maximum of the Gibbs free energy where

$$\frac{d(\Delta G_{het})}{dr} = 0 \qquad \frac{d^2(\Delta G_{het})}{dr^2} < 0$$

yielding the critical radius of void

$$\therefore r_C = \frac{2\gamma_{LG}}{P_G - P_L} = \frac{2\gamma_{LG}}{\Delta P}. \quad (3)$$

The Gibbs free energy change for critical void is achieved by plugging equation (4) into equation (2) and then yielding

$$\Delta G^*_{het} = \frac{16\pi\gamma_{LG}^{\ 3}}{3\Delta P^2} S(\theta). \quad (4)$$

Next, the heterogeneous nucleation rate N_{het} equation (6), the rate of formation of voids per unit time per unit volume, will be used to predict the number of voids in the flip chip.

$$N_{het} = Cf \exp\left(\frac{-\Delta G^*_{het}}{kT}\right) \quad (5)$$

where C is concentration of available heterogeneous nucleation sites, f is frequency factor of gas molecules, and k is Boltzmann's constant. The ΔG^*_{het} is given by equation (5). The natural logarithm of equation (6) is taken, yielding

$$\ln N_{het} = \ln\left[Cf \exp\left(\frac{-\Delta G^*_{het}}{kT}\right)\right] \quad (6)$$

$$\ln N_{het} = \frac{-\Delta G^*_{het}}{k}\frac{1}{T} + \ln Cf. \quad (7)$$

Thus, equation (8) will release the Gibbs free energy and $\ln Cf$ using an Arrhenius equation as shown in Fig. 5. The solid line and dot of Fig. 5 corresponds to a nucleation model and an experimental validation by counting the number of nucleation voids with respect time in unit area, respectively. Thus, the nucleation equation could predict the number of voids depending on temperature with a good agreement between model and experiment. The prediction model indicates zero number of voids in nucleation rate at around 204 ºC. Namely, the temperature might not provide enough energy to nucleate bubbles. Actually, the majority of model constants of equation can not be controlled by modifying process parameters in actual assembly process. Among them, the controllable process parameter is the temperature of a reflow process affecting the nucleation rate and solder wettability in flip chip assembly. Therefore, this study was designed to determine the process conditions to minimize underfill voiding with robust wetting for assembly yield regarding the peak temperature of a reflow process.

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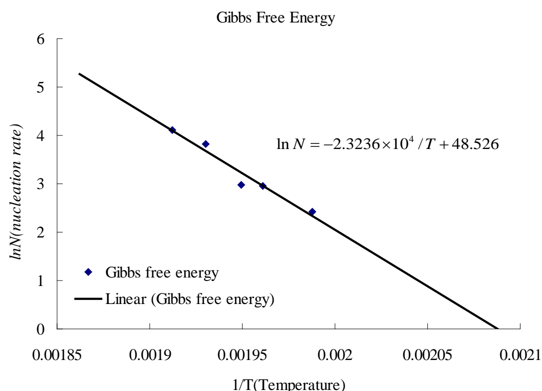

Fig. 5: Void nucleation rate versus 1/T(Temperature)

3. EXPERIMENT

The objective is to validate the critical temperature of void nucleation calculated on the classical theory. Below the critical temperature, a process condition would be determined to enable solder wet in assembly process using a commercial underfill material (see Table 1). Eventually, the no-flow underfill could achieve a high, stable yield and void-free assembly process. Therefore, a void formation study was designed to find process conditions to minimize underfill voiding with a robust solder wettability using simple structured test vehicles as described in Table 2. The voiding and wettability are mainly depending on the reflow parameters as illustrated in Fig. 3. Among the parameters, peak temperature is a susceptive factor affecting both voiding and wettability. In addition, the nucleation temperature would correspond to the peak temperature of a reflow profile. From this hypothesis on the previous research and nucleation theory, the void formation study investigated the effect of peak temperature on underfill voiding. Afterwards, a void formation characterization was conducted to determine the best reflow process conditions to minimize the underfill voiding using a high I/O, fine-pitch flip chips as described in Table 2. Then, the large scale assembly validated the stability of a high, stable yield and void-free assembly process with 30 assemblies of a high I/O, fine-pitch flip.

Table 1 Material property of No-flow underfill[17]

Material property	Value
Glass transition temperature (Tg)	81 °C
Viscosity @ 25°C	3,100 cp
Flexural modulus	2.6 GPa
Thermal conductivity	0.18 W/mK
Coefficient of thermal expansion below Tg	190 ppm/°C
Cure condition	a standard SMT reflow incorporating a 150-170°C dwell prior to ramp to reflow temperature

Table 2 Configuration of test vehicles used in the void formation study and void formation characterization

Experiment	Category	
Void formation study	Die material	Glass cover
	Substrate size(cm)	1x1
	Substrate material	ENIG
	Underfill	No-flow underfill
	Bond pad	37Pb-63Sn
Void formation characterization	Bump material	97Pb-3Sn
	Chip size(mm)	< 10 x 10
	Bump count	3000 >
	Bump pitch	< 200μm
	Bump layout	Full area

3.1 Void Formation Study

This study investigated the effect of peak temperature on underfill voiding and solder wetting. Prior to the assembly process, all moisture was driven out of the boards with exposure to an isothermal environment at 125 ºC for 3 hours. This bake out time was determined from a previous bake out experiment and was sufficient to avoid moisture out-gassing of the boards [24], [25]. Next, no-flow underfill was dispensed on the test vehicle and a cover glass was put on the underfill deposited test vehicle. Then, the test vehicles were reflowed at four levels of peak temperature (180,190,200, and 220 °C) with three replicates. The levels of temperature were determined to investigate the temperature of void nucleation. After the melting of Sn/Pb (63/37) solders, the test vehicles were held for three minutes at

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constant temperature. Typically, 90 seconds was used for solders reflow time in an actual assembly process.

During the reflow process, underfill voiding was investigated using a visual microscopy technique. The technique was also applied to examine whether the solder completely wet at each temperature levels. Thus, a critical nucleation temperature could be determined at the limit which no voids were observed on the test vehicles. Furthermore, the temperature would be the limit of assembly process, peak temperature, at which Sn/Pb (63/37) solders did not melt. The process conditions were characterized to determine the robust process conditions for high and void-free assemblies in the void formation characterization.

3.2 Void Formation Characterization

Void formation characterization validated whether the determined peak temperature, enabling Sn/Pb (63/37) solders wet without producing outgassing voids using a commercial high IO, fine-pitch flip chip in package (FCIP) as described in Table 2. The commercial FCIP tested the reflow process conditions which have two levels in the peak temperature of reflow parameters using parametric studies. The other parameters were determined by the past research achieving a high, reliable yield assembly process [2, 3, 7] as described in Table 3. Thus, this study determined the best reflow process conditions for a high yield and void-free assembly process. Besides, the stability of assembly process was validated for a high yield and void-free condition using large scale assemblies since the achieved assembly process needs to be considered for the application of a mass production. The quantity might be enough size to predict the result of mass production prior to actual assembly process on statistics.

Table 3 Design matrix for void formation study

	Ramp Rate °C/s	Soak Temp °C	Soak Time s	Temp. Above Liquidous °C	Time Above Liquidous s	Peak Temp
Level 1	1.3	120 ~130	120	>170	90	180 °C
Level 2						190 °C

Prior to the assembly process, all moisture was driven out using the same methodology used in the void formation study. Next, the plasma pretreatment for substrate surface cleaning was applied to the moisture free FCIP test vehicle using pure argon (Ar) for 10 minutes to remove contamination. Then, high I/O, fine pitch flip chips were assembled using a commercial no-flow underfill on the process conditions described in Table 3. Afterwards, the process conditions were evaluated by testing the electrical continuity and measuring void percent area respectively.

Finally, the void formation study and void formation characterization study determined the best reflow process conditions for a high, stable yield and void-free assembly process using experimental techniques for the application of mass production.

4. RESULTS and DISCUSSIONS

The void nucleation theory predicted the voids would form above 204ºC. From theoretical expected temperature range, the four levels of temperature were designed and evaluated using the void formation study. The experimental technique investigated four temperatures to find the critical nucleation temperature of void formation and the temperature limit of eutectic solder wetting. Consequently, the founding was that voids nucleated above 200ºC and solders could melt at around 190 ºC. Namely, small discrepancy observed between theory and experiment. Next, the void formation characterization examined two process conditions using a commercial high I/O, fine-pitch FCIP. The FCIP simultaneously achieved the high yield and void-free assembly process in both cases. Using one of condition with 190 ºC peak temperature, a large scale of assemblies validated the stability of process condition. Eventually, a series of systematic experiments developed a high yield, stable yield and void-free assembly process on the classical bubble nucleation.

4.1 Void Formation Study

The void formation study was conducted to investigate the effect of reflow process parameter such as peak temperature on the void formation using parametric studies. This study considered temperature from 180 to 220ºC, determined on the predicted nucleation temperature. At 180 and 190 ºC, no voids were observed as shown in Fig. 6-(a) and (b) respectively. On the contrary, a void and a large number of voids were observed in Fig. 6-(c) and (d) at 200 and 220 ºC respectively. Namely, voids could be nucleated above 200 ºC on this experimental study. Thus, the void nucleation temperature was determined using experimental investigation. Regarding wettability, solders completely wetted except for 180 ºC peak temperature. Therefore, the temperature range associated with (a) and (b) could be a good candidate for a high yield and void-free assembly process.

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Electroless Nickel Immersion Gold (ENIG) (Cu/Ni/Au)

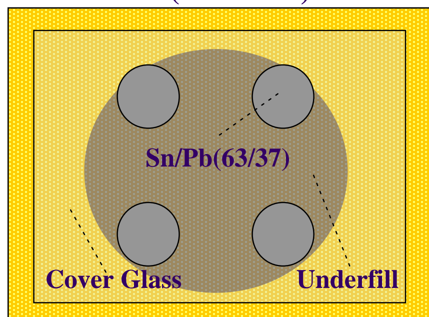


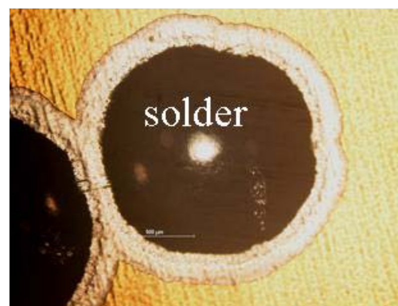
Fig. 6 Configuration of test vehicle for void formation study

On the conclusion, the void formation study found the peak temperature had strong effect on underfill voiding and solder wetting using parametric studies. In addition, the baseline for peak temperature was determined to accomplish a high yield and void free assembly process in void formation characterization.

4.2 Void Formation Characterization

No voids were observed in both reflow conditions as shown in Fig. 7. Simultaneously, both reflow process conditions achieved 100% interconnections. Afterwards, the stability of assembly process was validated regarding assembly yield and void characteristic. The validation was conducted on the level 2 (see Table 3), using high level in peak temperature. Consistently, no voids were observed and the yield loss did not occur in every assembled part. Eventually, a process condition was successively determined for high, stable yield and void-free assemblies.

(a)



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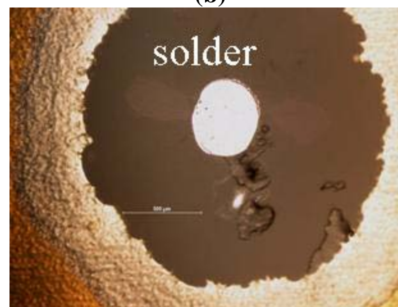

(c)

(d)

Fig. 7 Micrographs of void formation study at : (a) 180 °C, (b) 190 °C, (c) 200 °C, and (d) 220 °C

5. CONCLUSION

In general, void nucleation occurs on the interface between solder and underfill if the released energy exceeds the critical energy of void formation. The void formation energy is associated with material properties of no-flow and solders, and process conditions such as pressure and temperature. The temperature was an efficient way to control void nucleation from a process stand point. Consequently, the reflow process was a control parameter of void nucleation by modifying parameters in the reflow profile such as soak zone time/temperature and peak temperature (see Fig. 3). Indeed, the effect of soak zone time and temperature was investigated in previous our study. Eventually, the void percent could be reduced to 7% by modifying soak temperature and soak time [7, 17]. The effect of peak temperature was investigated in this research to find the critical temperature for void nucleation based on the classical nucleation theory. The void nucleation

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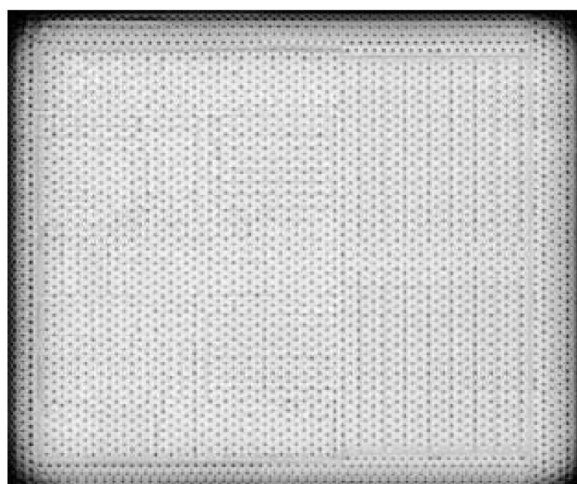
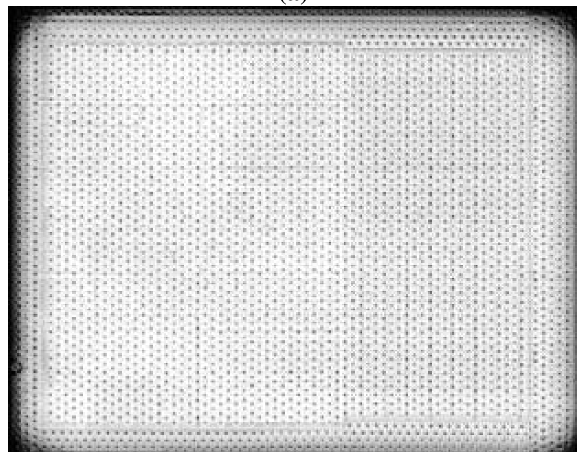
model predicted voids could form above 204 ºC, which is a critical nucleation temperature.

Therefore, experiments were designed to investigate the effect of reflow process parameters on voiding and to achieve the high, stable yield and void-free assembly process with FCIP using a commercial no-flow underfill. First, void formation study investigated the effect of peak temperature and reflow time on underfill voiding and Sn/Pb (63/37) solder wetting using a parametric study. Next, void formation characterization determined the best reflow process condition on the potential process condition found in void formation study using high IO, fine-pitch FCIP. Then, the stability of assembly process was validated using a large scale assembly.



(a)



(b)

Fig. 8 Micrographs of CSAM for void characterization study: (a) level 1 peak temperature (180 °C) and (b) level 2 peak temperature (190 °C)

Finally, these parametric studies determined the optimal conditions enabling a high, reliable yield and void-free assembly process. The assembly process used 200 ºC in peak temperature. The experimental result has an acceptable correlation with the model prediction, 204ºC. Therefore, the achievements in this study provide the design guideline for the high, reliable yield and void-free assembly process using no-flow underfill with high I/O, fine pitch flip chip. A nearly void free assembly process can be achieved using no-flow underfills in order to achieve long-term thermo-mechanical reliability.

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