A New Coreless Substrate Technology

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Abstract

Coreless substrate technology has been viewed as the holy grail of organic substrates for a long time. The benefit of this substrate concept is to reach the same level of wireability as in multi-layer ceramic substrates at lower cost and better electrical performance. Most approaches to date were based on materials like ABF or other resin systems with little reinforcement which resulted in substrates which were very prone to warping before die assembly and even more so after die attach. Here, the approach is to pattern plate the circuit pattern on a temporary carrier. In a second step, studs are plated for the future via interconnections. In a third step, prepreg is laminated over the prior structures. If a copper foil is included in the lamination step then the studs are accessed with etching openings in the copper foil and cleaning the top of the pillars to allow a plated connection in a pattern plating process. By repeating the appropriate steps of above on this substructure, a multi-layer coreless substrate can be built. The strength is equivalent to PBGA type substrates of equivalent thickness.

Introduction

The concept of coreless organic substrates is inspired by multi-layer ceramic substrate. The ceramic technology uses metal filled vias to interconnect adjacent layers of metallization. Because the vias are metal filled, the vias may also be stacked based on design requirements i.e. the vias may connect any number of the metal planes anywhere. Conventional organic substrates employ plated through holes (PTH) which must connect first to last plane plus any other selected inner layer. Buried vias (BV) which are essentially inner layer PTHs allow more selective interconnections at the expense of more complex processing [1]. Build-up (BU) technology essentially uses a core with PTHs and fine line redistribution layers on either side of the core. This also was an adaptation of multi-layer ceramic technology [2] where advanced ceramic substrates use redistribution layers mostly on one surface.

The first coreless organic substrate was actually a cell phone mother board from Matsushita called ALIVH (any layer inner via hole) which essentially emulated the process flow and materials of the ceramic technology. Thermount®[1] green sheets were laser drilled and filled with a metal paste to form building block A. Building block B was formed by laminating copper foil on both side of A and patterning the foils. Stacking of A and B blocks followed by lamination formed the raw mother board. Several years later, ALIVH was adapted for substrate applications but never successfully penetrated the market [3].

In the same time frame, Toshiba's B^{2}it substrate (buried bump interconnect technology) was introduced which used printed silver paste bumps to interconnect metal layers [4]. Eventually the technology was licensed to others but did not gain wide spread acceptance either.

Both technologies emerged during the early stages of BU technology development. With the advancement of laser via drilling and a new dielectric film from Ajinomoto, ABF (Ajinomoto Build-up Film), a de facto standard for BU substrates was established [5]. Further developments of coreless substrates either attempted to find variations of the Matsushita approach or to use ABF only as the dielectric for the coreless substrate. The Matsushita approach allowed for parallel processing i.e. the layer pairs were formed first and then laminated together in one step. When using ABF or similar dielectrics, the coreless substrate was built in a sequential fashion. In either case, the coreless substrates were extremely prone to warpage because the thick, reinforcing core

[1] Thermount® is a trademark of DuPont De Nemours Co.

was missing and the dielectrics did not contain any stiff, reinforcing fiber or fabric materials. Warpage presented a big problem during flip chip assembly as well as during board assembly.

The continued drive for miniaturization has lead to materials and process advancements like copper (Cu) via fill plating chemistries, ultra thin copper foils (UTC 1 to 3µ) and very thin prepregs of >= 35µ thickness. These components are now enabling a new type of coreless substrate based on glass fiber reinforced dielectrics which are much stiffer and more resistant to warpage than unreinforced materials.

Background for Development of Coreless Substrates

RF module substrates have already used fairly advanced designs and materials technology in the past few years. Essentially, these substrates often have used the concept of BU substrates except that the BU layer was based on either resin coated copper foil (RCC) or prepreg instead of the much more expensive ABF. This was facilitated by the fact that the circuit pattern was significantly more course and therefore achievable on a prepreg or RCC base. The copper foil pattern base is rather rough (R_z > 5 µ is not uncommon) which leads to a rather wide trace / space pattern in subtractive lithography. Initially the blind vias were conformally plated and had a significant dimple. As electro plating chemistries advanced, filled blind vias were introduced which supported bonding of components directly on the vias in pad, either wire bond or solder bond. A typical example is shown in Fig. 1.

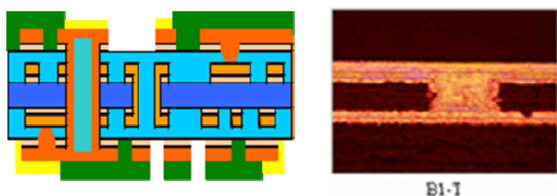

Fig. 1: Schematic of RF module substrate with Cu filled blind vias and example of Cu filled via.

The continued drive for miniaturization of RF modules demands further advancement of designs like stacked vias to facilitate high heat transfer from die to solder ball and higher routability / wireability as well as thin dielectrics to maximize electrical performance. These requirements can be best fulfilled with coreless substrates designs and, indeed, RF modules used to be built as multi-layer ceramic substrates except that the cost was extremely high. So after a detour through 'conventional' organic substrates, and now, that the organic substrates technology is ready, RF module substrates are the first applications to venture in to coreless organic substrates. Fig. 2 shows typical stack-ups / cross-sections for four and five layers designs. Ultimately, the layer count is limited only by manufacturing yields.

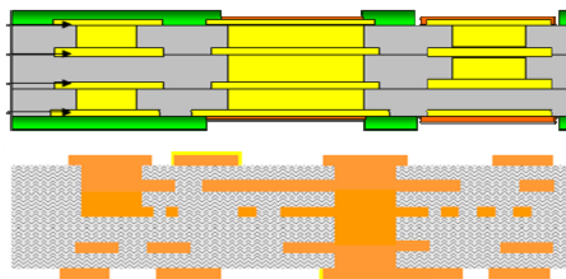

Fig. 2: Schematics of four and five layers coreless organic substrates respectively.

Single Sided Substrate

The manufacturing concept developed here is based on pattern plating and on using prepreg as the dielectric material. In a first step, a carrier with a metal layer suitable as a seed layer is prepared. Second, using modified semi additive plating (MSAP), Cu studs are plated in the locations of PTHs or BVs. Third, pre-drilled prepreg is placed over the Cu studs and laminated on to the base together with Cu foil. Fourth, the Cu studs are accessed by etching vias in the Cu foil and by subsequent cleaning of residual resin from the top of the studs. Chemical (permanganate hole clean) or plasma cleaning may be used to that effect. Next, the studs are connected to the foil via panel plating and subsequent pattern etching. This side of the substrate is finished by applying solder mask and plating and selectively plating Nickel/Gold (NiAu) as a wirebondable surface finish. Finally, the carrier is released from this substrate structure and the metal seed layer is etched off and the exposed Cu studs are protected with OSP (organic solderability preservative). Depending on the extent of etching, the studs are recessed accordingly. Actual cross-sections of such a single sided substrate, termed *a*S^3 ™ [2], are shown in Fig. 3 and the corresponding, schematic process flow in Fig. 4.

This *a*S^3 substrate is actually lower cost than the corresponding 2L substrate. The solder balls are recessed in the dielectric and there is no second layer of solder mask which results in a very low profile package. The benefits of *a*S^3 packages have been described elsewhere already [6].

Above process flow and resultant cross-

[2] *a*S^3™ is a trademark of ASE Group Inc.

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section is only one example. Some other versions have been described previously [6].

Fig. 3: Schematic of *a*S^3 (singled sided substrate) substrate based on coreless process flow.

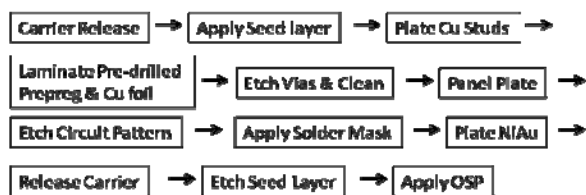

Fig. 4: Schematic of process flow for *a*S^3 type substrate.

Coreless Substrate

The *a*S^3 process concept has inspired a variation and extension of the process. Using the same seeded carrier, a first layer of circuit pattern is plated using MSAP. In a second lithography step, Cu studs are developed and plated in the locations to form the internal interconnects. Pre-drilled prepreg is placed over the studs and laminated to the circuit pattern. The stud surfaces may be planarized which exposes clean stud tops at the same time (Fig. 5). If necessary, the pillar tops may be cleaned wet-chemically or by plasma. This process may simultaneously be used to modify the dielectric surface as well to enhance adhesion to the next seed layer of Cu. The surface is seeded with electroless Cu and subsequently patterned. Now the carrier is released and both sides of this subunit are plated with Cu studs. The seed layers are removed by quick etching and pre-drilled prepreg is laminated over the studs together with UTC foil. The studs are accessed by etching vias and cleaning of any residual resin. Using MSAP, the external patterns are plated for a 4L coreless substrate. The substrate is finished by flash etching the UTC foil, applying solder mask and plating ENEPIG (electroless Ni electroless Palladium immersion Au) as a surface finish. A schematic process flow is shown in Fig. 6.

It should be noted here as well that several process variations can be employed to achieve the same type of substrate cross-section. Process choices are dictated by infrastructure and chemistries available in the manufacturing line.

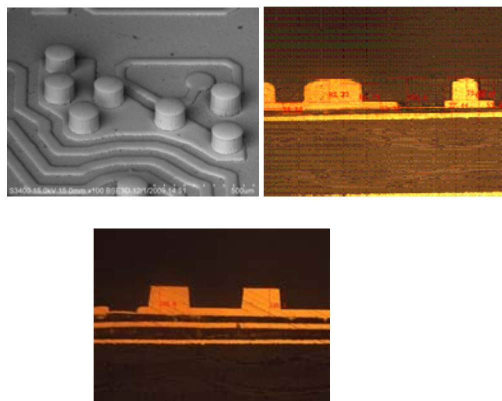

Fig. 5: Cu studs after stripping resist without planarizing (top) and after planarizing (bottom).

Depending on process uniformity and control, it may be necessary to planarize the Cu studs after plating, before stripping the photo resist. Likewise, additional planarization may be performed after lamination. Instead of seeding the dielectric with electroless Cu, sputtering may be used as well. When using sputter technology, it may be advantageous to use titanium coating first to enhance the adhesion of Cu.

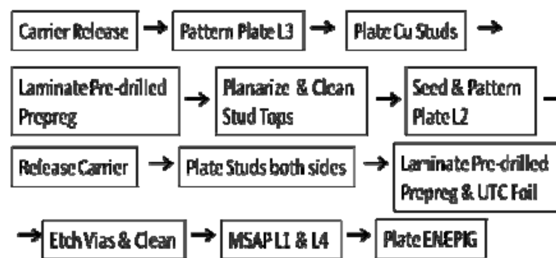

Fig. 6: partial cross-section of 4 layer coreless organic substrate.

In Fig. 7, a cross-section of an intermediate plating step is shown. Here all interconnecting studs for a four layer structure have been plated. The next step is to laminate the prepreg and UTC over the studs.

The process sequence for stacking the layers needs to be modified slightly to build odd number of layer coreless substrates. An example of a 5L coreless substrate is given in Figs. 8 and 9.

It should be noted that all process steps which use a carrier can be done in a doubled sided fashion to double the throughput and thereby significantly reducing the cost of these substrates.

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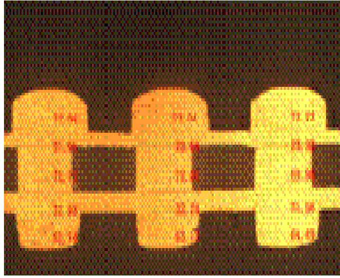

Fig. 7: Plated Cu studs for four layer coreless substrate.

It should be obvious from above, that embedded component substrates are easily manufactured with this process concept as well. To that end, dice are bonded to the appropriate layer using an epoxy type adhesive. The prepreg for the next layer has an opening for the dice. The die pads are accessed by laser drilled vias and subsequent plating. The die pad metal finish should be Cu platable i.e. the metal finish must be thick enough to withstand laser drilling and chemical cleaning. More details will be described in a future publication. A roadmap for the embedded die (or component) is shown in Fig. 10.

Since substrate yields are typically in the 90% range, there would be substantial loss of known good die (KGD) when embedding die. Therefore, the process concept has been adapted to a known good substrate (KGS) approach (Fig 11). Here, first a testable substrate block is built first. Dice are then placed into the KGS and the substrate is then finished with top layer (s) with fewer opportunities of defects. This approach will increase the yield of the embedded component substrate.

Currently, product characterization is in progress and will be reported in the future as well.

Fig. 8: Partial cross-section of 5 layer coreless organic substrate.

Conclusions

A new methodology for building organic, coreless substrates has been devised. Any number of layer substrates can be manufactured with the only limit being the yield. At this stage substrates from one to five layers have been built. Single layer substrates are ramping up in volume whereas four and five layer substrates are being sampled to customers. The dielectric material is glass reinforced prepreg which imparts mechanical strength to the substrate to minimize warpage. The interconnects are full copper being plated with MSAP technology. The technology can be extended to the manufacturing of embedded component substrates.

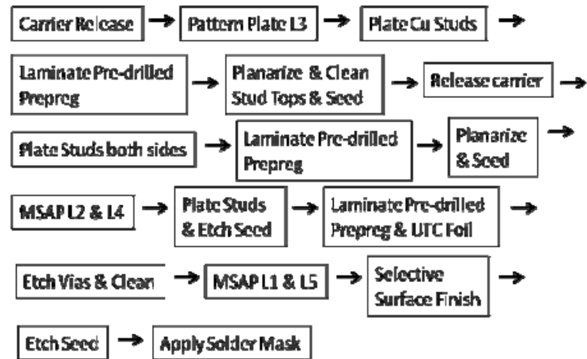

Fig. 9: Schematic process flow for a 5 layer coreless organic substrate.

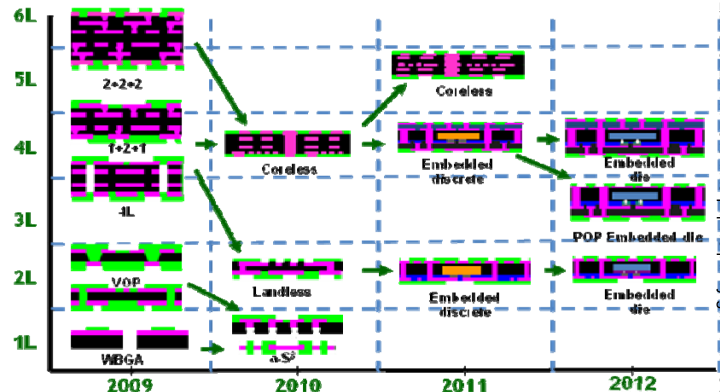

Fig. 10: Coreless substrate roadmap based on aS3 technology which has been extended to included embedded components.

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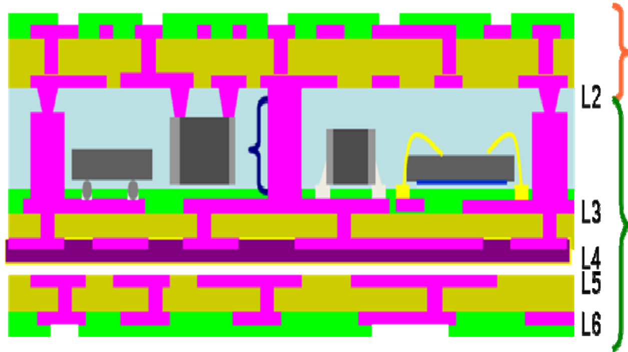

Fig. 11: This schematic of an embedded component substrate uses a known good substrate consisting of layers L3 – L6 including the Cu posts extending to L2. L2 and L1 are of substrate two which has been joined to the other substrate after attaching the components.

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