# High Aspect Ratio Package Core Production with Electrolytic Deposited Copper

**Stephen Kenny and Bernd Roelfs**
**Atotech Germany**
**Erasmusstrasse 20**
**Berlin, 10553 Germany,**
**+49 30 34985 921and 965**
**Fax +49 30 34985 618**
**Stephen.Kenny@atotech.com**
**Bernd.Roelfs@atotech.com**

## *Abstract*

*A typical package core consists of copper clad dielectric which is drilled to produce the necessary through vias serving two functions either as electrical or as thermal conduits. The thermal vias are normally characterised by a low drill pitch and a localisation at the centre of the package core. The vias are plugged after metallisation with a resin material to give the core the required planar surface necessary to provide the basis for the subsequent build up layers. Use of electrolytic deposited copper has been introduced as a new method to fill such through vias, pure copper as a plugging material has obvious advantages due its higher thermal conductivity in comparison to any currently available plugging resins. Significant cost savings are also possible as a fully automated in line processing sequence is available for electrolytic copper deposition in comparison to the more labour intensive resin plugging methods. The package cores utilising this technology have however been restricted to a dielectric thickness in the range 60µm to 100µm and with through via diameter 75µm to 100µm due to limitations in the processing technology. With these dimensions a hole pitch of down to 250µm may be filled reliably and is currently in production, latest results from this technology are shown. Hole filling with higher aspect ratios and particularly with substrates thicker than 200µm has required improvements in processing to ensure uniform copper filling. This paper describes the optimised process for through hole filling and shows the results achieved with dielectric materials 200µm and up to 400µm thick. Current qualification results of substrate 400µm thick with through via 80µm diameter are shown together with the comparison of filling with via pitch variation between 1.0mm and 0.6mm*

Key words: Core via filling, Production cost reduction

### Introduction

The manufacturing process for substrate cores requires production of a planar surface which is subsequently used as the starting point for the high-density build-up layers. The core is normally mechanically drilled to produce the required through-via connections which are then metalized and plugged with a thermally cured resin material. There is a current tendency for reduced core thickness and this has implications for yield, quality and ultimately for cost for product from the complete process. The plugging process itself is relatively labor-intensive and requires, as part of the sequence, a mechanical abrading or brushing process after resin cure, which can cause problems of dimensional stability, particularly for substrate cores less than 100µm thick. The plugging resin itself has disadvantages in that it is a high-solid content material, which has a different coefficient of thermal expansion (CTE) to that of the surrounding material, including the copper metal in the via and also to that of the dielectric of the core itself, typically a glass-reinforced resin material.

The disadvantages of the existing plugging process can be eliminated by using pure copper to produce the planar surface. For the next-generation process, copper is deposited into the through vias as an integral part of the metallization process. The drilled dielectric is made conductive and a thin layer of copper metal is deposited to give a seed layer for the copper deposition process. The through-vias are then completely filled by a modified electrolytic copper deposition process, which is accomplished in a single, fully automatic continuous processing line.

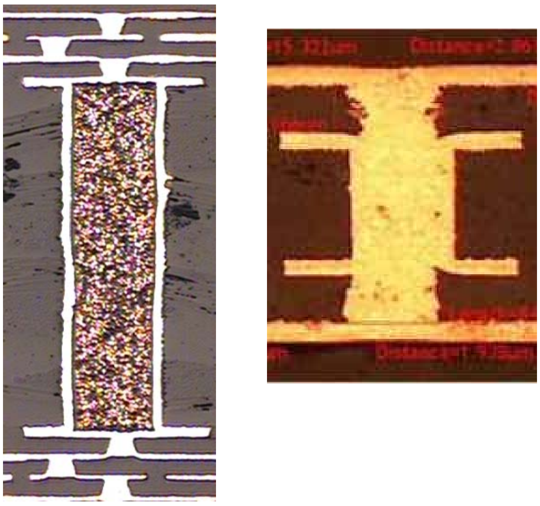

Fig. 1: X-sections showing a paste plugged through via in a core (left) and an electrolytically Cu filled through via (right), both with sequential build up blind micro via (BMV) layers.

The use of pure copper has obvious advantages in that its thermal characteristics are significantly better than any type of resin material available. This fact can give more design options to utilize the improved thermal transfer capability of vias in a substrate than are currently available. The CTE of the copper-filled core is dependant only on the copper metal and the glass-supported resin of the drilled dielectric. The copper structures in the subsequent layers may be positioned directly above the copper-filled through-vias with no reliability implications. In fact, the conductive path within the substrate may be designed to utilize the more direct and parallel connection from one side of the substrate to the other.

Table 1: Process flow comparison of paste plugging and electrolytic copper through hole filling.

| | Paste Plugging | Cu Filling |
|---|---|---|
| 1 | Hole drill | Hole drill |
| 2 | Metallisation | Metallisation |
| 3 | Cu plate 18µm to 25µm | Cu plate 3µm |
| 4 | Resin plug | Cu through hole fill 12µm to 20µm |
| 5 | Cure | Image and etch |
| 6 | Surface grind | |
| 7 | Resin metallization | |
| 8 | Cu plate 18µm to 25µm | |
| 9 | Image and etch | |

Via hole plugging as a process is used to produce a planar surface which enables subsequent sequential lamination for production of build up structures, a planar surface is particularly important to ensure uniform dielectric spacing between circuit layers critical for controlled impedance in high frequency applications.

The standard process is to use a plugging paste which is applied by methods such as stencil printing or roller coating. On top of the plugging paste there will either be the next resin layer which may be glass reinforced, or a plated copper layer. This copper surface may be used to allow production of staggered or stacked blind micro vias which are conformally copper plated or copper filled depending on the application requirements. An example for a substrate with a paste plugged core is given in figure 1 as well as an example with a copper filled core. Both examples show also filled BMVs positioned directly on top of the through hole allowing via in pad technology. This example illustrates well the technique of blind micro via filling to ensure void free sequential lamination. The direct positioning of the BMV on the core through hole will save space in the substrate design. The electrolytic copper filling process sequence in comparison to the paste plugging is shown in table 1, the reduction in processing steps illustrated gives significant potential to reduce production costs and also to increase production yields.

## Development of BMV filling process for through hole filling

The need for finer lines and higher reliability has driven the development for filled BMVs. The main drivers of the BMV filling technology have been IC substrate manufacturers with demand to reduce feature size to free up space on a substrate. One of the key methods for this has been to apply stacked via technology which is based on perfectly filled BMV´s of small dimensions (60µm x 40 µm). HDI manufacturers have followed this approach and tried to use the filling technology for their application. Unfortunately, HDI manufacturing requires filling of much larger BMVs (e.g. 125µm x 75 µm) at a significantly higher production throughput. Where IC substrates are produced at about 1-1,5 ASD, HDI boards are often produced with 5-10 ASD. This requires a significantly different production scenario. The key for success at such high current densities is a perfect distribution of copper, since the BMV filling is much more sensitive to copper thickness variations than normal conformal plating applications. Not only the distribution within the panel but also the panel to panel and batch to batch distribution needs to be optimized. For this very specific application use of completely horizontal conveyorized production equipment comprising of a desmear process, initial metallization of the surface and hole by electroless copper and an electrolytic copper plating step. A conveyorized approach is extremely beneficial as the panel to panel variation in such a system is minimized. For perfect distribution within a panel both the electroless and the electrolytic copper deposition was optimized.

The first step was to improve the distribution the e'less deposition of copper. It was necessary to improve the amount of copper in a BMV since drilling through a glass fibre reinforced material often results in a non regular BMV shape. Figure 2 depicts such a non optimal BMV shape which has been processed in a specially developed electroless copper metallization process to give optimal coverage and adhesion to dielectric and glass fibers.

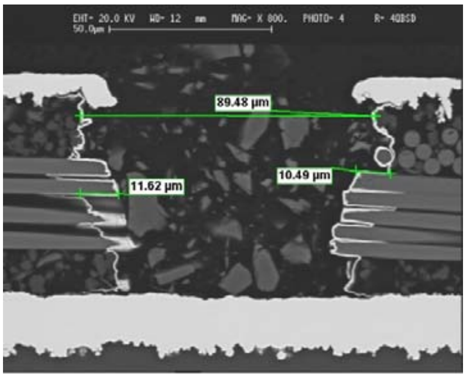

Fig.2: BMV after exposure to the latest technology electroless copper metallization process.

The biggest advancement in the subsequent electrolytic copper deposition has been the development of the so called Superfilling process for BMV copper filling. The system is based on a combination of inert anodes together with reverse pulse plating in horizontal production equipment. The process is in fact a combination of simultaneous electrolytic copper plating and copper etching in one electrolyte. This is realised by using an electrolyte which contains copper and iron which forms an equilibrium between $Fe^{2+}$ and $Fe^{3+}$ with relative concentrations dependant on the particular working conditions.

Originally, the iron redox system was introduced as a replenishment aid [1] for copper ions and as reaction partner for the inert anodes instead of additives and water. Use of the redox system significantly reduces the consumption of the additives by preventing oxygen evolution through any degradation of water. Moreover, it showed the added benefit of an increase in the life time of the expensive Iridium oxide coverage for such anodes since anodes are operating at the lower oxidative potential of the Fe redox couple. Through practical experiments it was found that the $Fe^{3+}$ can be further used to minimize the amount of surface copper which is the basic idea behind the technique to achieve copper through hole filling.

The principle of this Superfilling process is shown in fig.3.

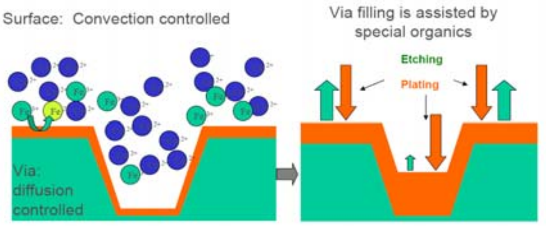

Fig.3: Schematic showing principle of simultaneous plating and etching with preferred surface etching

This illustrates well the difference between a surface and the base of a recessed structure during copper plating. Transport of ions and additives is for the surface mainly convection controlled due to the extremely high flow rate whereas a BMV behaves completely differently. The transport is diffusion controlled and as such is orders of magnitude slower. This leads to a concentration difference of $Fe^{3+}$ ions between surface and BMV bottom. By running this system with extremely high $Fe^{3+}$ concentrations in the range 4g/l to 6 g/l it is possible to reduce the amount of surface copper by up to 50 % compared to a conventional non redox system whilst maintaining the targeted copper deposition into the BMV.

**Mechanism for through hole filling**

In the development work for the blind micro via filling process it was seen in early experiments that through vias were excessively plated at the centre of the hole. This result is normal when reverse pulse plating is used however the extent of the plating thickness in the hole centre was a surprise, as can be seen in first image in figure 4.

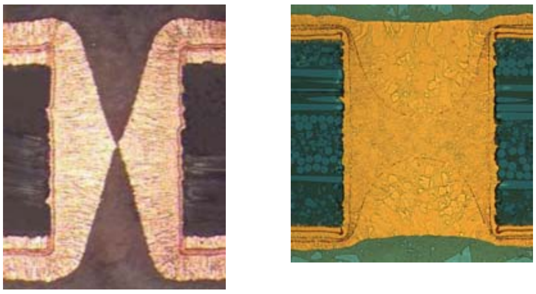

Fig 4: Two step process for through hole filling. 1st : X plating with extreme reverse pulse and 2nd BMV filling

The application of the reversed pulse now interferes with the distribution of these additives in a hole and on the surface. The reverse pulse is able to modify the concentration equilibrium in a hole and on the surface in such a way that the accelerating catalyst concentrates in the middle of a hole and is depleted from the surface. This is due to the fact that under reverse (=anodic) pulse conditions the catalyst is desorbing together with a small amount of copper. Since the concentration of the brightener is relatively small it takes a while to re-adsorb again and this catalyst is now partly missing for the subsequent cathodic pulse. The hole is compared to the surface electrically shielded so that the reverse pulse does not reach its maximum strength especially in the middle of the hole. Here, the desorption of the catalyst is incomplete and it can react immediately after switching the pulse to cathodic values. As a consequence the deposition speed in the middle of the hole is increasing compared to the surface and complete copper through hole filling can be achieved

**Through hole filling development and optimisation**

In the early stages of the process development a considerable amount of surface copper was necessary to fill through vias. In fact, more than 50µm panel plated copper was necessary to fill a 100µm thin panel with 100µm diameter holes as shown in Figure 5. Together with base copper foil of 17 µm it was not possible to apply this technology for any practical applications due to the etch limitations of such a thick copper layer. Trace dimensions in the region of sub 75 µm and for IC substrates less than 50 µm are required and to reach this technology level the plated copper had to be reduced. To enter the 50 µm lines and space arena it was necessary to reduce the amount of plated copper significantly down to about 20 µm and work with thinner laminated copper (e.g. 3 µm copper).

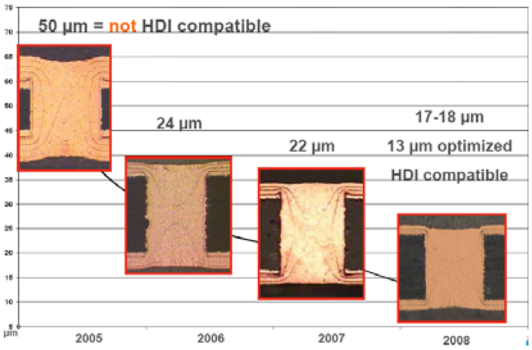

Fig.5: Development of the amount of necessary surface copper to fill a 100 µm hole in a 100 µm thin panel for TH filling capability

Constant process improvement as shown has reduced the required plated copper thickness so that currently in the range of 15µm to 18µm copper can effectively fill a substrate with 100µm thickness and with 120µm diameter drill via. In figure 6 optical microscope and also SEM image to show copper plated structure is shown from the core of a substrate with thickness 120µm.

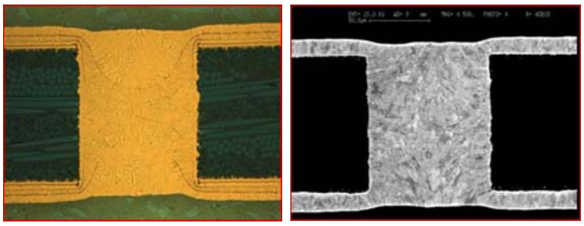

Fig.6**:** Optical microscope together with SEM of copper filled through hole in substrate.

Not only decreased copper thickness but also the copper crystal structure and physical properties of the deposit have to meet industry standards norms. The SEM image in figure 6 shows the copper deposit of the deposit achieved in production for such substrates. Both the etched and the SEM micrograph show the normal polygonal copper structure which is well documented from numerous investigations. A variety of quality measurements on ductility, tensile strength and differential scanning calorimetry (DSC) show that this deposit is comparable to the normal plated copper quality and withstands the usual industry requirements.

**Process Advantages for copper through hole filling**

Numerous advantages of copper filled through holes can be described, not least should be an expected increase in reliability. Reliability issues in accelerated aging test occur usually when the CTE of adjacent materials are very different. This is in fact the case for every circuit substrate. The CTE of copper is approx. 17 ppm/K and the CTE of typical FR4 base material is approx. 110 ppm/K. The CTE of plugging pastes for standard through hole filling processes is at 30-40 ppm/K in between that of the other materials. This means that a copper barrel in a through hole comes under stress from both outside and inside the barrel. This often results in corner and barrel cracks

Such a stress for a completely copper filled through hole can only be induced from outside but also a thicker copper barrel is a mechanically strengthened system due to the superior mechanical properties of the copper layer

Another benefit of copper filled through holes is the possible application for thermal vias. Copper has obvious advantages for thermal vias due to its high thermal conductivity, this is at 360W/mK much higher than that of any plugging material, and this has been described in [2]. Normal plugging materials have thermal conductivity values of about 1W/mK, specially developed high thermal conductivity paste at up to 8 W/m K. Compared to these pastes the thermal conductivity of copper is about 40-50 times better. Simple calculations show that more than 90-99% of the heat transfer is still carried by the copper barrel irrespective of which paste is used for plugging. This effectively reduces the application of such paste plugged thermal vias.

Also due to the increased thermal and electrical characteristics of a solid copper core the number of thermal vias required may be reduced whilst maintaining an equivalent thermal capability. This again may free up surface which can be made available for interconnections so allowing further miniaturization. Build up layers may be positioned directly above the filled core with no loss in reliability and this design gives the shortest and most direct circuit path from one side of a substrate to the other.

## Through hole filling with high aspect ratio substrates

The higher the substrate aspect ratio then the more demanding becomes the filling process. This can be understood simply by considering the increase in the volume of copper which has to be deposited and at the same time the requirements for HDI imaging have to be met which means keeping the surface plated copper to a minimum. After copper plating the surface thickness may be reduced with a chemical etching or even a mechanical brushing however these processes are relatively labour intensive and cause an increase in the process costs as well as increased consumption of raw materials.
For higher aspect ratio processing efficient electrolyte transfer into the through holes is critical, copper ions have to be made available to the plated surface even with a constantly changing, more demanding aspect ratio In figure 7 results are shown with 250µm and 300µm thick substrate with approx. 100µm diameter through holes. The result shows good filling and with approx 10µm surface plated copper this result is acceptable for HDI applications.

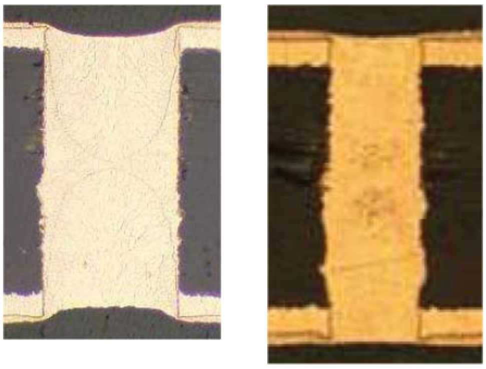

Fig.7**:** Through hole filled cores 250µm and 300µm thick.

The current development target is however to achieve copper filling in a core 400µm thick and with through holes diameter with 80µm and also 100µm. In particular investigations have been made on the impact of drill hole pitch on the copper filling process. With reduced drill pitch the effective hole density increases and the target volume of copper increases so making the filling process more difficult. An added complication is that typically drill pitch at 1mm and also 0.3mm may be present on the same substrate and a uniform processing result is required over the whole surface. In figure 8, results are shown from filling of a 400µm thick core with 80µm diameter through vias at drill pitch 0.3mm. In the following figure 9 the result with drill pitch 1mm taken from the same substrate is shown.

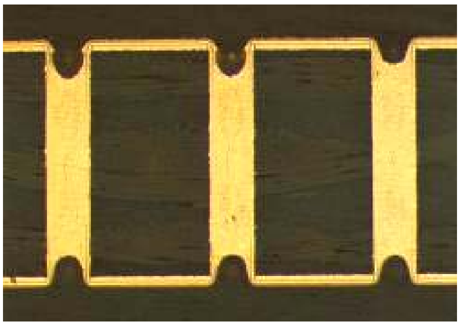

Figure 8: Through hole filled core 400µm thick with 80µm diameter vias at drill pitch 0.3mm

Figure 9: Through hole filled core 400µm thick with 80µm diameter vias at drill pitch 1mm

The result shows uniform filing result despite the drill pitch variation however the remaining dimple on the surface is relatively large.

## Summary

The current through hole filling process using horizontal copper panel plating technology is capable to fill through holes for HDI production with diameter 75µm to 100µm and with substrate thickness 100µm and up to 120µm. The technology is now qualified and in production for thin cores ranging from 50µm up to at the moment 150µm thick and with 500 thousand holes on one board at a major producer in Taiwan.

For this application a maximum surface copper thickness of 12µm including base copper foil is possible. Depending on the hole diameter, drill pitch and the required plated copper thickness filling of through holes in substrates 200µm and up to 300µm is currently in qualification. For substrates over 300µm the current plating thickness and processing time is too high for acceptable production requirements however development is ongoing with target to reduce both these factors and to ensure inclusion free copper filled structures.

## References

[1] Jürgen Barthelmes, "Acid copper plating with insoluble anodes a novel technology in PCB production" (ECWC), September 1999.

[2] Christoph Lehnberger, "Strategien zur Elektronik-Kühlung", (Leiterplatten-Design), October 2004, pp 24