AuSi and AuSn Eutectic Die Attach Case Studies from Small (12 mil) to Large (453 mil) Die

Daniel D. Evans, Jr. and Zeger Bok
Palomar Technologies, Inc.
2728 Loker Avenue West
Carlsbad, CA 92010
Phone: (800) 854-3467 E-mail: info@bonders.com

Abstract

High power transistor, laser, and LED devices require packaging to remove thermal energy from the die. Although some silver filled epoxies provide thermal conductivity approaching 60 W/mK, AuSi and AuSn solder have long proven superior thermal performance. Materials such as Si and GaAs on CuW and GaN on SiC will be discussed in three case studies for die sizes ranging from 12 x 21 x 4 mil thick to 453 x 274 x 12 mil thick, using AuSi or AuSn eutectic die attach processes. The cases provide an overview of material selection and methods for optimized utilization of eutectic solders. Bond quality metrics such as fillet, voiding, and shear will also be covered in this paper.

Key words: AuSi Eutectic Die Attach, AuSn Eutectic Die Attach, RF Package

Background

Motivation for this work is to provide an overview of eutectic die attach methods to help design and process engineers select equipment and processes for die and substrates that require high thermal dissipation and/or fluxless processes.

The challenge for designers is to make products more efficient but as devices become smaller the challenge continues to be maintaining die junction temperatures as power density increases. RF Power amplifiers approach 1,000 W/cm^2 while IGBT devices are approximately 100 W/cm^2 as shown in Figure 1.

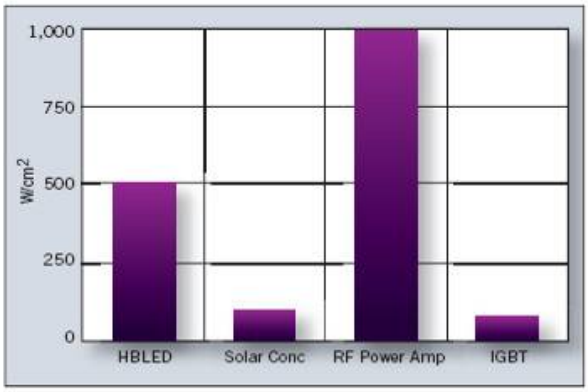


Figure 1 – Power Density of various High Power Semiconductor Devices. [1]

The die sizes vary from product to product as well as the required packages to transfer and dissipate the die heat. Figure 2 shows examples of high power density packages.

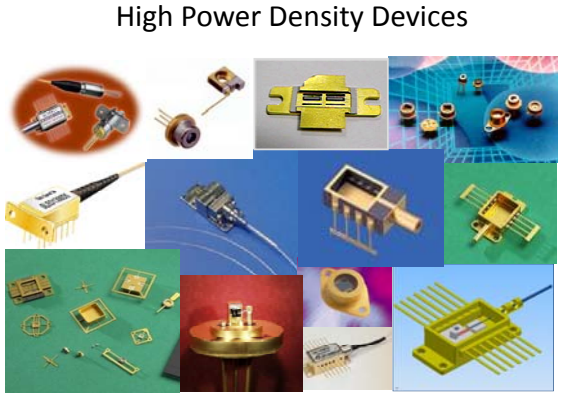


Figure 2 – High Power Density Devices in different shapes and sizes

The fundamental problem remains the same as design and packaging engineers work together to move heat from the die to the environment as shown in Figure 3. Each device in a stack has a thermal resistance. For example, Θ_{DA} is the thermal resistance from the top of the die to the bottom of the die at the attach interface. This paper will focus on the thermal resistance of the interconnect

material, Θ_{AS}. From the equation in Figure 3, it can be seen that thermal power transfer in the vertical direction is optimized by maximizing the thermal conductivity (k) and interface area (A), and by minimizing the interface thickness (x) with the objective of minimizing the temperature gradient (ΔT). The entire assembly stack should be modeled mathematically in 3 dimensions, to help design engineers select suitable materials, geometries, and processes for each step in the assembly process.

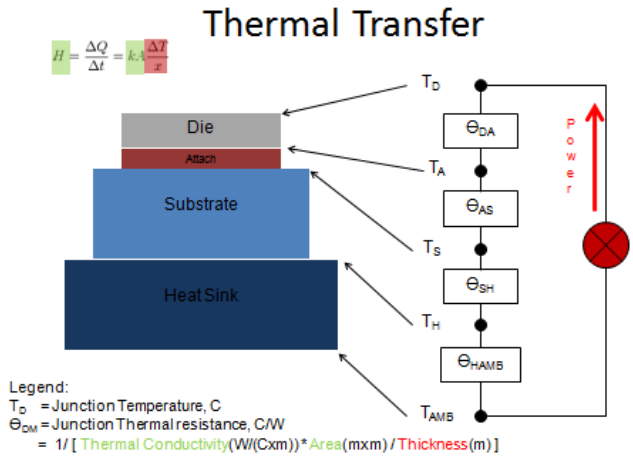


Figure 3 – Thermal Transfer Stack with Interconnect Material between Die and Substrate

The material selection for substrates and die can have an enormous impact on the thermal performance of the assembly, as shown in Table 1. The design and packaging engineer must consider thermal expansion, thermal conductivity, plus other mechanical properties of the interface that affect product performance and reliability. Both GaN and AlN have exceptional thermal conductivity of 130 and 140-180 W/(m*K), respectively and also have a relatively low Thermal Coefficient of Expansion (TCE) approaching that of Si. Pure metals have better thermal conductivity but a significantly higher TCE than GaN and AlN.

Table 1 – Thermal Properties (published sources)

Material	Thermal Expansion ppm/K	Thermal Conductivity W/(m*K)
Cu	17	401
Cu(45)W(55)	11.8	2.4
GaN	3.2-5.6	130
Al2O3	5.8-8.3	35-40
AlN	4.4	140-180
Al	23.5	237
Au	14	318
Ag	19.1	429
Si	2.6	190
Sn	22	66.8
Au(96.8)Si(3.2)	10-12.9	190-285
Au(80)Sn(20)	16	59
Ag(3.5)Sn(96.5)	30.2	33
Silver Filled Epoxy(generic)	40-50	2.5-3.6

Gold-Silicon Au(96.8)Si(3.2) has a thermal conductivity between 190-285 W/(m*K) with a TCE of 10-12.9 ppm/K and melts at a eutectic temperature of 363C. Gold-Tin, Au(80)Sn(20) is another common eutectic solder with thermal conductivity of 59 W/(m*K) and TCE of 16 ppm/K and melts at a eutectic temperature of 280C.

Eutectic Attach Overview

There are two main options for creating a eutectic attachment, as show in Table 2.

In-Situ Reflow forms the interconnect by heating the interface to eutectic temperature while holding the die in place, one die at a time. The placement accuracy is dependent on the precision of the selected equipment. There are several methods to generate the required heat (temperature required for reflow as shown in Table 2).

Mass Reflow forms the interconnect after placing all die and then transporting the entire assembly or a batch of parts to a reflow oven to reflow all die at the same time during the same cycle. The final placement accuracy is dependent on surface tension and/or fixturing.

Table 2 – In-Situ versus Mass Reflow

Method	In-Situ Reflow	Mass Reflow
Technique	Conductive heating of substrate and/or die (Steady or Pulsed)	Dry pick and place
	Conductive tool heating (Steady or Pulsed)	X-fer to reflow oven
	Convective heating (hot gas)	Reflow en masse
	Laser heating (spot size)	
Comments	Only one component held during reflow. Some see multiple or longer temp cycles	No component held during reflow. All see one temp cycle.

Conductive in-situ heating of the assembly may be implemented using "steady state" (constant temperature) or "pulsed heat" temperature profiles, as shown in Figure 4. Compared to a rather slow batch reflow oven process, the latter is used to heat the die or substrate quickly, hold temperature steady, then cool down quickly. A pulsed heat stage can also be used for batch reflow if the devices are small enough to fit in the stage envelope. The profiles are typically programmable and can reach multiple temperature levels and durations.

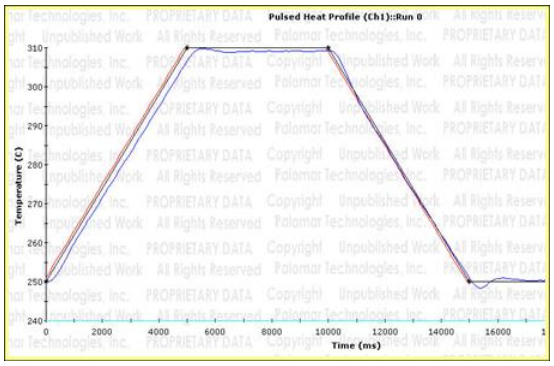
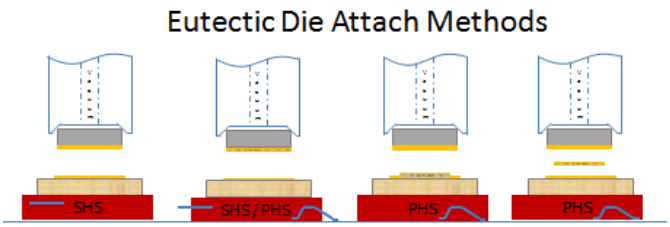


Figure 4 – Generic example of a Pulsed Heat Temperature Profile

The packaging engineer must select a pick tool type (surface, 2-sided inverted pyramid, or 4-sided inverted pyramid), a temperature profile (steady state or pulsed), a scrub pattern if required, and suitable substrate and die plating, as shown in Figure 4.



AuSi	AuSn on Die	AuSn on Substrate	AuSn Preform
Die w/2-3um Au	Die w/2-3um AuSn	Die w/2-3um Au	Die w/2-3um Au
Substrate w/Au	Substrate w/Au	Substrate w/AuSn	Substrate w/Au
Steady Heater Stage	Steady Heater Stage or Pulsed Heat Stage	Pulsed Heat Stage	Pulsed Heat Stage
Scrub X or Y or both	Scrub X or Y or both or none for small die	Scrub X or Y or both or none for small die	Scrub X or Y or both or none for small die
2Side or 4Side Tool	2Side, 4Side, or Flat tool if no scrub	2Side, 4Side, or Flat tool if no scrub	2Side, 4Side, or Flat tool if no scrub
1 PNP	1 PNP	1 PNP	2 PNP

Figure 4 – Eutectic Die Attach Methods

The four columns in Figure 4 summarize each eutectic die attach method. The first column is for AuSi attach while the last three columns are for AuSn, based on the location of AuSn in the process flow. The AuSn may be plated on the die, plated on the substrate, or presented as a separate solder preform that requires a separate pick and place operation thus reducing throughput, unless the preform is already attached (tacked) to the die or substrate as part of an upstream process.

Row three in Figure 4 shows the anticipated heating method from the perspective of in-situ reflow. For example, AuSi can use a steady state temperature for the substrate and then bring each die in contact with the substrate while applying scrub during reflow. The same technique could be used for AuSn, as long as the die is plated with the AuSn, otherwise reflow may occur before the die is even placed onto the AuSn solder.

The application shown in Figure 5 is a AuSi attach where the substrate is held above the eutectic temperature while all four die are placed and scrubbed sequentially. Since this is a serial operation, each die will see a different duration at temperature as the first die will be on the substrate longest. This will cause some variation in eutectic outflow (wetting) from die to die, which can be managed by reducing cycle time. For example, the ability to change pick tools on the fly clearly has an advantage over time consuming pick tool docking stations. The example shows a four-sided inverted pyramid pick tool for scrubbing in two directions and a two-sided pick tool for scrubbing in one direction only. Note that the eutectic process should be performed in a low oxygen environment to minimize oxidation and voiding.

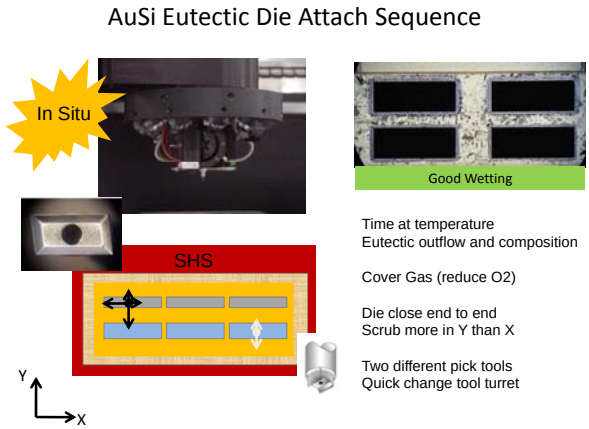


Figure 5 – AuSi Eutectic Die Attach Sequence

Eutectic Die Attach Case Studies

Three specific cases are described below to highlight the primary challenges and solutions in eutectic die attach assemblies for some of the following packages: AuSi (RFSOE) 16x63x4mil & 31x64x4mil, AuSn (P-Side Down) 12x10x12mil

with preform using pulsed heat top down, and AuSn (ASIC) 453x274x12mil with preform using pulsed heat bottom up.

Case 1: AuSi (RFSOE) 16x63x4mil & 31x64x4mil

The specific case in Figure 6 is a power transistor in RFSOE format. It contains two different die sizes with AuSi attachment. The mockup shows three die per die size and the photograph shows two die per die size. The eutectic process in this example uses a two-sided inverted pyramid pick tool to place both die with Au backside plating onto an RFSOE header with Au plating. The header is at a constant temperature during the eutectic attachment of the die. Each die is picked and then placed and scrubbed in one direction under a selected force to achieve the required solder coverage for fillet and voiding underneath the die.

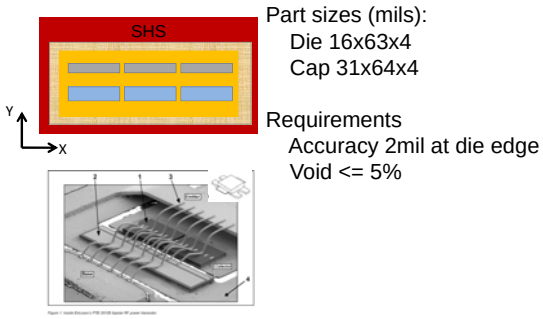


Figure 6 – RFSOE Power Transistor example showing two Die sizes.

The required placement accuracy of ±2mil is relatively easy to achieve with today's available die attach equipment. The eutectic solder coverage after destructive shear test for this case study is shown in figure 7. Both die were bonded in the same package but the die on the right was above eutectic temperature for multiple minutes and illustrates the time at temperature dependency of eutectic attachment. The die shows a much wider wetting area (light gray zone) of the original solder fillet during bonding. Formation of the eutectic AuSi composition will continue if the die is held above eutectic temperature until the Au or Si is fully consumed. It is important to avoid excessive wetting as studies have shown that small voids, initially formed during eutectic attachment due to imperfections, contamination or gas entrapment, tend to grow with time at temperature.

The die on the left shows a more typical destructive shear test example with proper fillet and solder coverage underneath the die, shown as a flat gray zone along the perimeter of the die. This gray zone is a result of the scrub motion and eutectic solder outflow during reflow.

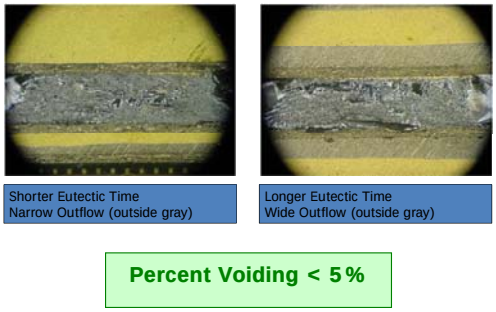


Figure 7 – Destructive Shear test results of two Die with AuSi Eutectic Attachment and comparison of shorter vs. longer Eutectic Time.

Equipment requirements depend almost entirely on production volume needs:

Semi-Automatic - Figure 8 shows an example of a semi-automatic system with batch loading of die in GelPak™ and headers in matrix trays. The machine will automatically pick a header from the input tray and place it on a heater stage that is set at reflow temperature and encases the header in a cover gas environment. Each of the die are then picked from the GelPak™ and placed into the package using scrub and force. Once the package is completed, it is moved to an output tray. The build sequence is continued until all headers in the tray are completed.

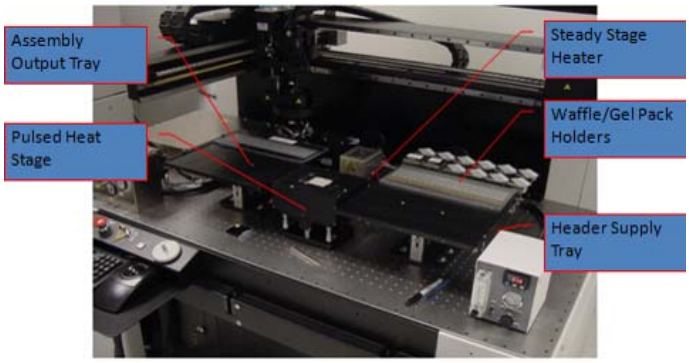


Figure 8 –Automatic Tray Load/Unload RFSOE Eutectic Assembly Cell with Pulsed and Steady State Heater Stages

Automatic - Figure 9 shows an example of a fully automatic system with SMEMA compatible [3] magazine loading and unloading of headers. The 4 different die are loaded in wafer frame or grip ring. Other configurations of wafer handler systems allow 6 different types of wafers in a single build

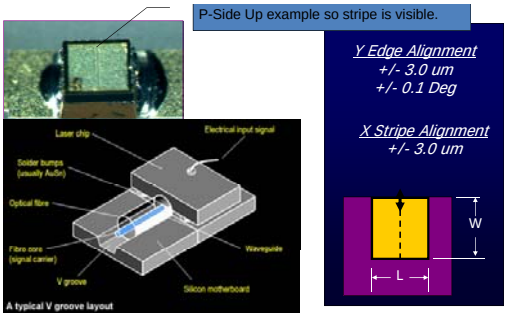
operation. The magazine to magazine handler will automatically present a header into a heater stage bond station, often equipped with pre-heat stages to reduce temperature ramp-up time. This allows higher throughput than the semi-automatic system since the handler positions the header rather than the pick-and-place head. The handler provides the reflow temperature and encases the header in a cover gas environment. Each of the die are then picked from the wafer frame and placed into the package using scrub and force. Once the package is completed, the magazine to magazine handler will move it along towards the output magazine. The build sequence is continued indefinitely until no more headers are loaded in the loading magazine. The handler automatically heats and cools the headers during production.

Figure 9 – Automatic Magazine to Magazine Header Load/Unload and 4 Wafer Frame/Grip Ring RFSOE Eutectic Assembly Cell

Case 2: AuSn (P-Side Down) 12x10x12mil with Preform using Pulsed Heat Top Down

The physical samples in this case include a 6" wafer that contains a matrix of substrate devices upon which a laser die is solder attached. The wafer has fiducials for each individual substrate device with alignment targets and gold pads that are pre-metalized with AuSn eutectic solder. The laser die is 300µm long by 250µm wide by 125µm thick with backside (P-Side) gold plated pads for solder attach.

This specific details of the components used for this case are proprietary but a generic case is shown in Figure 10. The example shows the alignment criteria and one possible implementation for Si wafer scale packaging. The actual image of the laser die is shown P-Side up so the details of the P-Side are visible. The P-Side is referenced with a lookup camera followed by an alignment algorithm during the pick and place cycle. [2]



Die Size 12mil x 10mil x 125um thick, Au plating on die, AuSn plating on Substrate

Figure 10 – Wafer Scale P-Side Down Au(80)Sn(20) Eutectic Die Attach using a Pulsed Heat Pick Tool

A close-up view of the Palomar Technologies Model 6500-WSP with a 6" steady state heater wafer stage, pulsed heat pick tool, and lookup camera with alignment algorithm that was used for execution of this work is shown in Figure 11.

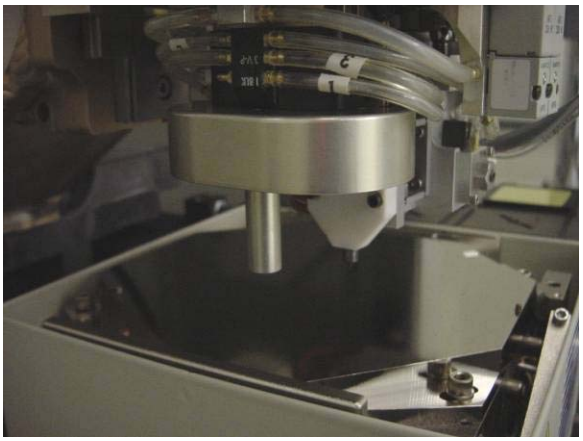


Figure 11 – Steady State Heater Wafer Stage and Pulsed Heat Pick Tool Optimized for Laser Diode Eutectic Solder Attach

The pulsed heat tool is controlled through a temperature profile as shown in Figure 4. This is not the profile used for production but it shows a representative shape. While holding the laser die in place on the heated wafer, the tool's temperature ramps from a background temperature to the eutectic reflow temperature, maintains the temperature during the reflow cycle, and then cools down to the background temperature by means of forced cooling.

The pulsed heat tool used to pick the laser die includes the following capabilities and benefits:

- Pulsed heat controller with real-time feedback and closed loop control
- Temperature up to 600C
- Temperature accuracy ±3C
- Fast ramp (up to 65C/s) - minimal overshoot
- Die is at high reflow temperature for a limited time only
- Programmable 'point and click' profiling
- Real-time data logging of each profile execution

The wafer assembly process steps include:

- Load wafer onto steady state heated stage and enter the wafer ID (identification, barcode, etc.)
- Load laser die Gelpak™ (pre-flipped with P-Side down) onto machine and enter the Gelpak™ ID (identification, barcode, etc.)
- Automatically download the Wafer INPUT map describing available substrate sites for population
- Repeat the following process for all substrate sites:
  - Vision find wafer at next available substrate site (per wafer INPUT map)
  - Vision find N-Side of next available laser die and pick it
  - Vision find P-Side of laser die on pick tool using lookup camera with laser alignment algorithm
  - Align and place laser die to substrate site
  - Apply bond force and initiate pulsed heat profile
  - Release laser die upon completion of pulsed heat profile including forced cooling cycle to below reflow temperature
  - Optional in the machine program: use the machine vision system to make N-Side measurements of placement accuracy and store to a data file (allows real-time monitoring of placement accuracy during build cycle)

Wafer Scale – Considerations

- P-Side down laser die attach is accomplished across multiple (1000X) substrates on a single wafer. Each laser die is pulsed heat reflowed at a vision guided substrate location and then removed from heat. Wafer scale laser die attach must consider the affects of both solder aging and accuracy consistency as lasers are attached across the entire wafer area on the bonding equipment.
- Solder aging at temperature is typically not considered for singulated substrates since the solder is exposed to temperature for a short duration of time only. When moving to wafer level substrates however, solder can be exposed to background temperatures over 200C for tens of hours depending on the number of bond sites and process throughput.
- Tables 3 and 4 provide a summary of the results from a study on the effects of exposure to time at temperature. A combination of time intervals at a background temperature of 230C was used to evaluate both non-reflowed solder and reflowed solder in completed assemblies. The study involved waiting the pre-bond time intervals and then attaching a set of 4 laser die each. These laser die sets were then sheared after waiting the post-bond time intervals. This particular test sequence allowed testing of solder exposure to temperature before laser die attach (0 to 72 hours), solder exposure to temperature after laser die attach, and a combination of both (0 to 96 hours = Pre-bond Attach Time + Post-bond Shear Time).

Table 3 – Average Shear Strength vs. Time

Shear Average [grams]		**Post-bond Shear Time [Hrs]**				**Shear Time [Hrs]**
		0	24	48	72	0
Pre-bond Attach Time [Hrs]	0	270	275	310	253	24
	24	217	210	241	193	48
	48	239	206	202		72
	72	192	189			96
	Grid	1		2		

Table 4 – Shear Strength Range vs. Time

Shear Range [grams]		Post-bond Shear Time [Hrs]				Shear Time [Hrs]
		0	24	48	72	0
Pre-bond Attach Time [Hrs]	0	36	128	128	87	24
	24	53	21	90	38	48
	48	6	7	119		72
	72	24	31			96
	Grid	1		2		

Table 3 shows a reduction in average shear strength from 270 grams to a minimum of 189 grams over all aging conditions compared to zero pre-bond attach time and zero post-bond shear time. Visual inspection of the sheared samples showed no observable differences in solder joint quality at 60X magnification. Table 4 shows the effect on shear strength range for each data set. The data did not indicate a significant degradation of shear strength range for pre-bond attach time or post-bond shear time exposure.

Case 3: AuSn (ASIC) 453x274x12mil with Preform and Pulsed Heat Bottom Up

The die shown in Figure 12 are significantly larger than those presented in cases 1 and 2, and they are classified in eutectic solder processes as large die. The main challenges for large die are relatively void-free solder coverage under the die without creating too much or too little solder outflow past the fillet. Large die examples include the preforms of various compositions, shown in figure 12. Large die applications require optimization of preform volume, substrate base temperature, placement force, pulsed heat stage profile, and scrub pattern.

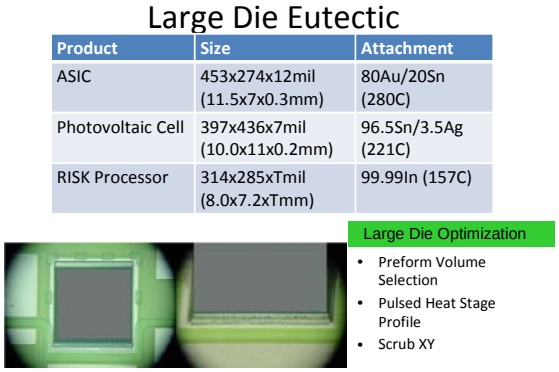


Figure 12 – Large Die Eutectic Attachment

Proper selection of solder volume is required to avoid the significant outflow of excess solder shown in the left side of Figure 13. The figure shows three separate views for the excess volume and three views for proper volume. The Top view illustrations compare the final solder coverage and flow as captured by means of acoustic microscopy. The "Excess Volume" view shows too much outflow which may be challenging if die are placed next to each other at a relatively close distance. The "Before" view shows the preform under the die before reflow and the "After" view shows the same die after reflow. This case was built using a four-sided inverted pyramid pick tool with scrub in two directions and pulsed heat stage during reflow.

Although not shown in figure 13, one can also use too little solder volume, resulting in voiding under the die and a poor fillet.

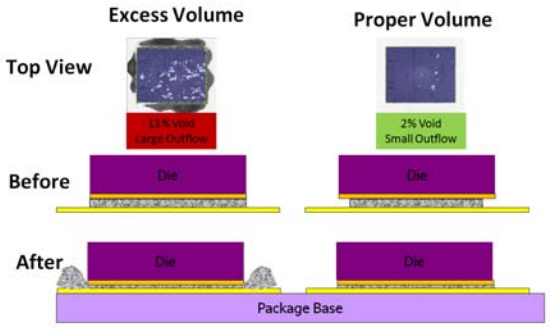


Figure 13 – Preform Sizing on Solder Outflow

Summary and Conclusion

In this paper we have provided an overview of eutectic die attach processes to help design and process engineers select equipment and processes for die and substrates that require high thermal dissipation and/or fluxless processes.

A background of eutectic die attach was presented along with various combinations of substrate and die plating materials.

Three specific cases were then presented to provide the reader with a range of real-world applications including setup and results:

Case 1: AuSi (RFSOE) 16x63x4 & 31x64x4mil

Case 2: AuSn (P-Side Down) 12x10x12mil with preform using pulsed heat top down

Case 3: AuSn (ASIC) 453x274x12mil with preform using pulsed heat bottom up

References

1. Jonathan Harris, "Selecting Die Attach Technology for High Power Applications", Power Electronics Technology, Nov 1, 2009 12:00 PM (http://www.ormetcircuits.com/m/Selecting%20Die%20Attach%20Technology%20for%20High-Power%20Applications%20Page%20of.pdf)
2. Evans, D. et al, "Micron Level Placement Accuracy for Wafer Scale Packaging of P-Side Down Lasers in Optoelectronic Products", The 42nd International Symposium on Microelectronics, San Jose, CA, November 2009
3. Surface Mount Equipment Manufacturers Association (no date), SMEMA Mechanical Equipment Interface Standard, Interface Standard 1.2 Retrieved from http://smema.ipc.org/smema1.2.pdf