Ink-jetting for Electronic Assembly

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Abstract

We report experimental results on applying ink-jetting to dedicated system-in-package technologies. Special focus is on die-attach, vertical and horizontal interconnects. Our experiments on die attach experiments demonstrate that today we have still too high expenses to adapt materials, filler size and viscosity. The filling experiments of 150µm diameter vertical through encapsulant vias for package-on-package applications with ink-jetting showed void formation, which requires still smaller ink jet drops in the future. For formation of horizontal interconnects, e.g. for rerouting, by ink-jetting we observe that a functionalization of the surfaces e.g. with plasma or sulfur acid is required. Based on these project results and experience we suggest a roadmap for ink-jetting using parallel nozzles and single nozzles.

Key Words: ink-jetting, system-in-package, silver ink, solder stop, solder paste, roadmap

Introduction and Motivation

During the last years progress on ink-jetting made this technology attractive for microelectronic applications. Progress was achieved both for inks and equipments. Especially nano-particles brought much progress to inks that allowed higher resolution at adequate sintering temperatures. A selection of references is given in [1-19].

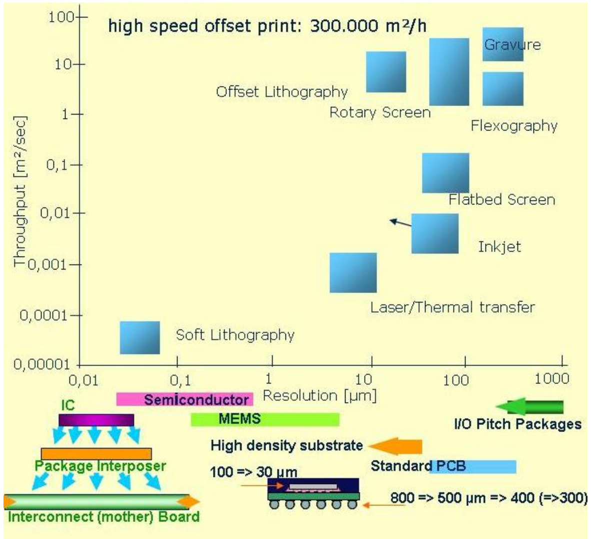
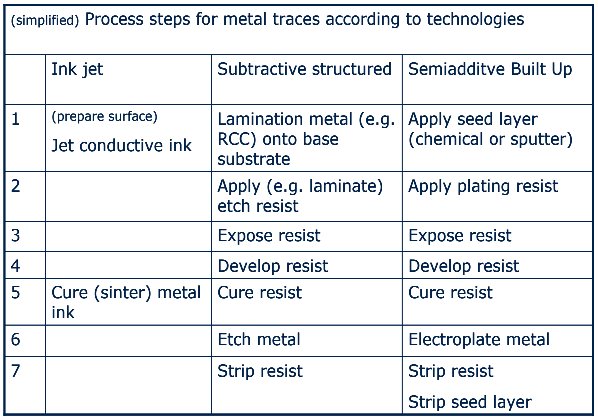


Figure 1: Accuracy versus speed dilemma for different printing methods. The lower part shows the dimensions on chip/package/board level.

Figure 1 presents a generic overview of printing methods in correlation of throughputs and resolutions. The plot demonstrates the problem of accuracy and speed for different printing methods.

Advantages for ink-jetting are tool-less production, low cost, no chemical waste (environmental friendly) and the possibility for corrections by applying software. Tool-less production means production without masks, stencil or screen. Figure 2 compares the attractive advantage of the two steps ink-jetting with the seven steps PCB manufacturing.



(simplified) Process steps for metal traces according to technologies

	Ink jet	Subtractive structured	Semiaddditve Built Up
1	(prepare surface) Jet conductive ink	Lamination metal (e.g. RCC) onto base substrate	Apply seed layer (chemical or sputter)
2		Apply (e.g. laminate) etch resist	Apply plating resist
3		Expose resist	Expose resist
4		Develop resist	Develop resist
5	Cure (sinter) metal ink	Cure resist	Cure resist
6		Etch metal	Electroplate metal
7		Strip resist	Strip resist Strip seed layer

Figure 2: Formation of metallic traces: The two step ink-jetting process compared to the seven steps PCB process.

Although ink-jetting is used for printing on paper today it is not used in electronic mass markets. One reason is just the amount of printing area. For a rotary screen printing newspaper the demand is to print at good resolution and day by day an amount of more than 100,000m² per page / design, often more than 100 pages. Here the investment is huge, justified by volume, and has taken much time to have the equipment and inks ready to print on paper. In electronics packaging, we simply do not have these volumes per area and design. Further we do not have paper to print on but various surfaces, none of them with paper like properties like flexibility and the ability to absorb the ink, furthermore one simple pixel error may result in a non-operative product. When talking about ink-jetting in electronics manufacturing, this has to do with suitable materials to be printed, surface preparation, process control, high reliability and last but not least the speed versus accuracy trade-off.

This work is organized as follows: After this introduction and motivation we report and discuss our experimental results on applying ink-jetting to dedicated system-in-package (SiP) technologies. Special focus is on ink-jetting for die-attach, vertical and horizontal interconnects. Based on these results and experiences we suggest roadmaps for ink-jetting with parallel nozzles and single nozzles.

Our experiments on die attach demonstrate that today we still have too high expenses to adapt materials, filler size and viscosity. The filling experiments of 150µm diameter vertical through encapsulant vias (TEV) for package-on-package (PoP) applications with ink-jetting showed significant void formation. Still smaller ink jet drops are required for less void formation. For horizontal interconnects, e.g. for rerouting, we observe that a functionalization of the surfaces e.g. with plasma or sulfur acid (H_2SO_4) is required. Today's application for ink-jetting in electronics is especially prototyping because no hardware tooling is required (computer integrated manufacturing, CIM). The roadmaps for ink-jetting between 2010 and 2015 suggest increasing use for MEMS, MID, and PoP. Attractive applications from 2012 could be ink-jetting of solder paste and dielectrica or electrical conductive interconnects, especially on 3D- structures because the tools are not touching the device itself.

Project Results

In this work we investigated especially two test vehicles. Firstly, we investigated the use of ink-jetting as alternative approach for insulated die attach, which is important in high voltage switching circuits (see Figure 3). Secondly, we investigated ink-jetting applied to a typical package-on-package (PoP) test structure of vertical and horizontal interconnects (see Figure 5).

The common method to apply highly electrical insulation with thermal conductive glues for die attach is dispensing. Some of the quality parameters here can be influenced by the applying process. A thin bond line delivers a low thermal resistance. Being able to apply highly filled materials is also lowering the thermal resistance. Having a bond line that is void free allows electrical insulation. If the die attach area is printed exactly, then not much material is wasted and bleeding does not occur. We investigated to which extend ink jetting can deliver improvement in terms of speed, insulation or less bleeding.

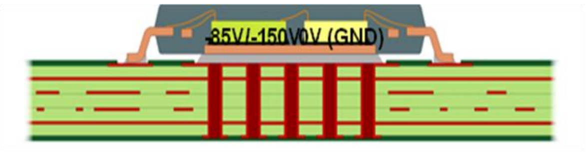


Figure 3: Test vehicle for investigation of ink-jetting for die attach with two chips arranged side by side in a quad flat package type.

We optimized ink heads, steering and materials. Nevertheless printing of all materials is a challenge. Especially the materials promising best thermal conductivity by SiC fillers allowing 1,6W/mK could not be printed satisfactory with the used equipment. Experimental results are shown in Figure 4, where we see the appearance of the bleed out effect, formation of satellite drops and void formation.

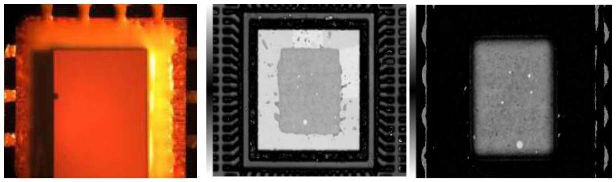


Figure 4: Ink-jetting for die attach. Left: problem of bleed-out effect, center: formation of satellite drops, right: void formation.

At the left picture we see a leadframe. On that leadframe we have ink jetted various pastes and then did die attach. Around the die, the bleeding out of the paste is visible. We measured over 100µm, which is too much for following assembly processes.

The picture in the center shows a leadframe after ink jetting of the adhesive. We see the die attach area is covered with it. Around this, we see additional material, small splatters of the paste. This is a common problem in ink jetting, the “satellite drops”. They occur when secondary drops are created during ink drop forming and are scattering when hitting the target. These satellite drops are less focused.

The last picture was taken from an acoustic microscope focused on the die attach area of the leadframe. On this, filled paste was ink-jetted, then a die attach was performed. The die is transparent in this view, but the paste below is still visible. Here voids have been detected below the die. These voids usually weaken the insulation of the interfaces and thus lowering the yield and reliability.

The second application is related to the structuring of system in package (SiP) solutions with electrical traces. We applied ink jetting technology to filling of vias and structuring of horizontal conductive traces. As test vehicle we created an 8x8 mm^2 daisy chain substrate of 0,45mm thickness with through holes. These holes, which were created by laser application, had 150µm diameter and 0,5mm pitch (see Figure 5).

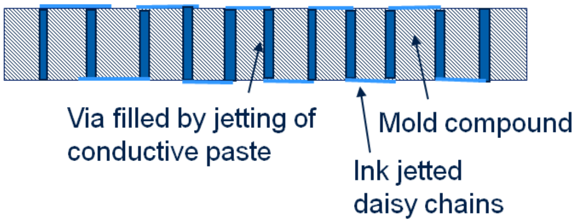


Figure 5: Schematic of the test vehicle for study of ink jetted daisy chains.

Figure 6 shows the filling of vertical through encapsulant vias (TEV) with ink-jetting. The two cross-sections show the formation of voids. Main problem is the large size of the ink-jetting drops, which had a diameter of 250um compared to the 150 um thin vias. The large drops require a subsequent grinding, but this should be avoided here.

Figure 7 shows the filling of vias with alternative plugging technology, where we did not observe the problem of void formation.

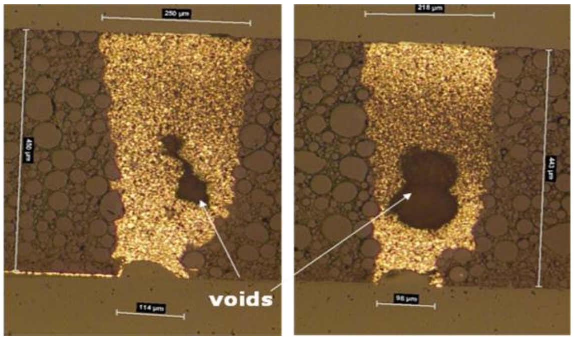


Figure 6: Via tapered and with holes.

To use the vias, at least a further treatment such as back grinding is necessary. But this leads to larger costs and limits application.

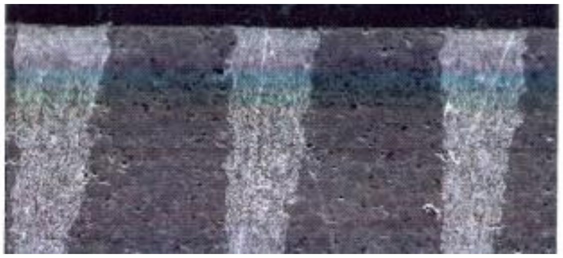


Figure 7: Via filling with alternative plugging PCB technology; no voids were observed.

Of special interest for PoP applications is the formation of conductive horizontal traces with ink-jetting. Figure 8 shows ink-jetted traces of a test structure, which was fabricated with different ink-jetting and drop speed of a 128 nozzles per head (diameter 27µm). The left picture in Figure 8 shows the result for the lowest speed. In this example the nozzles were moved with a speed of 10mm/s over the area to be jetted. A silver nano-ink was used. Every 2 ms drops were generated. Increase of the speed and frequency by a factor of 10 leads to rougher traces (center picture). Because of the high shooting frequencies for the drops the solvent has no time for evaporation. Therefore drops more and more overlap and the traces get broader. The whole experiment gets worse with further increase of the speed. Experiments with heated substrates to remove the solvent faster showed improvements, but increased the danger for blocking nozzles. Each missing drop can cause a non-operative device.

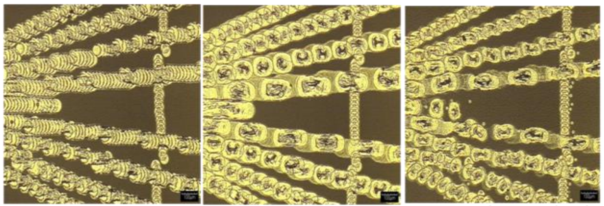
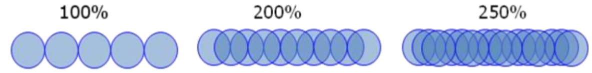

10 mm/s → 2ms/Droplet 80 mm/s → 0.25ms/Droplet 225 mm/s → 0.1ms/Droplet

Figure 8: Formation of conductive traces with different ink-jetting speeds. Lower speed leads to better interconnects.

Figure 9 presents for the different degree of overlaps 100%, 200% and 250% of the drops for different speeds and generated area/second. At smaller traces the jet velocity and power per area decreases accordingly. Best resolution results we achieved for the traces with the smallest diameter (right column in Figure 9).

Nozzle diameter [µm] ==>		D=200	D=100	D=60	D=30
speed	coverage				
line/sec [mm/s]	100%	800	400	240	120
area/sec [mm^2/s]		160	40	14,4	3,6
line/sec [mm/s]	200%	400	200	120	60
area/sec [mm^2/s]		40	10	3,6	0,9
line/sec [mm/s]	250%	320	160	96	48
area/sec [mm^2/s]		25,6	6,4	2,3	0,58



Definition of coverage (each circle represents a jetted drop

Figure 9: Theoretical throughput at a drop frequency of 4kHz @ diameter and coverage.

Figures 10 and 11 show detailed microscope views of vias and traces of interconnects. Figure 10 shows interconnects at the interface between the vertical via and the horizontal conductive traces on top of the package. We observe that the traces are foamy in this area. Figure 11 shows a detailed top view from the top and a cross-section analysis. We observe that the ink-jet drops shrink during sintering.

The results show that a functionalization of the surface is a must. After functionalization (e.g by plasma or chemistry like sulfur acid) we achieve much better results after ink-jetting (compare summary table in Figure 12).

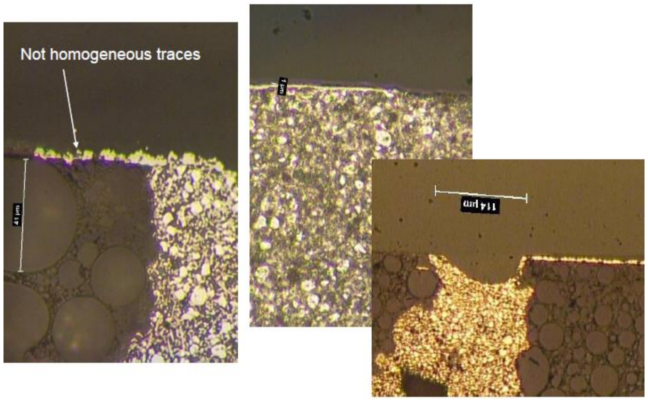


Figure 10: Traces at the interface via to horizontal traces. The traces are foamy in this region.

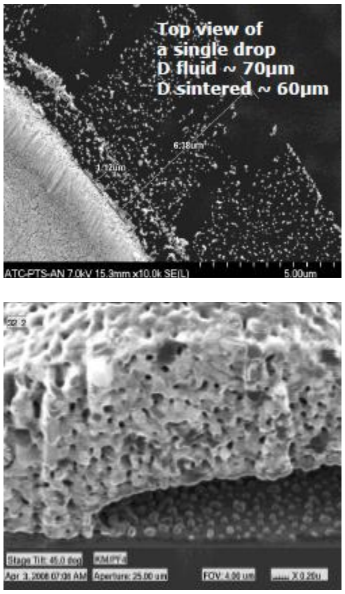


Figure 11: Analysis of the interconnects: view from the top (left), cross-section: the inkjet drops shrink during sintering.

The line width is determined not only by the drop size but also by wetting kinematics, which has a large tolerance without pretreatment. The table in Figure 12 summarizes the results for pretreatment with plasma and sulfur acid.

Surface	Contact Angle Water [°]	Contact Angle Diiodomethane [°]	Surface Energy [mN/m]	Disperse Part [mN/m]	Paolar Part [mN/m]
Base material A H2SO4 + Ag2SO4	87,8±0,6	40,6±1,7	40,7±0,4	39,3±0,4	1,4±0,1
Base material A Ar/O2-Plasma	94,3±1,0	60,1±2,7	30,9±0,6	28,6±0,5	1,5±0,1
Base material B H2SO4 + Ag2SO4	79,0±1,9	36,6±3,9	44,8±1,1	41,3±0,9	3,5±0,2
Base material B Ar/O2-Plasma	83,6±3,6	57,9±4,7	34,2±1,2	29,8±0,9	4,4±0,3

Figure 12: Summary of surface functionalization with plasma and chemicals.

Conclusion: Ink-jetting for different applications

Based on the results and experiences of our studies a roadmap for applying ink-jetting technologies in PCB and packaging was derived. Figure 13 shows the elaborated roadmap for ink-jetting with parallel nozzles. Here we see increasing use of ink-jetting for niche markets like MEMS, MID, 3D structures, PCB or PoP applications. Attractive applications from 2012 are direct printing of solders stop and printing of seed layers.

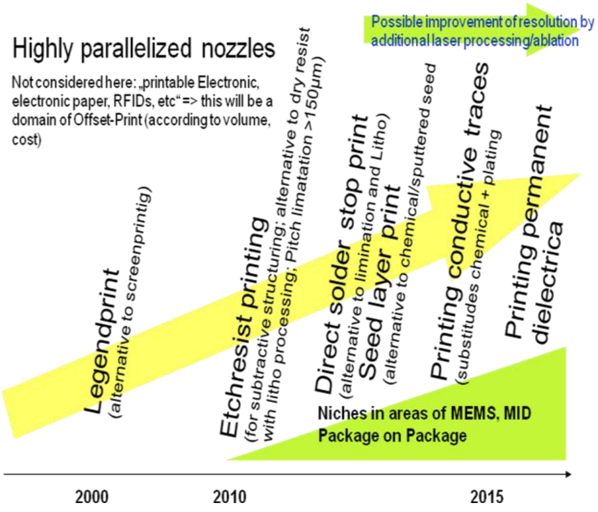


Figure 13: Roadmap for ink-jetting with parallel nozzles. Between 2010 and 2015 increased use of ink-jetting for MEMS, MID, 3D structures, PCB and PoP application is seen.

Figure 14 shows the elaborated roadmap for ink-jetting with one nozzle only. Since years jetting of underfill is well established. From 2010 we see a strong use of ink-jetting for different MEMS technologies. Examples are dam and fill or sealing of MEMS. Typical future application areas are jetting of solder paste, printing of dielectrica and electrical conductive traces.

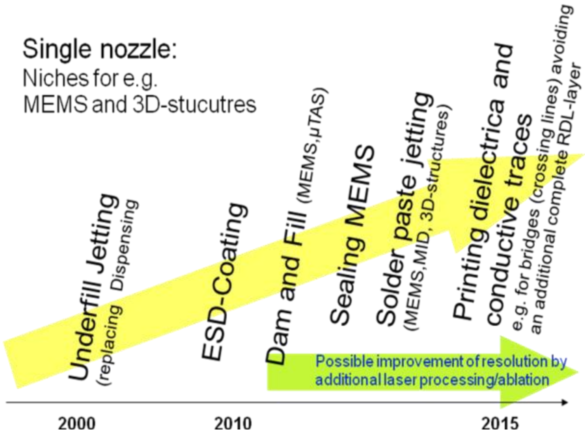


Figure 14: Roadmap for ink-jetting with one nozzle. From 2012 jetting of solder paste, printing of dielectrica or electric conductive traces could be attractive applications.

Currently ink jetting in the electronics industry is well suited for dedicated applications especially in the area of MEMS. For single nozzle systems sealing of MEMS or solder paste jetting can be done. Especially in case of prototype building, ink jetting has an advantage. For production, ink jetting can be used, where e.g. the metal content per layer is extremely low such as for bridging single lines to save a complete second metal layer. If productivity is increased by multi nozzle systems legends can be printed, etch resist or a solder stop. Today’s place for ink-jetting in the electronics industry is where prototypes are needed only or where the area to be printed on is extremely small versus the total processing area.

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