Impact of Mechanical Simulation Methodology on Electronic Package Reliability Assessment with Applications to 3D TSS Technology

Zhongping Bao, James Burrell
Qualcomm Inc,
5775 Morehouse Drive
San Diego, CA 92121

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2010/1/000170/2253126/ism-2010-tp1-paper2.pdf by guest on 14 June 2024

Abstract

Mechanical reliability issues in electronic packages have drawn significant attention in semiconductor industry for decades and have increased product development cost significantly. Recent rapid growth of various portable electronic devices like smartphone and smartbook with increasing demand for more functionality in tighter space further challenges the limit of mechanical reliability. To reduce the product development cost and time-to-market, mechanical simulation has been extensively employed in semiconductor industry for the purpose of design optimization and reliability assessment. The importance of having the correct simulation methodology can't be overemphasized considering the extent of its utilization throughout the product development cycle. In this paper, we will discuss three fundamental mechanical modeling methodologies that are widely used for simulating flip-chip overmolded packages. These approaches are generally used to simulate package warpage at End-of-Line (EOL) as well as to assess package reliability from a stress point of view. The first approach we studied in this paper is to assume that the package is initially stress-free at a given uniform temperature, which is usually taken to be the peak temperature of the mold cure profile. However, this differs from the actual assembly process where package composition and cure profiles are different at each assembly processing step. The second approach simply accounts for that fact and assigns different stress-free temperature to each individual package component. For example, the die is assumed to be stress-free at the chip attach temperature and substrate is assumed to be stress-free instead at the substrate baking temperature. This approach captures more physics compared to the first approach. The last approach explores that idea further by simulating the actual assembly process, step by step, through element removal and addition techniques available in the software. Such study is also carried out for a flip-chip overmolded package with Through-Silicon-Stacking (TSS) technology. Both Die-to-Die-first (D2D) and Die-to-Substrate-first (D2S) processes are examined. Simulated warpage, as well as reliability assessment regarding different failure mechanisms using these three modeling methodologies are discussed in detail. The paper is prepared to the best knowledge of authors and those statements do not necessarily reflect opinions of Qualcomm Inc. Some data shared in this paper is normalized such that no commercial confidential information is published.

Key words: electronic packaging, mechanical simulation, reliability assessment, TSS, TSV, warpage

Introduction

Advances in CMOS technology have been steadily improving processor performance moving from one technology node to the next[1,2]. Higher performance with lower cost in smaller form factor become a major driving force for packaging development. To reduce the cost of product development and time-to-market, mechanical simulation is commonly used to assess package design and reliability integrity. However, inconsistent or incorrect mechanical simulation methodologies always raise questions on the validity of numerical results and derived design recommendations. In turn, it may discourage the employment of mechanical simulation in product development cycle and diminish to a large extent benefits from simulations. This paper represents a first attempt at quantifying the impact of mechanical simulation methodologies on package reliability assessment with demonstration to TSS technology. Our work focuses on flip chip overmolded packages, and examines package EOL warpage and residue stress in silicon. We do not consider any effect from wafer processing or include any modeling results of standard reliability testings, such as thermal cycling and drop test in this paper.

Material thermomechanical properties are required to perform stress simulation and its accuracy is critical for predictive modeling. Therefore, we will first describe our material characterization results briefly and present DMA results on 4-layer laminated substrate. The second section will summarize different simulation methodologies that are examined in this paper. Numerical results on two test vehicles (TV) will then be presented in the next section. One TV is an overmolded package with 2 flip-chip dies. The other TV is an overmolded package with a memory die stacked on top of a logic die using Through-Silicon-Via (TSV) technology. Finally, discussions and our key recommendations are included at the end of the paper.

Material Characterization

Our internal packaging lab has established industry-leading material characterization capabilities in recent years. Q800 DMA system from TA Instruments [3] shown in Figure 1 is one of their latest investments and shown in the same figure is a 5mm 3-point bending kit for small sample testing. A 4-layer laminated substrate was tested and sample orientation is shown in Figure 2.

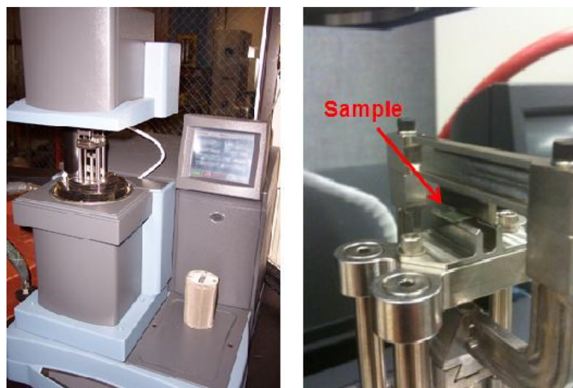

FIG 1. TA Q800 DMA system and 3-point bend kit

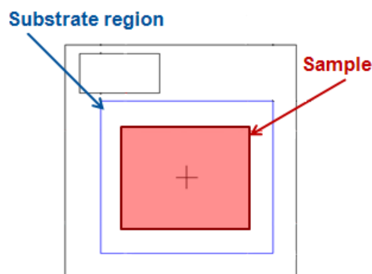

FIG 2. Sample preparation for material testing

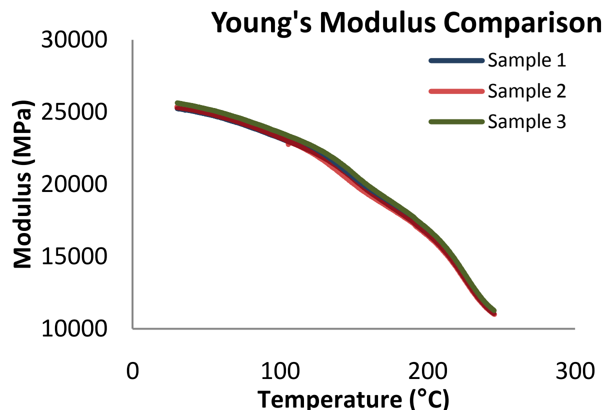

FIG 3. (Color online) Modulus measurement on the substrate

Dynamic Mechanical Analysis (DMA) measures the modulus and damping properties of materials while applying a periodic stress to the sample. The time-dependent storage (E') and loss moduli (E") are monitored by the Q800 DMA and are used to derive the material's Young's modulus by using the following equation:

$$\sqrt{E'^2 + E''^2}$$

To obtain the substrate's mechanical properties, three samples were precisely cut and tested from the substrate region underneath the die. Since composite material's elastic strength depends strongly on temperature, DMA tests were performed from 25 ℃ to 245 ℃ which also meets stress modeling needs. The temperature-dependent Young's modulus was plotted in Figure 3. The average modulus for the three samples at room and high temperature are ~25.4 GPa and ~11.1 Gpa, respectively. Clearly, the substrate is much stiffer at room temperature than at high temperature (~2.3 times).

Mechanical Simulation Methodologies

Mechanical simulation has been adopted widely in the electronic packaging industry for design optimization, process evaluation and reliability assessment. Before applied to any such purposes, the model must be validated with experimental data. As widely accepted as an important metric for product qualification, package warpage at EOL is a first data point for such validation. Several mechanical simulation methodologies exist to capture package warpage. Here we describe three commonly practiced ones among others. Depending on the understanding of assembly process and material physical behavior, they differ in detailed assumptions embedded in the

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2010/1/000170/2253126/isom-2010-tp1-paper2.pdf by guest on 14 June 2024

simulation techniques. To establish sound comparison between numerical results, a simplified common assembly process is assumed for flip-chip overmolded packages, as demonstrated in Figure 4 for all simulation methodologies we studied. The first step during the assembly process is baking where substrates are usually held at 150°C for certain amount of time. The next step is chip attach (C/A) during which the flip-chip bumps are reflowed onto substrates. Capillary underfill (UF) follows that step and the underfill is cured for the protection of flip chip bumps. Finally, mold compound (MC) is added to the package and encloses die as well as underfill. This completes the assembly process assumed for the study at hand and the EOL package warpage can then be simulated. Figure 4 also includes a presumed peak temperature for the profile associated with each assembly process step. Peak temperature of each profile will be used as initial stress free temperature in the simulations in the following study.

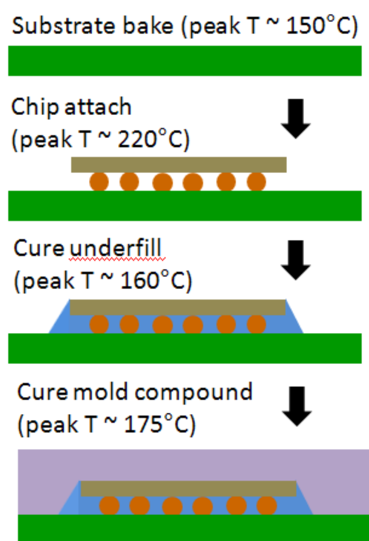

FIG 4. (Color online) Simplified assembly process for flip-chip overmolded packages

The first mechanical simulation methodology we studied in this paper to capture EOL package warpage basically focuses on the last step in the assembly process and assumes that package is stress free at the peak temperature of the molding step, ~175°C in this case. During implementation for such a simulation, a static step is carried out with a simple uniform temperature field change. If we were looking at wire-bonded dies in an overmolded package, this may not be a bad assumption since there are no strong deformation coupling between die and substrate due to flip chip bumps. Because Tg of underfill is usually 60°C~90°C and therefore its elastic modulus is reduced about 5 to 10 times when the temperature goes above 100°C, the die and substrate shall be roughly stress-free at 175°C. However, with flip-chip bumps in place, the solidified solder bumps provide strong deformation coupling between die and substrate after C/A process. As a result, the underlying assumption of the first approach becomes questionable.

The second approach re-examines the assembly process and notes each component in the package is introduced as stress-free at different temperatures. Though each component is also introduced at different step, this approach assumes that linear superposition is valid. Consequently, in the numerical model each component is assigned with a specific initial temperature where it is assumed to be stress-free. Again, a single static step is carrier out in the numerical scheme but this time it is associated with an un-uniform temperature field change. In such analysis geometry and boundary of each component is pre-defined as in initially constructed geometry configuration. Unless there is significant deformation introduced at each assembly process step, this approach would be a good approximation. Nevertheless, deformation at each step is probably not negligible for flip-chip overmolded packages. For example, at C/A step, due to large number of flip-chip bumps, there is a considerable amount of deformation on both silicon and substrate. Subsequently, at UF step, underfill is dispensed between silicon and substrate. Its geometry and boundary must be constrained by the deformation introduced at previous step. These underlying physics is not captured correctly by the assumptions of the second approach.

The third approach studied in this paper considers both the temperature and deformation history presented in the assembly process. By invoking element removal and addition techniques provided in the software, it activates and deactivates corresponding element sets accordingly. Numerically, either a sequence of static or viso-elastic analysis steps can be implemented to capture package warpage at EOL. Viso-elastic analysis would require physical time and visco-elastic material properties incorporated in the numerical model. Such an approach is closest to the reality and shall provide a sound baseline to the other methods. On the other hand, because it includes actual physical steps and considers material visco-elastic behavior, the associated computational cost would be sizeable.

Impact on Flip-chip Overmolded Package

As mentioned in previous section, we studied three different mechanical simulation

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2010/1/000170/2253126/ism-2010-tp1-paper2.pdf by guest on 14 June 2024

methodologies to capture package warpage at EOL. Comparisons of numerical results from these three approaches are discussed here. The TV is a 12.6x6.2mm package with 2 flip chip dies and 0.24mm laminated substrate which is shown in Figure 5. Die 1 is 4.0x6.6mm and die 2 is 4.0x4.3mm; both are 250um thick. To validate the modeling, 5 actual devices were measured for warpage at substrate bottom surface from 50°C to 200°C and averaged values are reported. Figure 6 summarizes data from measurement and simulations based on three numerical approaches discussed above on a normalized scale. Results from approach 1 and approach 2 seem overpredicting package warpage over the entire temperature range compared to measurement. The simulated values of these two approaches at 50°C are about 70% larger than measured values and there is no significant difference between numerical results based on those two approaches. The third approach captures package warpage at EOL much better but still has an error ~18%. The numerical scheme does not take into account of other process related loading and boundary conditions which may cause such error. It is also worth noting that numerical predictions all deviate from the actual measurement when temperature is beyond 80°C. This very likely is caused by the fact that only elastic material properties are used in the simulations. Consequently, the glass transition behavior of underfill which happens around 60°C~90°C is not captured correctly. Mold compound goes through glass transition at slightly higher temperature. It is obvious from figure 6 that the predicted values diverge even further at 150°C from measured values. It is recommended to perform a visco-elastic analysis with necessary material properties if package warpage at high temperature is

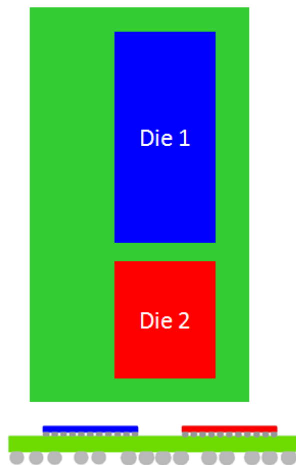

FIG 5. (Color online) Test vehicle package configuration

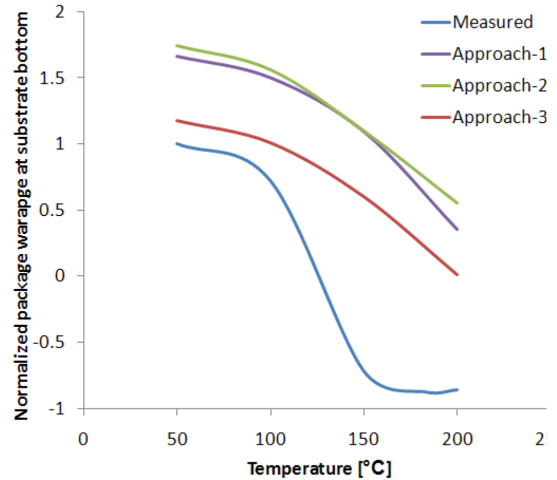

FIG 6. (Color online) Normalized package warpage at substrate bottom (both measured and simulated)

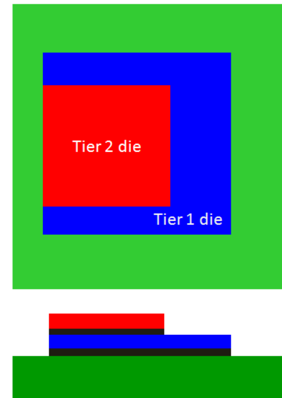

FIG 7. (Color online) Test vehicle configuration with TSV technology

desired. On the other hand, the third approach discussed in previous section containing static analysis with elastic material properties only can provide a reasonable estimation for package warpage at EOL.

TSV has been the critical enabler for 3D stacking technology and in recent years it has gained significant momentum [4,5]. Compared to standard flip chip overmolded packages, its assembly process is much more complicated and far more challenging. Depending on process and cost considerations, TSS can have die-to-die (D2D) stacking first or die-to-substrate (D2S) attachment first among other options. Mechanical simulation of such device and process becomes difficult. Package EOL warpage is a good validation for mechanical simulation methodologies and we presented our preliminary findings below. The current TV has 2 flip chip dies stacking on top of

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2010/1/000170/2253126/ism-2010-tp1-paper2.pdf by guest on 14 June 2024

each other. Tier 1 die attached to the substrate is 11x9mm and tier 2 die is 8x8mm stacked on top of tier 1, see Figure 7. We applied the third approach discussed in previous section to simulate both D2D and D2S processes. For comparison purpose, the same geometry configuration is simulated using the first approach as discussed previously which is assuming a uniform temperature field change and a static analysis step. Because of its assumptions the first approach can not differentiate D2D and D2S processes. In present numerical models, boundary conditions (BC-1 in Figure 8) are applied such that no rigid body motion is allowed. To improve yield and manufacturability, during assembly process, substrate may be held on a vacuum chuck. Package warpage measurement on mold compound surface at EOL is sometimes done with the same boundary condition as well. Such boundary conditions are typically different from what we usually assume for warpage modeling (BC-1). This scenario is also considered here (BC-2 in Figure 8). Based on numerical results summarized in Figure 8, D2S process always generates smaller EOL package warpage, about 10% less than D2D process. Package warpage predicted by approach 1 has 50% error for the case with BC-1 but is surprisingly close to result of D2D process for the case with BC-2. The absolute package warpage at EOL is very small for the case with BC-2 because the substrate bottom surface is constrained by a vacuum chuck. To verify if the simplified approach 1 can capture correctly the stress field for the case with BC-2, Figure 9 showed stress contour plot in tier 1 die at EOL from both D2D and approach 1. The max principal stress, as well as inplane normal stress (S11 and S22) is different between these two approaches, both in overall profile and magnitude. Thus, it is not recommended to apply any such simplified simulation methodologies for flip-chip overmolded packages with TSS technology.

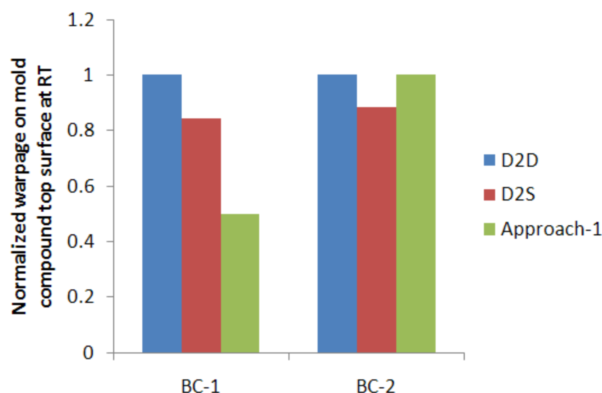

FIG 8. (Color online) Normalized package warpage at mold compound top surface

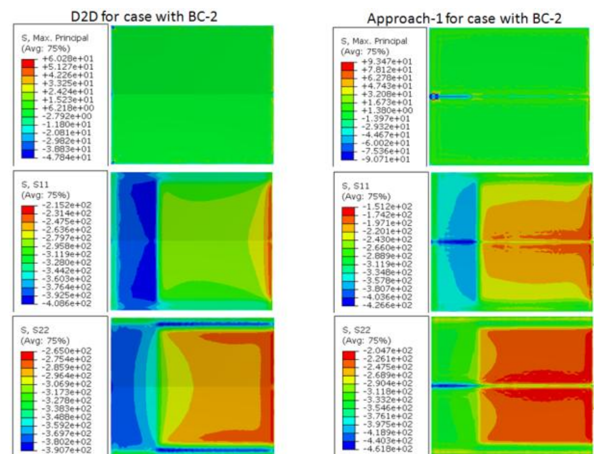

FIG 9. (Color online) Tier1 die stress at EOL as calculated for D2D process and for approach-1

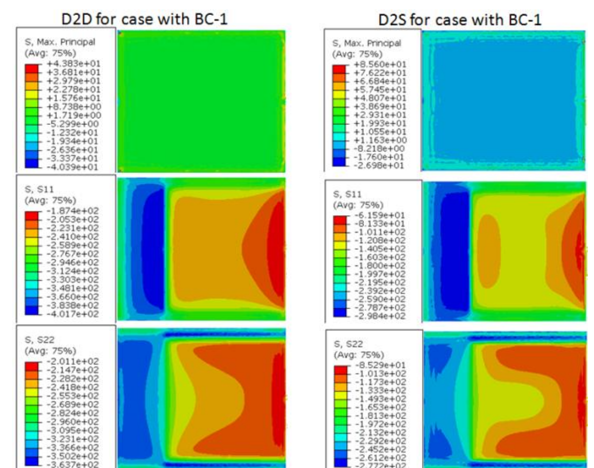

FIG 10. (Color online) Tier1 die stress at EOL as calculated for D2D process and for D2S process

While displacement field provides good validation for numerical models, one would be more interested in the stress field which impacts reliability and performance. It is also interesting to compare the stress field caused by D2D vs. D2S processes. Figure 10 captures such comparison for the case with BC-1 at EOL where only rigid body motion is excluded from the model. Max principal stress in tier 1 die at EOL for both processes is much lower than the silicon material strength so die cracking shall not be a major failure mechanism at EOL. The largest max principal stress in tier 1 die at EOL of D2D process is 50% of that of D2S process. This probably is due to the fact that with D2S process attaching tier 2 die may introduce localized stress. Looking at inplane normal stress, D2D process introduces significant larger amount of compression stress in tier 1 die

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2010/1/000170/2253126/isom-2010-tp1-paper2.pdf by guest on 14 June 2024

outside the tier 2 die shadow region, roughly ~30% larger. Devices which performance may be negatively affected by large compression stress shall be placed under tier2 die shadow region then.

Conclusions

In this paper we examined three mechanical simulation methodologies and shared numerical results on flip-chip overmolded packages. The simplified approaches which are the first and the second discussed in section 3 do not provide accurate EOL package warpage predictions. The error can be over 50% compared to actual measurement. On the opposite, the third one which takes into account of actual assembly process details presentes reasonable estimation for EOL package warpage. This is the one we recommend for EOL package warpage simulation. Results from all three approaches diverged from measurement at high temperature possibly due to lack of visco-elastic analysis and corresponding material properties in the model. It is recommended to perform viso-elastic analysis if warpage at high temperature is needed.

Simulation of flip-chip overmolded package with TSS technology is also examined and results for both D2D and D2S processes are included. It is clear that only the recommended approach above shall be used for simulating the complicated assembly process associated with TSS to obtain package warpage at EOL. It is interesting to note that D2D process introduces less max principal stress but larger inplane compression stress in tier 1 die compared to D2S process. Tier 2 die shadow region on tier 1 die has smaller inplane compression stress under both conditions. Devices which performance may be negatively affected by large compression stress shall be then placed under tier2 die shadow region.

Acknowledgements

We would like to thank Alan Choi of Qualcomm for his help with the substrate material testing, and Mark Nakamoto and Riko Radojcic, also of Qualcomm, for numerous discussions on TSS technology.

[1] Havemann, R.H., Hutchby, J.A., ‘High-performance interconnects: an integration overview’, Proceedings of the IEEE, Issue 5, pp. 586-601, May 2001

[2] E. P. Gusev, D. A. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P. C. Jamison, D. Neumayer, M. Copel, M. A. Gribelyuk, H. Okorn-Schmidt, C. D'Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L. Ragnarsson, P. Ronshein, K. Rim, R. J. Fleming, A. Mocuta, and A. Ajmera, "Ultrathin High-κ Gate Stacks for Advanced CMOS Devices," *IEDM Tech. Digest*, p. 451 (2001)

[3] http://www.tainstruments.com/

[4] SEMATECH 3D wiki http://wiki.sematech.org/

[5] Garrou, P., ‘3-D Integration Technology and Industry Update’, 3-D Architectures for Semiconductor Integration and Packaging, Dec 2009

Downloaded from http://meridian.allenpress.com/ism/article-pdf/2010/1/000170/2253126/isom-2010-tp1-paper2.pdf by guest on 14 June 2024