Enabling Robust Copper Fill of High Aspect Ratio Through Silicon Vias

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Abstract

Today's Through Silicon Via (TSV) processes are limited to aspect ratios of 10:1. High performance logic devices drive the need for aspect ratios approaching 20:1 in order to achieve the desired performance while simultaneously reducing costs. The reduced via area required on the wafer enables the designer to utilize less real estate on the die to reduce cost or to potentially add redundant vias to improve yield. However, current conventional processes and techniques are not capable of achieving robust fill on aspect ratios greater than 12:1. This presentation will highlight the technical challenges in achieving robust copper fill on super high aspect ratio TSV structures. Additionally, a compelling, economic solution pathway will be presented that integrates a low temperature conformal high quality dielectric isolation layer, a high step coverage Cu barrier / seed technology and a void free high speed electroplating process with a wide process window that could accelerate the adoption of the high aspect ratio TSV design schemes.

Key Words: Through Si Via, dielectric liner, PVD barrier/seed, and Cu electroplate

Introduction

The shift to through silicon vias (TSV) is primarily to enable 3-D packaging, in which multiple chips can be stacked into a single module. These stacked chips are then connected with short TSV copper interconnects to increase device speed and reduce power consumption. The resulting 3-D TSV packaging offers the benefits of increased functionality in a much smaller footprint for mobile electronics applications.

Copper interconnects in TSVs rely on a conventional damascene deposition sequence of PVD copper barrier-seed, followed by electrochemical copper fill to create the "pillars" that connect one chip to another. Compared to traditional dual-damascene copper interconnects, TSV features are extremely deep, in some cases as deep as 200µm. High aspect ratio structures make deposition of conformal seed layers extremely challenging. Non-conformal copper seed layers have minimal sidewall coverage and can lead to void formation during the subsequent copper TSV fill step, which negatively impacts device reliability. To electrically isolate the embedded Cu wires from the Si substrate, an insulating layer is applied prior to metallization. As with barrier/seed, achieving good step coverage in high aspect ratio features is essential.

Addressing the technical challenges posed by high aspect ratio vias must be balanced against the need for low cost. In this paper we discuss how each unit process was optimized for successful integration while maintaining lowest possible cost.

Dielectric Liner (PECVD)

TSVs require a dielectric liner film that can be deposited over a range of temperatures, depending on the application it will be used for (via-middle or via-last). The primary requirement in a TSV liner is a film quality that includes good electrical isolation performance – leakage, breakdown strength, dielectric constant, film stability and compatibility with metal barriers. In addition, the film needs to have adequate step coverage so that the CMP over-burden is minimized. The film needs to be free of any Si-OH moieties that can compromise the reliability of the TSV by attacking the metal barrier film. Complicating this objective is the need for achieving all the above requirements at low process temperature (<180 °C in the vias last, backside case).

Conventional PECVD technology isn't really suited to providing conformal coverage on TSV structures with high aspect ratios, so significant innovation is necessary to ensure quality films. Advanced plasma-based deposition technology has been developed to deliver high quality TSV liner

films that are extremely stable. FT-IR of an as-deposited film shown in Figure 1 shows no Si-OH related peaks. Dielectric integrity of these films is comparable to that of conventional PECVD, even at deposition temperatures of 180 °C and lower.

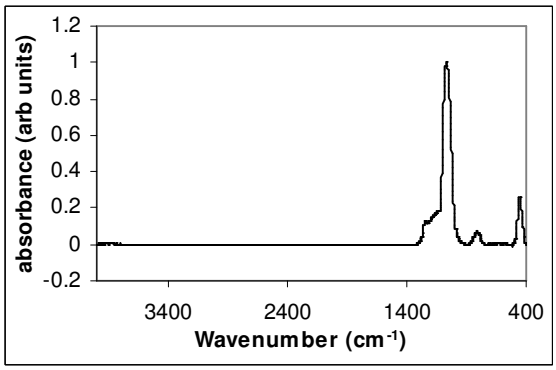

Figure 1: FTIR analysis of TSV liner SiO_2 film deposited at 180 °C

In addition to the liner film within the TSV structure, another area where dielectrics are used is where dielectric isolation is required between different wafers of the multi-wafer stack. In this case, the challenge is in depositing good quality insulating films at low temperature (usually below 180°C) so that the integrity of the adhesive used to bond the thinned device wafer to its glass or silicon carrier is preserved. The isolation stack consists of two types of dielectric films: a copper diffusion barrier and a passivation layer. The former prevents Cu from migrating between adjacent TSVs, and the latter isolates the different wafers in the stack. For each of these applications we have developed films that meet the process temperature requirements (<200 °C) while matching dielectric performance of films deposited at high temperature (400 °C). This is demonstrated in Figure 2, which shows similar I-V performance for low and high temperature PECVD SiO_2 films

In summary, the dielectric liner and back-side low temperature films have been developed with an aim to minimize the overall cost to the TSV stack through optimization of the liner conformality, liner dielectric integrity, back-side film properties and deposition rates.

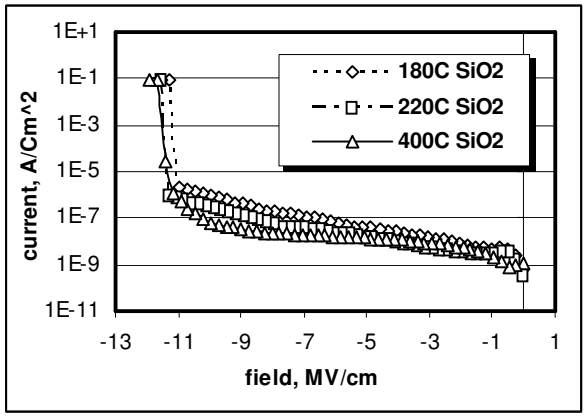

Figure 2: I-V behavior of low temperature and high temperature PECVD SiO_2 films

Barrier / Seed (PVD)

The main challenge for TSV Cu barrier / seed processing is achieving continuous sidewall and bottom coverage in high aspect ratio features with minimum thickness, and ultimately, cost. We recently developed a hollow cathode magnetron (HCM®)-based ion induced copper flow process (IONFLO™) for through-silicon via applications that addresses the technical and high manufacturing cost concerns associated with conventional approaches.

The IONFLO™ process is designed to produce highly conformal copper seed films that are much thinner than conventional seed approaches used for TSV applications, while also delivering excellent sidewall and bottom coverage and enabling a void-free copper fill during the subsequent TSV electroplating step. The process starts with an ion source designed to allow modulation of ion/neutral ratio and reduce ion loss to chamber sidewalls. A magnetic chamber wall then channels charged species only and creates a strong local field, which raises ion density at the wafer level and increases the fraction of sputtered species landing on the feature sidewall. The end result is a more conformal deposition. This highly conformal process eliminates the need for tapered sidewalls of the TSVs and allows the deposited film thickness to be at least 2X thinner than the typical PVD seed layers used for TSV applications. The IONFLO™ process is suitable for a low temperature TSV scheme, as the "ion-induced flow" does not require high-temperature for activation. During deposition, the wafer temperature does not rise above ~100°C.

A typical 60um deep 10:1 AR TSV with vertical sidewalls requires only a 2000Å-thick IONFLO™ copper seed layer for a void free fill, as

compared to a conventional PVD approach that requires an 6000-8000Å-thick seed layer to achieve the same result. This is shown in Figure 3. By significantly reducing seed layer thickness, higher overall tool throughput can be realized, leading to a substantial decrease in cost of consumables.

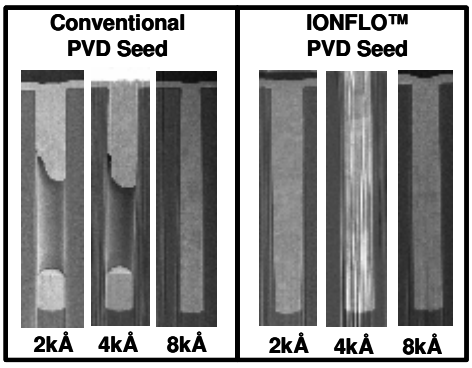

Figure 3: FIB SEM images of 6 X 60 µm TSVs plated using conventional (left) and IONFLO™ (right) seed of varying thickness

After Cu fill, the Cu overburden must be removed from the field surface. The overburden includes both plated and seed material. If the seed portion can be thinned down during deposition, it not only reduces the cost of PVD seed process step, but also the cost and process time of subsequent CMP step. The benefit of this technique enables manufacturability of 3D packaging with TSV.

Balancing integration and manufacturing costs is essential to bringing TSV to production. Barrier / seed processing represents a significant portion of the overall TSV cost. By enabling reduced seed thickness, IONFLO™ technology can provide a direct and immediate cost benefit. The cost benefit of IONFLO™ over conventional PVD is shown in Figure 4.

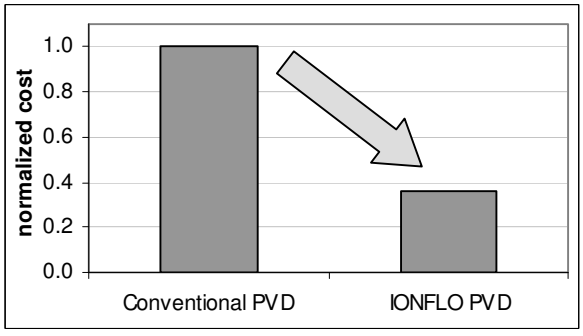

Figure 4: Normalized cost for barrier / seed comparing conventional and IONFLO™ PVD

Cu Fill (Electroplate)

The challenges associated with filling leading edge interconnect structures – down to 2Xnm in size are quite different from those filling micron scale through silicon vias. A complete shift in strategy for process and bath chemistry is required. The development effort initially focused on optimizing the chemistry, plating waveform, and additive set needed for void-free fill. The early TSV aspect ratios were low (5:1 – 10:1) but are now approaching 20:1. Further process / chemistry optimization was required to enable full fill and consistent results across the entire wafer. Void free fill of a 16:1 via is shown in Figure 5.

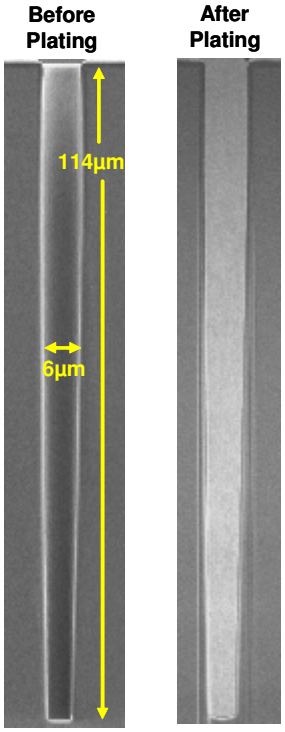

Figure 5: TSV with 16:1 aspect ratio, before and after Cu fill

A major integration challenge for TSV is the management of copper thermal expansion and keeping the Cu mechanically in place after CMP. Differential rates of expansion between Cu and Si can lead to extrusion of the plug above the entrance of the via which can jeopardize subsequent interconnect levels. Through experimentation, we have found that the severity of the extrusion can be modulated by the properties of plated copper and the process by which copper is deposited. We have

determined that the resulting phenomenon of substantial reduction of extrusion is structure-dependent and must be optimized for each aspect ratio and shape.

Reducing cost of processing is always a prime consideration in process development. In the case of electrofill, cost is primarily a function of the length of time it takes to fill large structures. Typical plating rates in copper plating yield process times for 60-100µm TSV structures in the order of tens of minutes. Thus it is critical to provide not only robust fill, but also a process that is as fast as possible in order to minimize the plating cost of ownership.

Another area for cost reduction of the TSV structure formation is CMP. CMP of the copper overburden scales directly with the thickness of that film. If the overburden is thick (several microns) then CMP costs can be very high. Electroplating development has been focused on minimizing the copper overburden to reduce copper CMP costs and eliminate the need for development of new CMP technologies. Driving overburden thickness into the sub-micron range enables the use of established, low-overburden damascene CMP technologies. This minimizes both development and unit process costs.

Development efforts focused on the chemistry and hardware have yielded a plating process which overcomes the key challenges associated with TSV plating. The developed process produces intrinsically robust fill while providing process time and plated film characteristics consistent with the goals of low cost of ownership and seamless integration in the process flow.

Summary / Conclusion

We have discussed here the challenges associated with filling of high aspect ratio TSV structures. For each of the unit processes involved we have demonstrated solution pathways that balance well against keeping cost low. The work presented here is just a snapshot of the current state of technology. We fully intend to continue optimizing unit process performance and integration to improve TSV reliability and drive down overall cost.

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