Spin Coating of Dielectrics on Thin Silicon To Enhance Strength Characteristics

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Abstract

Use of very thin wafers in the semiconductor industry poses handling challenges during manufacturing. The goal of this study was to determine whether applying thin coatings could create stronger, easy to handle wafers. Standard three-point bend testing of coated and uncoated thin wafer samples was used to determine whether the coating strengthened the wafers to improve their handling properties. Data indicated that only the thinnest coating on the thinner silicon increased the peak break strength in three-point bend testing.

Keywords: Thin wafer handling, thin die handling, thin wafer, thin die, handling, wafer stiffening, die stiffening.

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Introduction

Thinner dice and wafers allow great shrinkage in package dimensions and circuit board form-factor but handling of thin silicon or other types of thin wafers is a challenge in the semiconductor manufacturing. As wafer thicknesses drop to 100 micron or below, die and wafer handling without cracking or breaking becomes an issue. Thin wafers can flex and bend inducing micro-cracking throughout the wafer resulting in weak die possibly affecting quality and long term reliability.

By adding a spin-on coating to the wafer prior to backgrinding to final thickness, wafer strength may be increased and flexing, bending and handling issues may be addressed thus allowing the use of thin wafers and thin dice for mainstream electronic products without effecting their quality and reliability.

As wafer strength increases, handling issues are reduced. Three-point bend testing of coated versus uncoated wafer test pieces of various thicknesses can determine flexibility and indicate if coating the wafer actually strengthens it to improve handling properties.

Additionally, if the spin on coating is photo-imageable or is of a type of material that can support other deposition processes, the other side of the wafer or die may be used to contain circuitry or inter-connection structures allowing additional assembly or 3D design techniques to be applied.

In order to handle a thin silicon wafer during processing, it is typically attached to a rigid device or carrier. Adding a stiffener or support aids in handling thin silicon. [e.g., 1-8]

Experimental Details

ASTM D790 three-point bend stress test [9] was used to evaluate silicon wafer samples of two different thicknesses, 100 microns and 50 micron. Strength of non-spin coated wafer samples was compared to coated samples. Different thicknesses of a dielectric material were characterized to study how the coating thickness relates to the strength of the thin samples and determine if spin coating actually improves handling issues of thin wafers and dice.

Eight 6-inch semiconductor grade silicon wafers were used for this experiment.

Three wafers were coated with 5, 15, and 25 microns of the dielectric material and background to a final thickness of 50 microns.

Three wafers were coated at 5, 15, and 25

microns and background to a final thickness of 100 microns.

The remaining two uncoated wafers were background to 50 and 100 microns thick and used as control samples.

The 50 and 100 micron thicknesses were chosen for final wafer thicknesses as they represent thin wafer thicknesses which are harder to handle and more prone to breakage. These two thicknesses cover appreciable range of thin dice in use in the industry.

HD Microsystems 2611 polyimide was selected as a useable stiffening material. It is a dielectric material that can be applied at very thin layers and it has been in use for electronic applications. It is low stress. It has a CTE close to that of silicon. The material is recommended for thicknesses of 20 microns or less. Multiple layers can be applied to achieve greater thickness. In order to reach 25 micron thick target, three layers of this material were used.

Prior to applying the dielectric, the wafers were measured in five locations to check for average flatness with a wafer thickness gage (MTI Proforma 300). Each wafer was measured first in the center followed by four radial points taken around the central point. A piranha bath cleaning followed. An application of VM651 adhesion promoter was carried out just prior to spin coating the dielectric.

Data supplied by manufacturer illustrated what thickness of the polyimide dielectric could be achieved at specific RPMs (Figure 1).

In order to establish a baseline of coating thickness and plot an accurate spin speed curve, four silicon wafers were measured for flatness. Each wafer was coated at set speeds with the dielectric material.

The dielectric was spun at 1500, 2000, 3000, and 3800 RPM. Manufacturer's recommended cure profiles followed to determine how close the manufacturer's spin speed data related to real spin data derived at NDSU/CNSE. This experimental data was used to determine the proper spin speeds for the required 5, 15, and 25 micron coating processes.

Spin coating was followed by a soft bake cure at 110° C for 15 minutes for stabilization of the coating followed by a final cure starting at 200° C for 15 minutes and then ramping to 300° C and holding for 1 hour. For multiple layers to attain desired thicknesses, the soft bake cure was done at 110° C for 30 minutes between each layer.

Baseline spin coating for each thickness was carried out as follows and the resulting thicknesses were recorded:

At 500 RPM for 5 sec followed by 1500 RPM for 30 sec yielded 9.7 micron thick post-cure material thickness.

At 500 RPM for 5 sec followed by 2000 RPM for 30 sec yielded 8.3 micron thick post-cure material thickness.

At 500 RPM for 5 sec followed by 3000 RPM for 30 sec yielded a 5.6 micron thick post cure material thickness.

At 500 RPM for 5 sec followed by 3800 RPM for 30 sec yielded a 4.5 micron thick post-cure material thickness.

A spin speed vs. coating thickness curve was plotted in graphical form as shown in Figure 2.

The coated wafers were diced to produce ASTM required test pieces of standard size of 2″ x 0.5″ to be tested at a span of 1″. ASTM three-point bend stress test was used to evaluate silicon wafer test pieces of the respective thicknesses of 100 microns and 50 microns and bend data was

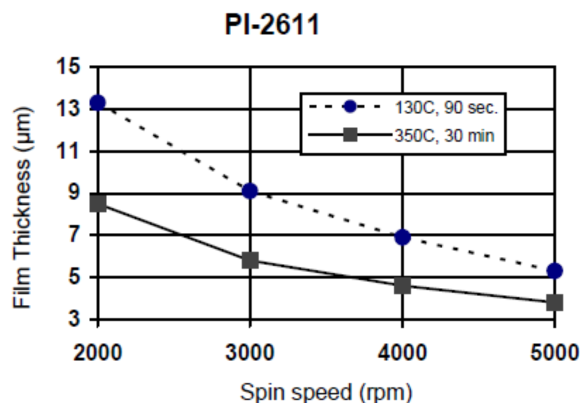

Figure 1. Process guidelines provided by the supplier to achieve target thicknesses.

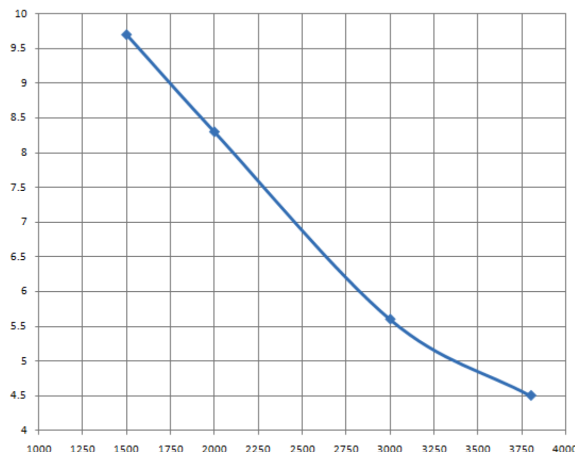

Figure 2. Spin speed in RPM vs. coating thickness in microns as determined through experiments.

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recorded. ASTM three-point bend stress test was also used to test uncoated wafer samples of 50 and 100 micron thick silicon for comparison.

ASTM required test sample size was used. Wafer IDs were noted and all wafers were sent to GDSI (Grinding and Dicing Services, Inc., San Jose CA) for dicing before grinding followed by backgrinding with ‘Disco Polygrind’ as recommended by GDSI for thin silicon for creating stronger test pieces by polishing to a finer grit which leaves less scarring on the wafer. Per the supplier, by polishing to this specification, less deep scarring of the wafer occurs. Scarring by polishing can initiate cracks in the wafer making it fragile and affect the overall flexibility of the wafer.

Results and Discussion

Upon receipt from the supplier after thinning, diced pieces were inspected for damage.

None of the 64 test pieces (4 wafers x 16 pieces/wafer) from the 100 micron thick wafers, with and without coating, were damaged or broken.

Of the 50 micron thick uncoated control test pieces, only 6 out of the 16 test pieces were useable, illustrating how challenging it is to handle, ship and preserve thin silicon through standard machining and shipping processes.

Of the coated 50 micron thick test pieces, 8 test pieces from the 15 micron thick coated wafer came back cracked on the tape. All other 40 test pieces were intact illustrating that coating the wafers may help improve their general handling characteristics.

It was noted that the difference in polyimide thickness had an effect on curvature of the wafers Figure 3). The wafers were coated only on one side. The coating caused bowing according to the coating thickness. The photographs in Figure 4 illustrate the effect of the stress the different thicknesses of polyimide had on the 50 and 100 micron silicon test pieces.

Figure 3: Bending of silicon test pieces due to film stress. Left: 50 micron silicon test pieces. Right: 100 micron silicon test pieces.

In each picture, test pieces with 25 microns of coating are at the top, test pieces with 15 coating are in the middle and the test pieces with 5 micron coating are at the bottom.

It was also noted that the de-taping of all coated test pieces was much easier and resulted in less broken test pieces than either of the uncoated 50 or 100 micron thick test pieces.

Test pieces were demounted from UV dicing tape and were bend tested using the MTS Insight 5EL tensile strength tester (Figure 4).

The parameters used for three-bend testing are listed in Table 1. Ten test pieces from each wafer were bent until broken. Half the coated test pieces were tested with the coating facing the impinging wedge and the other half of the coated test pieces were tested with the coating facing away from the testing wedge.

During the testing of the test pieces from the 50 micron thick silicon wafers, it was noted that 1 inch span was too wide for testing purposes. The flexibility of the 50 micron thick silicon was so high that it did not break until it was actually pinched by the head of the three-point bend tooling. The bend span was decreased to 0.5″ and results were recorded.

The data for the sample set from 50 micron thick wafers coated with 25 micron dielectric film with silicon on top is not listed as the curvature of the test pieces was so extreme that they continued to bend and were pushed through the test apparatus

Figure 4. A bend test in progress.

Table 1. Bend test parameters.

Test Speed	0.8 mm/min
Strain endpoint	0.1 mm/mm
Span	25.4 mm for 100 micron test pieces, 12.7 mm for 50 micron test pieces
Width	12.7 mm
Data Acquisition Rate	10 HZ

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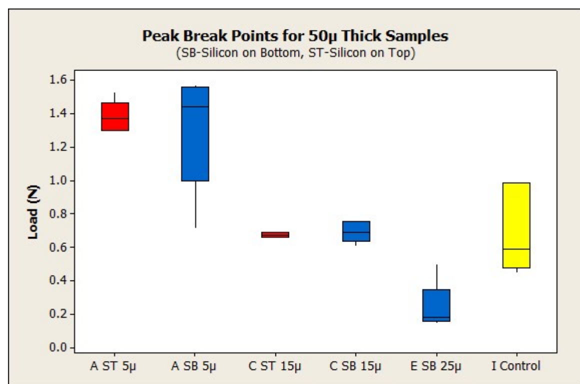

Figure 5. Three-point bend test performance of 50 micron thick test pieces (test span 0.5 in).

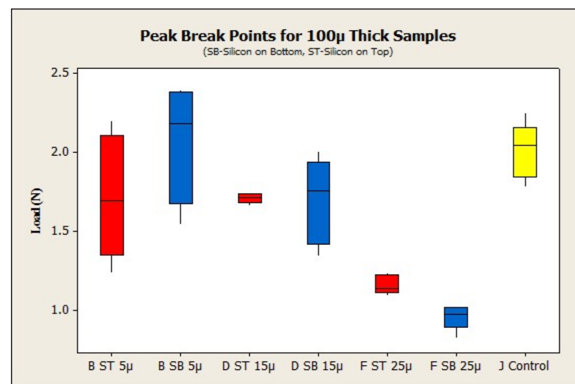

Figure 6. Three-point bend test performance of 100 micron thick test pieces (test span 1 in).

without breaking.

The results of three-point bend testing for the 50 micron thick test pieces are given in Figure 5.

The 100 micron thick test pieces were bent at the 1″ span and results were recorded. The results are summarized in Figure 6.

In Figures 5 and 6, A-J are wafer IDs. SB represents silicon on bottom and ST represents silicon at top.

Bend stress measurements of the 50 micron and 100 micron thick silicon die coated with 5 micron, 15 micron, and 25 micron thick polyimide dielectric illustrate the following results.

1. The 50 micron silicon test pieces with the thinner 5 micron polyimide coating showed higher peak breaking points than the uncoated control test pieces in both silicon side up and silicon side down three-point bend tests.
2. The 50 micron test pieces with the 15 micron polyimide coatings yielded tighter strength distribution but did not show significant strength advantage over the uncoated control test pieces.
3. The 50 micron test pieces with the 25 micron polyimide coatings yielded lower peak breaking points than the uncoated control test pieces.
4. The 50 micron test pieces with the thicker coatings showed increased warping due to the thicker polyimide that could actually be stressing the silicon and weakening it. Not a good choice for applications where silicon needs to be kept flat for adequate functionality.
5. The thinnest coatings (5 micron) showed the greatest peak stress values over the uncoated control test pieces for 50 micron thickness of silicon.
6. Overall handling of the wafer and die was improved by adding the polyimide coating for both wafer thicknesses using the 5 and 15 micron thick polyimide dielectric.
7. Overall handling of the thinner wafer with the thickest coating (25 micron) was not as successful due to extreme curvature of the silicon even though less breakage was noted when handling the wafer and individual test pieces.
8. Individual coated die were noted to be easier to handle and pick up with tweezers and vacuum tools and even by hand without breaking in comparison to the uncoated test pieces.
9. Coated test pieces were also easier to remove from the dicing tape compared to the uncoated test pieces.
10. Overall breakage by handling seemed to be less.
11. Even when the overall bend strength did not increase, the polyimide coating seemed to improve general physical handling properties. More confidence in handling the thin die was noted. Die could also be flexed manually by hand with less chance of breakage.
12. Coated test pieces also did not shatter when broken. The polyimide coating held the silicon together similar to safety glass.

Conclusions

Three coating thicknesses of a particular polyimide dielectric on two wafer thicknesses were studied in this work. It is a significant result that the thinnest coating on the thinner silicon increased the peak break strength in the standard three-point bend testing. The thinnest coating also caused lowest bowing if any compared to thicker coatings thus providing a viable thin wafer strengthening option. This result meets the industry need to produce thin stiff wafers and dice for trouble-free handling during device manufacture.

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It was a general observation during the course of the experiment that coatings improved wafer handling overall and reduced handling damage.

Acknowledgements

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