Wafer-Level hermetic packaging for bio-medical applications

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Introduction

Packaging of medical implants has been always a challenging topic due to the strong requirements in term of sizes, biocompatibility and safety [1, 2].
This is often required for placing an implant at a specific location of the body, without disturbing the surrounding tissues, and aiming at avoiding discomfort for the patient.
The implants should be packaged in order to have a hermetic closed shield around the device, protecting the human body from diffusion of materials from inside the package into the body [3, 4]. Moreover, in order to ensure the functionality of the implanted device, the package should also protect the device from any insertion of body fluids into the implant, especially for active electronics.
An implantable device could consist of several sub-devices connected each other and integrated in a single package. These sub-devices could be one or more CMOS chips, a battery, a sensor, etc. They need to be electrically connected with each other and if required be accessible through the guest body by dedicated electrodes.

We present here a process flow (Figure 1) aiming at encapsulating single dies as commodity Integrated Circuits (IC). The encapsulation consists of a stack of layers, to prevent diffusion of metal contaminant, prior to final encapsulation in a bio-compatible package.
The reported process relies on classical CMOS and 3D wafer-level packaging processes. The test devices for encapsulation consist in test silicon chips with Cu metal structures designed to be characterized in a standard daisy chain configuration. A double diffusion barrier is created on the top side of the chip to avoid Cu diffusion. The first barrier consists on a thick layer of Silicon nitride which offers superior performance with respect to Cu diffusion in the immediate vicinity of the interconnect layers. After this step the wafer is processed with Dicing-Before-Grinding (DBG) technique. A thick silicon oxide is deposited on the sidewalls of the pre-grooved wafers to protect the edge of the IC dies, prior to thinning the wafer down to ~80µm. The sharp edges from the backside of IC dies are then rounded and a 3µm thick oxide deposited at low temperature is deposited to complete the encapsulation. Finally, the test chips are de-bonded and cleaned.

The functionality of the encapsulation process as diffusion barrier is tested by various experiments as cell culture test and leaching test followed by TXRF analysis of the elution. After the hermetic encapsulation of single dies, the next step would be the assembly of the final device. The various sub-devices will be connected through a bio-compatible inter-die metallization (e.g. gold, platinum or other) that will have access to the die's active site by electrodes also them metalized with biocompatible materials (Figure 2a). The total system will be then further encapsulated by using embedding technique where a flexible and biocompatible material [6] will be used to provide the dies a sufficient mechanical support (Figure 2b).

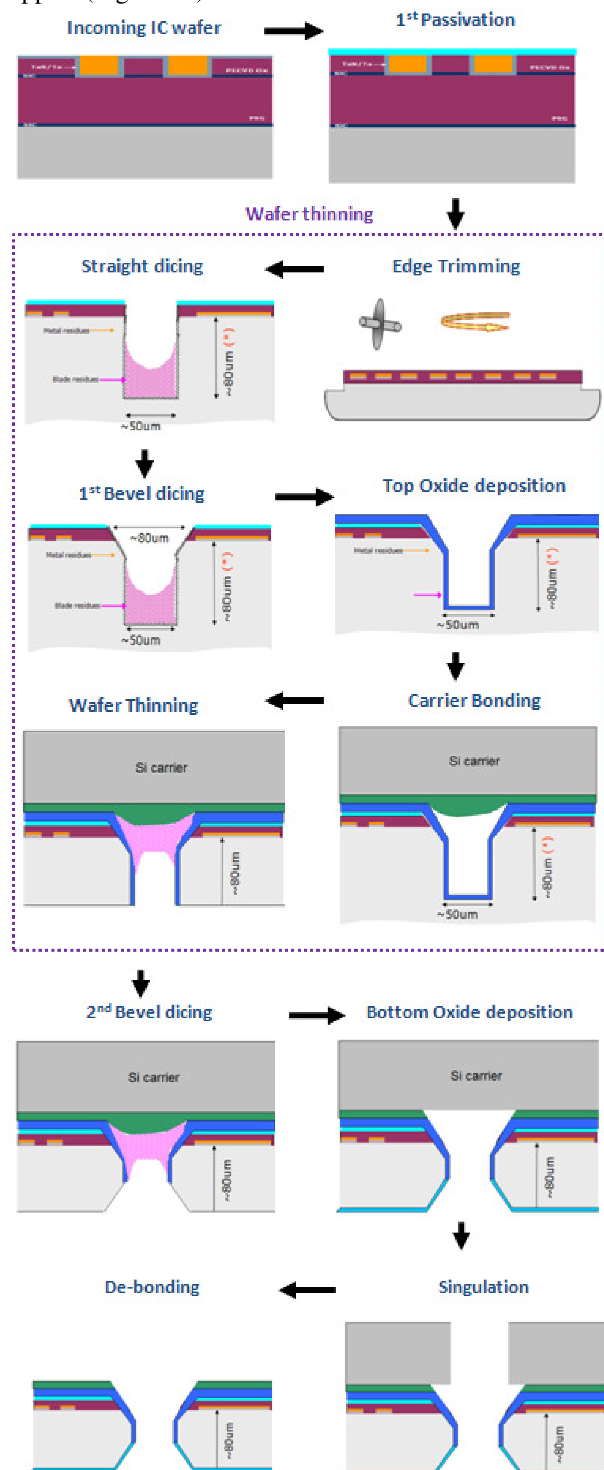

Figure 1: Process flow for wafer-level IC encapsulation and die corners rounding

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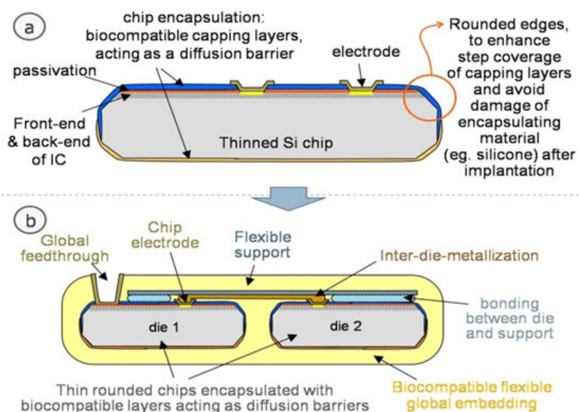


Figure 2: (a) Schematic view of encapsulated chip; (b) possible scheme for a system made by two dies connected by inter-die metallization and embedded in bio-compatible material.

Process flow description

The starting point of the process flow is a silicon wafer where Cu patterns have been realized using a conventional 0.13 µm Cu damascene process. The first encapsulation consists in a standard passivation stack (50nm SiC + 400nm oxide + 550nm Si-nitride) using CVD (Chemical Vapor Deposition) technique.

Depending on the required final thickness for the dies (<100µm), the wafer is processed by thinning including DBG (technique. Before the dicing steps the wafer is processed by edge trimming. This method is used to avoid particle generation during wafer transport after the thinning process. A cross section of the wafer edge is shown on figure 3

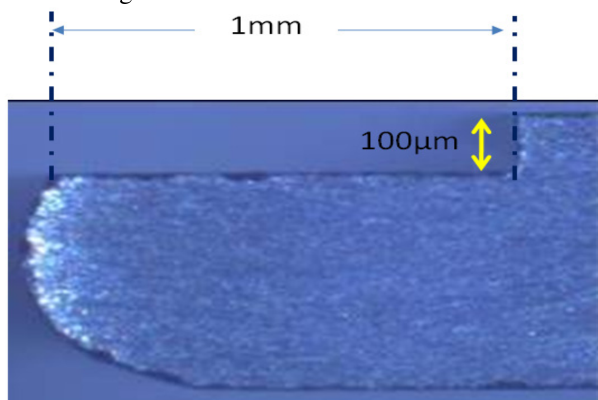


Figure 3: Wafer edge trimming

The DBG processing is done in 2 sequential steps using straight and bevel blades. The straight blade has a nominal width of 25µm, it could dice the wafer up to a depth of 500µm. Considering that target die's final thickness is 80µm, the depth selected for dicing is 100µm. After the straight dicing we have used a bevel blade to create sloped die edges. The bevel blade dicing is controlled by measuring the top width of the dicing grooves (Figure 5-a). This technique is a relative fast and cost effective solution to avoid dies with sharp corners that could result in poor step coverage of the passivation barrier and also introduce risks of cracks in the final embedded global system.

After DBG a second oxide deposition (Top Oxide deposition) is performed to cover chip side walls and at the same time improve the chip encapsulation. This process is optimized using 2 sequential steps of 800nm CVD oxide. A cross –section of the top side of the test chip is shown on Figure 4.

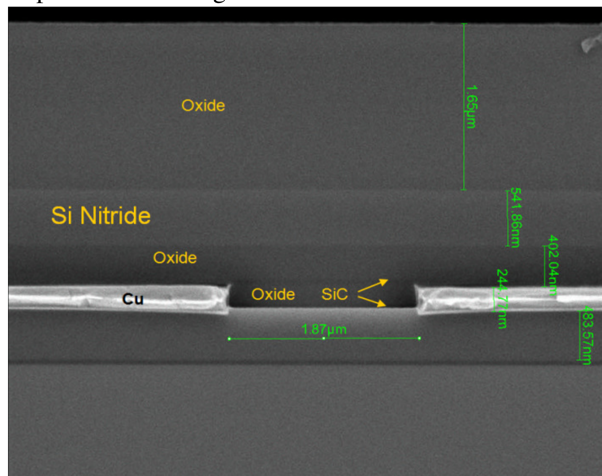
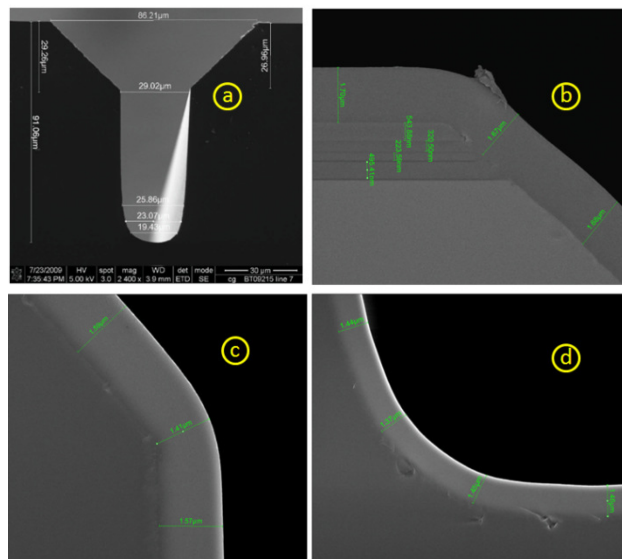


Figure 4: SEM image of processed wafer after Top oxide side (second diffusion barrier). Cu patterns (~250nm thick) are covered by SiC (~50nm), Oxide (400nm), Si nitride (550nm) and a second layer of Oxide (1600nm).



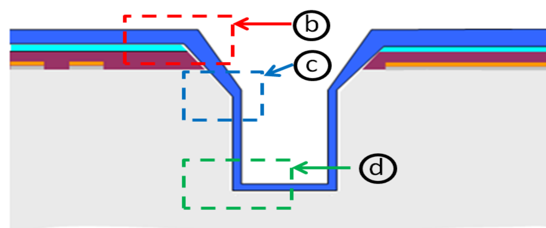


Figure 5: (a) SEM image at dies edges after Top Oxide deposition; (b) Top side of the dicing side wall; (c) Focused image on the intersection of straight-bevel dicing; (d) Bottom of the diced side wall.

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As can be seen on Figure 5, the passivation oxide is fully covering the sides of the dies.

Subsequently, the test wafer is thinned to reach a final thickness of ~80µm. The thinning process is done using another Si wafer as temporary carrier: the metal side of the test wafer is bonded on the carrier by thermoplastic glue and the backside is thinned down to the required thickness using an optimized abrasive grinding. After thinning also the wafer backside is processed with a bevel blade in order to have same sloped die edges as the front side (Figure 6).

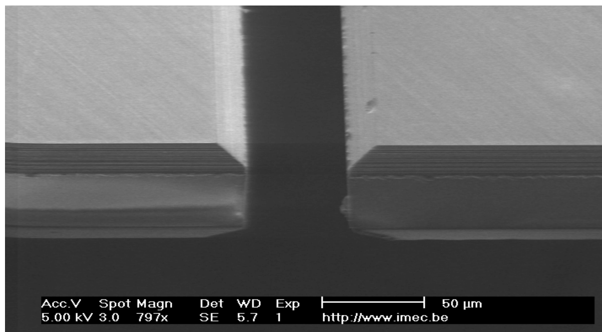

Figure 6: (a) SEM image at dies edges after second bevel dicing (bottom side of the chip is the top in this figure)

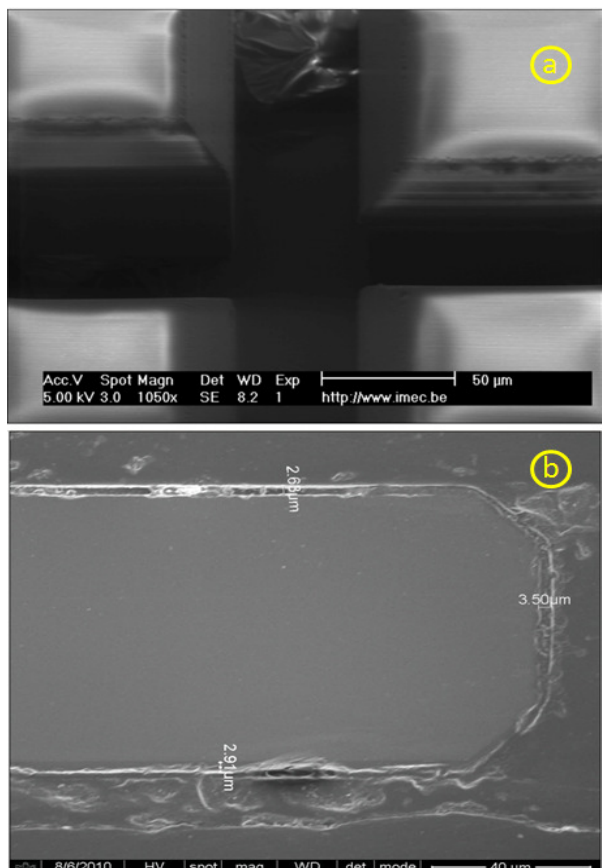

Figure 7: (a) SEM image at dies edges after bottom oxide deposition (bottom side of the chips is the top in this figure; the dies are still on wafer carrier). (b) SEM image of a released die after cross sectioning

To complete the chip encapsulation a new oxide deposition is done on the backside of the wafer. This process is done with the wafer still glued on carrier and to avoid risks of wafer de-bonding due to the glue instability (thermal budget of max 200°) we had to develop a specific process that has enabled us to have a CVD oxide at 170°C.

After the bottom oxide deposition the wafer stack is diced and the dies are finally released from the carrier using the glue solvent.

The result of this dedicated process optimization combined with straight/bevel blade dicing is shown in Figure 7. It is worth noticing that the structure present very good mechanical integrity.

Initial testing of the hermetic encapsulation of individual chips

The functionality as diffusion barrier of the above encapsulation technique could be tested by various experiments such as cell culture tests and leaching tests followed by TXRF analysis of the elution. Several factors like the type of cells used, the elution time, final application, etc. have important effect of the test results and need to be detailed described [5]. In this work, as proof of the obtained diffusion barrier, we refer to only one of the various tests.

The tested dies are selected along the process steps described in Figure 1. Cell culture tests are carried out, using neonatal cardiomyocytes as test cells. In a well plate, culture medium and cells are brought into contact with 3 types of chips: the encapsulated chips as described above (chip A: Cu = 1st passivation + oxide), chips with only passivation on top of Cu (chip B) and chips with Cu patterns only without any cover layer (chip C). The wells have 1, 2 or 4 dies of each type of chip; all chips are 5x5mm wide. After a co-culture of 5 days, a live-dead cell assay is applied and the fluorescent intensity of each well is measured, as is plotted in Fig. 8. Since only cells which are alive are fluorescent, the intensity is a figure of merit for the amount of living cells. Cu is known to be poisonous, which is obvious from the measurements: chip C with naked Cu is causing the death of most of the cells. Chip B with only passivation blocks the Cu diffusion rather well: a much higher intensity is measured proving a lot of cells are alive. Chip A, with the oxide encapsulation on top of the passivation, is improving the diffusion barrier properties even more.

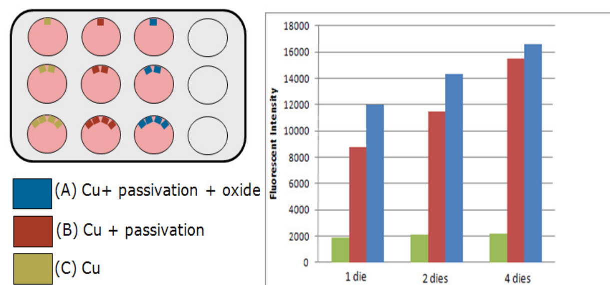

Figure 8: Fluorescent intensity measured over the total well area, for wells containing 1.2 and 4 dies (5mm x5mm die size)

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Conclusions

Based on the requirements for miniaturization and biocompatibility of packages for medical implants, we have developed in a first phase a process flow to obtain a hermetic encapsulation of individual dies using a stack of encapsulation layers. Using a wafer-level processing, the dies are also processed in a way to have sloped edges in order to ease the encapsulation and reduce stress concentration that could results in damages to the IC, the package or the living tissues. As a proof of concept the obtained diffusion barrier properties of this encapsulation is illustrated by cell culture tests.

References

1. Velten, T. *et al*, “Packaging of Bio-MEMS: strategies, technologies, and applications ,” *IEEE Trans. on Adv. Packaging,* Vol. 28, No 4 (2005), pp. 533-546.
2. Lee, Y.C. *et al*, “Packaging for Microelectromechanical and nanoelectromechanical Systems,” *IEEE Trans. on Adv. Packaging,* Vol. 26, No 3 (2003), pp. 217-226.
3. Anderson, J. M., “Biological responses to materials” *Annu. Rev. Mater. Res.*, Vol 23 (2001), pp. 81-110.
4. Anderson, J. M. *et al*, “Monocyte, macrophage and foreign body giant cell interactions with molecularly engineered surfaces,” *J. of Mat. Sci: Mat. in Med.*, Vol. 10 (1999), pp. 579-588
5. Dy E. et al, “Biocompatibility Assessment of Advanced Wafer-level based Chip Encapsulation”, to be published in *Proc. of IEEE ESTC Conference, Berlin* (2010).
6. Brosteaux D. *et al*, “Design and Fabrication of Elastic Interconnections for Stretchable Electronic Circuits”, *IEEE Electron Dev. Lett.* (IEEE-EDL), Vol. 28, No. 7 (2007) pp. 552-554.

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