The Role of Wafer Bonding in 3D Integration and Packaging

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Abstract

There are numerous process integration schemes currently in place for the implementation of 3D-IC. Via first, via middle, via last along with back end of line (BEOL), front end of line (FEOL) and other variations of these approaches. This work will explore the role of wafer bonding, both permanent and temporary, in the fabrication of 3D-IC. Additionally, the materials and process flows used for these processes will be examined in detail.

I. Introduction

3D Integration and Packaging are currently described as "paradigm shifts", "revolutionary technologies", and other equally prophetic catch phrases. The realization of 3D to meet and exceed these expectations requires significant advances in surface preparation methods (CMP – chemical mechanical polishing), development of metal fill technologies (TSV – through silicon via etch, plating, and vapor deposition), redistribution layers, interposer technology, and micro bumping methods, advanced permanent bonding methods, thin wafer handling (materials, carriers, bonding and debonding), as well as simulators (architectural design to cost of ownership modeling). The complexity of 3D integration and packaging blurs the line between process node delineation and requires an overall evaluation and understanding of the entire process flows. All downstream processes are affected by the methods used prior to actual integration processing. Wafer level bonding is a key step, if not the fundamental step, in the success of 3D. If the stacking of the devices is not successful all the previous and subsequent steps are moot.

The ultimate goal of 3D is the flow of electrical signals between layers. This can be at the transistor level between memory layers as in 3D ICs, or it can be at the packaging level between the various heterogeneous devices e.g., logic controller to MEMS device. Permanent wafer bonding methods used in 3D involve metal bonding or hybrid approaches with metal and dielectric layers. The most often used materials are Cu and CuSn for 3D ICs and Au, Al, or Cu based eutectics for hermetic packaging and micro bumping. The process flows, requirements and specification requirements for each bonding technology are based on standard metrology metrics but the requirements for high yields are specific for each technology and will be discussed.

Equally essential to the success of 3D integration and packaging is the ability to retain final stack dimensions that meet the application form factor. For example, it would be unwise to promote vertically stacked devices that resulted in a "chip" that was several millimeters thick when the applications require the devices to fit into smaller and smaller spaces. To facilitate stacking, minimize the vertical interconnect length, and achieve form factor requirements it is common to thin each layer in the stack to 50µm or less. The development and fine tuning of temporary adhesives, the support substrate options, and the quality of the debond and thin wafer transfer robustness are all advancing toward high volume manufacturing options. The leading technology choices for TWH with compatibility tables will be provided to assist in the selection process for various types of device applications.

II. Bonding Sequences for 3D-IC

The nine major 3D-IC process flows are shown in Table 1. In every case, a permanent bonding step is required to form the 3D-IC. Almost all of the bonds are metal to metal and five out of nine of the processes call for temporary bonding to a handle wafer followed by wafer thinning.

TABLE 1. Major 3D-IC Process Flows

Process	IC Wafer	Step #1	Step #2	Step #3
A	FEOL TSV (vias first)	Wafer Thinning (temp. handle)	"face-up" Bond (metal bonding)	
B	FEOL TSV (vias first)	"face-down" Bond (metal bonding)	Wafer Thinning (on 3D stack)	
C	BEOL TSV (vias first)	Wafer Thinning (temp. handle)	"face-up" Bond (metal bonding)	
D	BEOL TSV (vias first)	"face-down" Bond (metal bonding)	Wafer Thinning (on 3D stack)	
E	No TSV	TSV from front (vias first)	"face-down" Bond (metal bonding)	Wafer Thinning (on 3D stack)
F	No TSV	TSV from front (vias first)	Wafer Thinning (temp. handle)	"face-up" Bond (metal bonding)
G	No TSV	"face-down" Bond (all methods)	Wafer Thinning (on 3D stack)	TSV from back (vias last)
H	No TSV	Wafer Thinning (temp. handle)	"face-up" Bond (all methods)	TSV from front (vias last)
I	No TSV	Wafer Thinning (temp. handle)	TSV from back (vias first)	"face-up" Bond (metal bonding)

Figure 1 shows in graphical form the nine major 3D-IC process flows. [1]

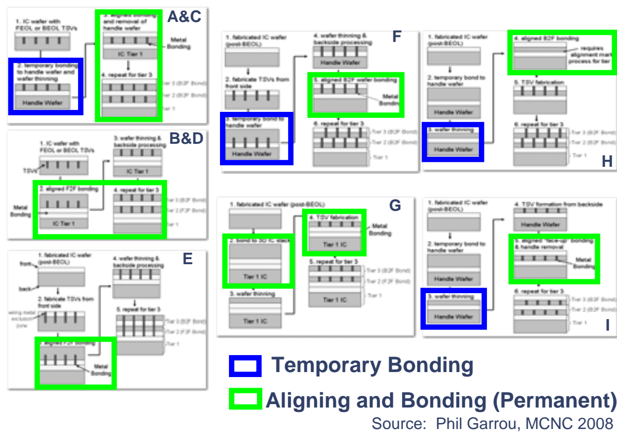

Figure 1. The nine major process sequences for 3D-IC.

III. Primary Metal Schemes Used for Bonding

The selection of metal interconnect between two wafers is often a byproduct of the metals used in the metal wiring of the individual chips. Copper and copper-tin are leading choices due to the wide availability of copper processes in wafer fabs. Copper to copper (Cu-Cu) bonding is a diffusion based process while copper-tin (CuSn-Cu) bonding is a eutectic type. Table 2 shows various metal bonding schemes.

TABLE 2. Comparison of Metal Bonding Schemes

ReactionType	Metal	Bond Temp	CMOS Compatible
Diffusion	Cu-Cu	>350°C	Yes
	Au-Au	>300°C	No
Eutectic	Al-Ge	>419°C	Yes
	AuSi	>363°C	No
	AuGe	>361°C	No
	AuSn	>278°C	No
	CuSn	>231°C	Yes

Diffusion bonding has stringent surface roughness and flatness requirements. It is known that for diffusion bonding, the contact area and bonding energy must be as large as possible. It is therefore important for the two mating metal surfaces to be very smooth and flat to allow for solid state diffusion. The surface roughness of the substrate in addition to its activation state defines the temperature and the force required for good bonding. It has been demonstrated that the surface roughness affects the bonding quality when the bonding temperature is low. The typical reported micro-roughness values of sputtered Cu on (300nm) on Ta (100nm) range from 1.5 to 2nm. Low temperature bonding processes (<300°C) for Cu-Cu bonding have been demonstrated by controlling copper surface roughness (using optimized CMP processes) and oxidation. Figure 2 shows Cu-Cu bond interface note the lack of surface roughness across the interface. Figure 3 shows the grain boundaries and structure of the Cu which is found inside a via.

The requirements for a copper surface which will be the basis for plating are very different compared to a copper surface which will be the basis for bonding. Plated copper may be readily available for bonding processes but it can be challenging to work with given the sensitivity of Cu to surface contaminants such as carbon and copper oxides combined with their abundance during normal processing. Work reported by Dr. Tan, et al [2] and T. Kim, et al [3] show the importance of surface cleanliness on bond temperature and quality. Cu-Cu bonding can be achieved relatively easily with excellent interface

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diffusion at temperatures as low as 200°C using a self-assembled monolayer approach or at room temperature after ion sputter cleaning.

For Cu eutectic wafer bonding, the surface micro-roughness is not as important. There is significant industry experience from solder joint studies relating to chip packaging that indicates this bond approach is also less sensitive to surface contamination[4]. The lower processing temperature also makes it friendlier for wafer processing thermal budgets.

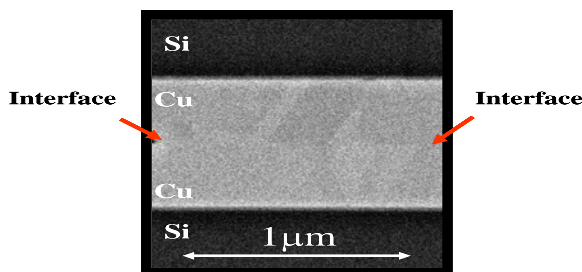

Fig. 2. Cu-Cu bond interface showing grain boundary.

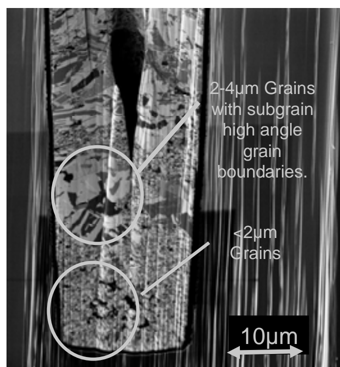

Fig. 3. Copper via illustrating grain size and morphology within the via. Oxide liner and seed layer not visible.

IV. Key Temporary Adhesive Specifications

The major requirements of temporary adhesives are related to its process flow, thermal stability, chemical resistance, and mechanical strength. The desired properties have changed in one significant area – debonding process flow. Debonding is where the device wafer is separated from the carrier after significant value has been added to the device wafer through wafer thinning, via processing, insulator, barrier and metal deposition, patterning, and so on. The thin wafer is normally under internal stress at this point which would cause it to warp or even roll up and crumble if it were not secured in a fixed position. The situation is further compounded as the wafer size increases to 300mm, while the wafer thickness is reduced below 85μm.

Additionally, at the present time industry focus is to output the thinned device wafer onto a tape frame. Consequently, processes that debond the thinned wafer after it is mounted to a tape frame by their nature allow the highest potential debond yield due to the fact that the wafer is always firmly supported. [5]. In SUSS' experience, the robustness of debonding after tape mounting allows the thinnest wafers to be successfully processed compared to methods employing thermal-slide or solvent debonding. Therefore, our focus will be on processes that allow debonding after frame mounting.

The major requirements of temporary adhesives in order of priority are related to its process flow, thermal stability, chemical resistance, and mechanical strength. TABLE 3 provides an overview of desired material and process properties.

TABLE 3
Desired Properties of Adhesive and Carrier

Adhesive and Process Properties:
Debond while on dicing frame
Bond Temperature <200C
Stable up to 400C, no delamination, voids
No handling of thinned wafers
No damage during debond
Simple, low CoO process

Carrier Properties:
Material: non-contaminating, Si or glass
Ability to align through the carrier/adhesive
Diameter relative to Si wafer: 0 to +1.0mm
Recycle 50x minimum
Low cost
TTV similar to Si or quality glass
One carrier through entire process (no need to swap carriers)
Wafer edge must be supported

V. Thermal Stability

Thermal stability of temporary adhesives has been a major concern as defects have been reported to occur after high temperature processing [6]. Thermal stability of temporary adhesives relates to the ability of the material to resist decomposition and outgassing during exposure to high process temperatures over periods of time. Common modes of adhesive failure after exposure to high temperatures and high vacuum conditions are the

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complete delamination of the thinned wafer from the carrier; areas where pockets of the thinned wafer delaminate in the form of centimeter sized bubbles, see figure 4; and "flowers" where the thinned wafer exhibits millimeter sized flower shaped defects [7]. Thermal performance measurements should predict the formation of these defects.

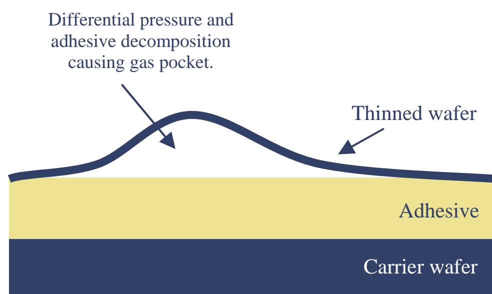

Figure 4. Adhesive decomposition and adhesive vapor pressure during high temperature, high vacuum processing leading to gas pocket.

Thermo-gravimetric analysis (TGA) is a simple tool useful for comparing different adhesives. TGA can be used to narrow the selection of an adhesive but it does not reveal the materials that evolve during thermal processing. Thermal desorption spectroscopy (TDS) or thermal extraction with mass spectrometer (TEDGCMass) can provide detailed information relating to the relative quantity and types of compounds evolved during thermal processing. This information can be useful for even more detailed comparison of adhesives as well as predicting the potential impact on the process equipment exposed to these compounds, for example, cleaning frequency. However, these measurements should be interpreted carefully as they do not represent the actual use of the polymer where it is sandwiched between two wafers.

VI. Adhesive Systems

There are three main thin wafer handling adhesive systems which allow debonding after tape frame mounting: 3M™ Wafer Support System adhesive system [8], Thin Materials AG adhesive system (T-MAT) [9], and Brewer Science Inc.'s ZoneBOND system [10]. As a point of reference, one thermal-slide process will be shown [11].

A. Brewer Science, Inc. WaferBOND HT10.10

Brewer's material uses an adhesive cast in solvent which is spin coated and baked much like photoresist. Bonding is done in a vacuum chamber at moderate force (<8kN) and at ~200°C. Debonding is conducted using a thermal-slide process where the wafer stack (carrier, adhesive and thinned wafer) is heated and the thinned wafer is slid off the carrier wafer. The thinned wafer must then be cleaned using a solvent to remove the residue of the adhesive, figure 5.

It is important to note that this type of processing requires another carrier or secondary carrier to support the thinned wafer during debonding, for example an electrostatic chuck, Gelpak-type material, or vacuum chuck. As a result, the process is more complex and expensive while placing the expensive thinned wafer at risk of breakage from the added handling.

This type of process has been used for over twenty years. The main appeal of this process is due to the simplicity of the bond process and the widely available equipment for bonding.

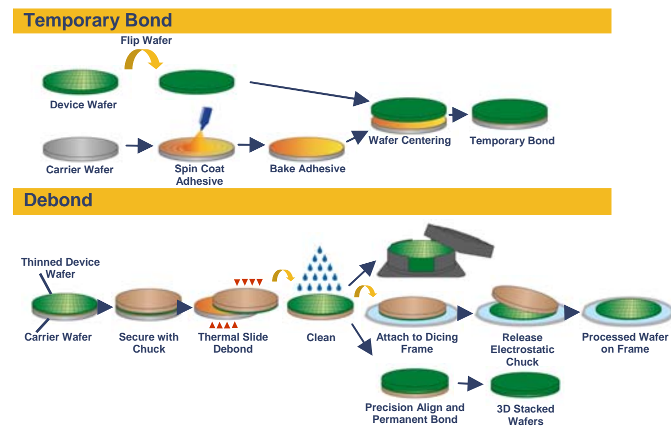

Figure 5. Typical process for Brewer HT10.10 and other thermal-slide adhesives.

B. 3M Wafer Support System

3M's material system uses a room temperature UV curable adhesive coated on the CMOS wafer and joined to a laser absorbing adhesive layer coated on a glass wafer carrier. The laser absorbing material is known as Light To Heat Conversion (LTHC) material. Debonding can occur after the wafer stack is attached to a tape frame with the thinned wafer attached to the tape. A laser then irradiates the stack through the glass side allowing easy removal of the glass carrier. The thinned wafer remains constantly supported by and attached to the tape/frame. The adhesive remaining on the thinned CMOS wafer is removed by a peeling process using detaping tape. 3M's adhesive does not require cleaning after debonding. The overall process is shown in figure 6.

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The key characteristics of the 3M process include room temperature debonding and debonding after frame mounting.

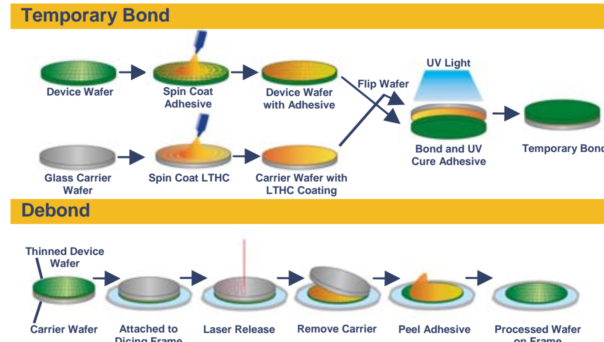

Figure 6. 3M WSS process flow.

C. Thin Materials AG (T-MAT)

T-MAT's process uses a precursor spun on to the CMOS wafer. This is then converted via a simple PE-CVD process to form a release layer ~100 – 150nm thick. The elastomer used is a high temperature material cured at ~180°C which joins the wafer to the carrier. Debonding can occur after the wafer stack is attached to a tape frame with the thinned wafer attached to the tape. One vacuum chuck is used to hold the thinned wafer via the taped side while another holds the carrier. Upon slight separation of the stack at one side, a debond wave moves across the stack separating the wafers and leaving behind the thinned wafer supported by the tape/frame. The process is shown in figure 7.

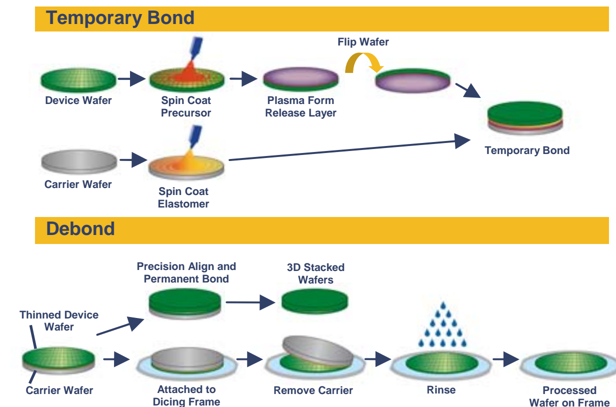

Figure 7. Typical T-MAT process flow.

B. Brewer Science Inc., ZoneBOND

ZoneBOND uses a specially prepared carrier with two distinct zones as shown in Figure 8. The edge zone consists of a normal silicon wafer while the center zone exhibits low adhesion properties. The carrier is then bonded to the device wafers using heat and force.

Debonding is a multiple step process whereby the first step removes the adhesive joining the wafer and carrier at the edge. The second step is a mechanical wedge separation of the carrier from the wafer by a means very similar to TMAT. The final step is the removal of the adhesive from the face of the device wafer.

The key characteristics of BSI's ZoneBOND process include room temperature debonding and debonding after frame mounting.

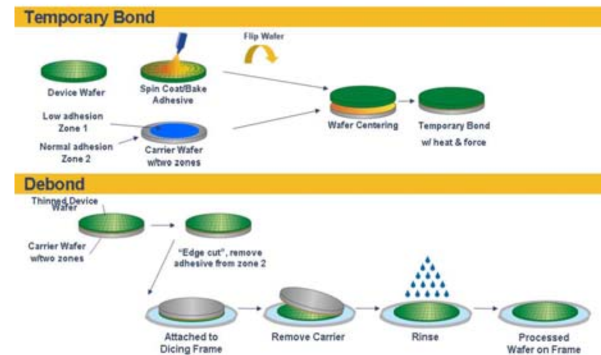

Figure 8. Typical process for BSI ZoneBOND

VII. Mechanical Properties

Again, five of the nine 3D-IC process flows call for the transfer of the thinned wafer supported by the carrier to another wafer using permanent bonding. Mechanical hardness of the temporary adhesive must hold the thinned wafer flat to the carrier during high temperature processing. If the adhesive gives during the bond process, the thin wafer will flex under pressure from the bonding points as shown in Figures 9a and 9b. If these process flows are expected to be utilized then thermo-mechanical analysis testing should be conducted to ensure suitable hardness during the process conditions.

Delamination of the wafer from the carrier is not normally an issue for these processes. In fact, it is desired for the thin device wafer to delaminate or debond from the carrier while it is bonded to another wafer. In this case, the process might be considered a layer transfer. In the case of TMAT's adhesive system, this has been demonstrated and will likely

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work as well with other silicone based adhesive systems. More often the adhesive will change under the heat and pressure of the permanent bond process and not allow debonding later or the adhesive will become too difficult to remove by normal means.

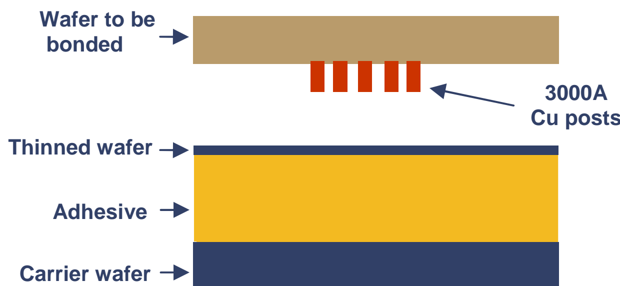

Figure 9a. Wafers before bonding.

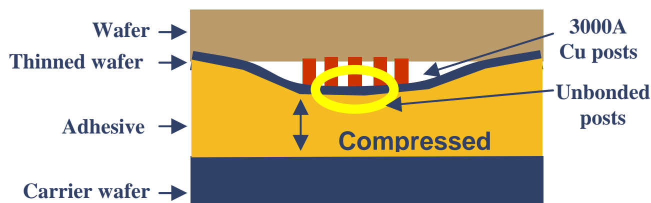

Figure 9b. Thin wafer after bonding showing deformation due to lack of support from adhesive at high temperatures.

VIII. Summary and Conclusions

Wafer bonding has an important role in 3D-IC applications. Wafer bonding, permanent or temporary, is an essential requirement and the only viable means to achieve cost effective chips. Permanent bonding is used in all process flows while temporary bonding is also used in over half of the process flows.

Copper based processes dominate for permanent bonding as copper is readily available in wafer fabs globally. However, copper bonding is susceptible to defects and degradation caused by surface contamination from oxides and organics. Eliminating and controlling these impurities is imperative for 3D-IC Cu bonding processes.

The leading temporary bonding adhesives use a process flow that allows debonding after mounting to a tape frame. The taught tape on the frame provides a necessary and sound surface for supporting the thinned wafer. Traditional thermal-slide and solvent debond processes do not allow debonding after mounting to a tape frame limiting debond yield and minimum wafer thickness.

The desired properties for temporary adhesives are extremely challenging. An approach to quantify thermal performance of temporary adhesives at high temperatures using TGA and TDS data has been presented. The approach provides a good predictor of the complex processes that occur at high temperatures.

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