Processing aspects to achieve high-end hybrid backside illuminated imagers

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Abstract

We present a successful integration scheme of a backside illuminated 1024x1024 pixel sensor array, flip chipped on top of a ROIC with 10µm diameter Indium micro bumps, where the pixel pitch is 22.5µm. Backside illumination results, as compared to front side illumination, in a large gain in quantum efficiency because no incoming light is lost in the metal and dielectric layers. At the other side however, backside illuminated imagers requires more complex post processing because the detector array has to be thinned down to 30µm or less. Surface treatment reduces surface combination and lead to an improvement of the quantum efficiency of the device. Any damage induced at the backside of the imager is detrimental for the quantum efficiency since defects act as recombination centers for the light generated electron-hole pairs. In the end, all process optimizations on the hybrid backside illuminated imager device lead towards a quantum efficiency of 80-90% (over the visible spectrum). Next to the discussion on the critical steps (such as wafer thinning on carrier, wafer flip, cleaning), we introduce a novel backside alignment strategy to avoid using pyrex substrate as temporary carrier for thinning. Pyrex is namely not compatible in a high-end Si process environment due to its fragile nature. It is also shown that through introduction of a high aspect ratio pixel separating trenches, inter pixel electrical crosstalk can be avoided. Finally an alternative micro bump formation by means of CuSn bumps is presented.

Keywords: backside illuminated imager, high broadband quantum efficiency, thinned imager, high aspect ratio trenches for low electrical crosstalk, Indium bumps, CuSn bumps

Introduction

Backside (BS) illuminated CMOS imagers, as compared to front side (FS) illuminated imagers, results in a large gain in quantum efficiency (QE) since no incoming light is lost due to reflections on the metal interconnects, leading to a 100% fill factor. Also anti-reflective coatings (ARC) on the Si BS can be optimized independently of the back-end structure on the FS, thus maximizing the light coupling to the substrate. As a result BS illuminated imagers can have a wider spectral response than FS illuminated imagers. On the other hand however, BS illuminated imagers require more complex post processing because the detector array has to be thinned down to 30µm or less. When choosing for BS illumination, quantum efficiency is intrinsic the same for monolithic and hybrid imagers.

For hybrid imagers, by splitting up the processing of the detector array and the read-out IC (ROIC), each part can be separately optimized to the needs of the application. As such special substrates or epi layers can be chosen, pixel separating trenches can be added for crosstalk reduction, etc. This additional degree of freedom has the advantage to produce photodiodes which are not available as standard for monolithic imagers fabricated in commercial foundries. The hybrid approach on the other hand is more costly but the ROIC does not have to withstand all the post CMOS processing like for monolithic imagers.

In this paper the process integration of a hybrid backside illuminated 1024x1024 pixel imager is presented. The sensor array, thinned to 30µm, is flip chipped on top of a ROIC with 10µm diameter Indium micro bumps, where the pixel pitch is 22.5µm. The detector IC was produced at imec and the ROIC at a commercial foundry, both in a 0.35µm technology. Also the route towards CuSn bumps is assessed in a feasibility study.

Processing aspects versus imager performance

In this section the processing scheme is discussed together with its impact on the imager performance.

Starting from 200mm p-type wafers, a 30µm graded epi-layer was grown to introduce a built-in electrical field to pull generated carriers from the non-depleted substrate [1,2].

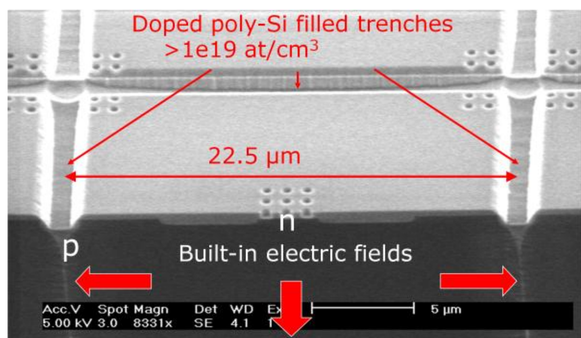

Figure 1: Tilted SEM cross section view of a detector pixel after W contact plug formation. The filled deep trenches for cross-talk reduction are clearly visible and introduces a lateral built-in electrical field. The vertical electrical field is formed by the graded epi-layer.

To reduce cross-talk, pixel separating trenches are foreseen. These high aspect ratio (1.2µm wide, 32µm deep) trenches are etched before all front-end steps, using an oxide hard mask based Bosch DRIE process (alternating steps of SF_6 etching and C_4F_8 passivation). Conditioning of the sidewall of the deep trench after etch is very crucial. Without special treatment, the quantum efficiency of the imager can drop by 10%, due to carrier recombination at the trench sidewalls [3]. After highly Boron doped poly-Si filling, planarization by means of chemical mechanical polishing and oxide hard mask removal finalizes the trench definition. The deep trenches filled with poly-Si provide a lateral drift field (Figure 1) which counteracts minority carrier diffusion between pixels and thus blocks inter-pixel diffusion, thereby substantially reducing electrical crosstalk. The last can be defined as the ratio of the output signal of neighbouring pixels to the output signal of the central pixel when illuminating only the centre pixel. For the non-trenched imager, a large part of the signal is captured by the neighboring pixels [4] (Figure 2).

After trench definition, all following front end and backend steps run in a standard 0.35µm technology. Only the implantation conditions are dedicated for the diodes.

Post-processing starts with trimming of the edge of the wafer by dicing. As explained in Figure 3, edge conditioning of the wafer before thinning will avoid chipping of the edge after thinning.

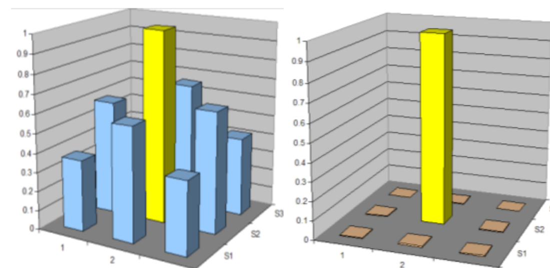

Figure 2: Cross-talk measurement for a non-trenched (left) and a trenched detector (right) array using single pixel illumination [4].

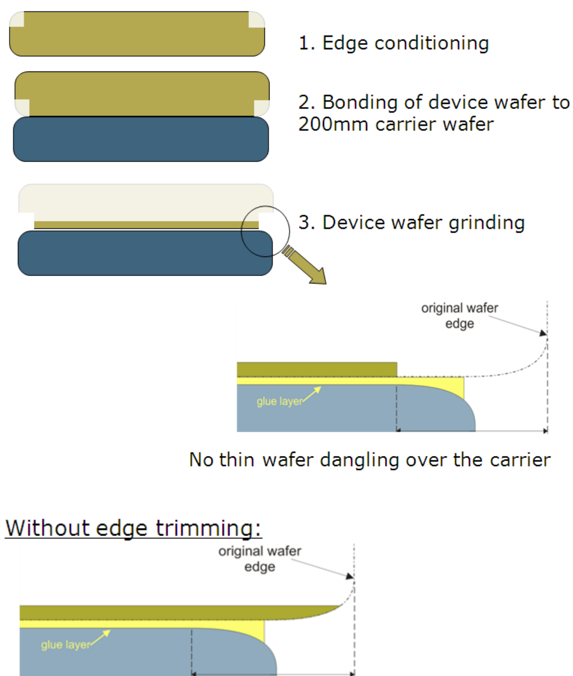

Figure 3: Edge conditioning. Without edge trimming wafer to carrier misalignment can lead to overhanging of sharp wafer edge which is sensitive to chipping.

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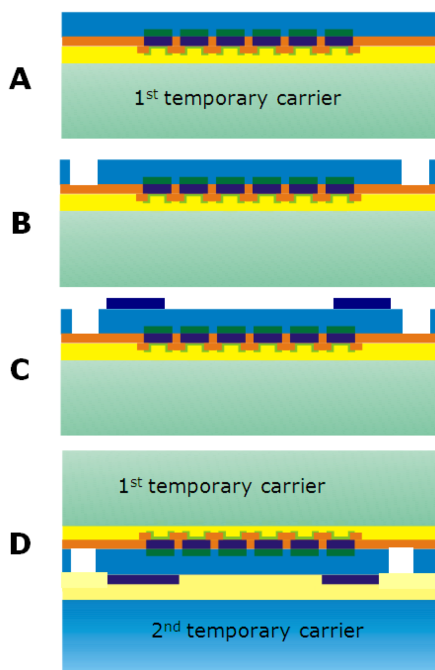

Figure 4: Post-processing of the detector array

A: Bonding to 1st temporary Si carrier + thinning to 30µm + post grinding clean

B: DRIE of large cavities to open front side alignment marks + DRIE new backside alignment marks next to cavities + implantation + laser annealing

C: Aluminum light shield patterning, aligned to the new marks

D: Bonding to 2nd temporary Si carrier

After edge trimming, the device wafer is bonded face down on a temporary carrier by means of a temporary glue (Quickstick 135). In order to align the Aluminum (Al) light shield on the backside of the thinned wafer to the diode array on the front side (Figure 4C), normally a (CTE matched) glass temporary carrier is used. Glass is however not compatible with high-end Si process environment due to its fragile, non-conductive and (Na) contaminating nature. Therefore, a novel backside alignment strategy is introduced, avoiding glass as temporary carrier for thinning. In this novel strategy the device wafer is bonded to a Si carrier. After thinning by grinding down to 30µm (Figure 4A), large cavities are etched through the thinned Si on the position of the front side alignment marks (Figure 4B). Then these exposed marks are transferred to the silicon backside next to the cavities by DRIE (to introduce topography). The new alignment marks are used to align the Al metal shield (Figure 4C). By using this method, misalignment of the Al backside light shield to front side metal layer is limited to 5µm, which is far below the allowed 22.5µm (i.e. 1 pixel pitch) misalignment.

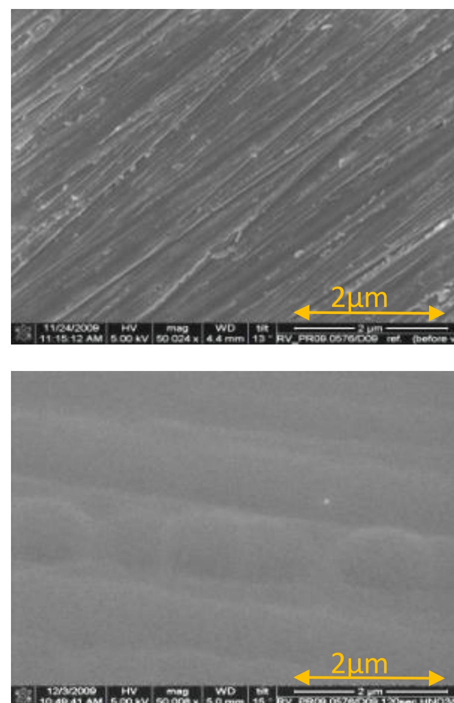

Figure 5: Smoothening of the ground surface using an optimized HF/HNO_3 wet etch.

Special attention is given to conditioning the backside Si surface after grinding. As shown in Figure 5, an optimized HF/HNO_3 wet etch process smoothens the rough ground surface. This smooth surface, in combination with shallow implantation and laser annealing, is very important to keep the QE high [2]. Any damage induced at the backside of the imager is detrimental for the QE since defects act as recombination centers for the light generated electron-hole pairs. Shallow implantation followed by laser anneal introduces an electrical field which is shielding generated carriers from the recombination centers at the backside surface.

After defining the Al light shield (Figure 4D), the wafer is bonded to a 2nd temporary Si carrier using a 2nd glue, followed by debonding of the 1st carrier. Next to this waferflip operation (Figure 7E),

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Au-based under bump metallization together with Indium bumps are formed by lift-off. In Figure 6 the resist pattern for 10µm bumps, 10µm spacing is shown, together with the defined bumps after lift-off. Further the detector arrays are diced on carrier and flip-chipped on to the ROIC dies. The second carrier is removed followed by a thorough cleaning of the detector surface. This step is crucial to ensure low photon response non-uniformity. The processing is finalized after mounting the hybrid imager on a PCB through wire bonding and ARC deposition (Figure 7G).

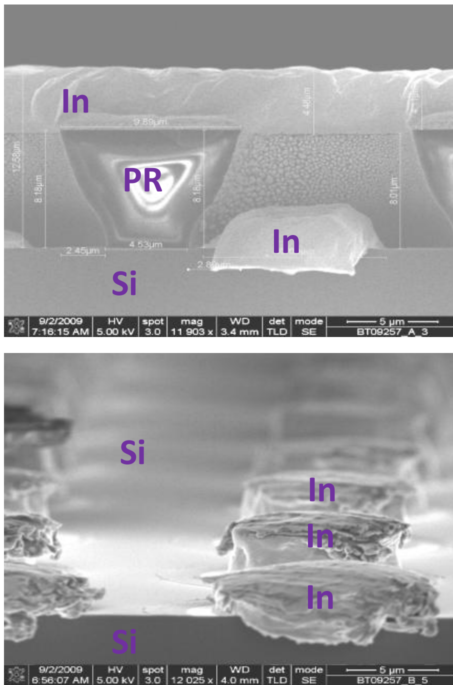

Figure 6: (Top) Patterning for lift-off definition of Au/In bumps. For lift-off a negative resist profile is desired. (Bottom) 10µm diameter bumps defined after lift-off (10µm spacing) Due to its soft nature, indium was smeared out over the wafer edge during sample preparation.

All backside surface optimizations (post-grinding clean, implantation and laser annealing) and an optimized ZnS/MgF_2 ARC [2] lead towards an excellent quantum efficiency (QE) on the 1024x1024 imager. In the wavelength range of 400-850nm a QE above 80% was measured (Figure 8). The measurements are amongst the highest broadband QE's reported for CMOS imagers [1] and CCD camera's [5]. Next to this, a 99.93% high bump yield and low diode dark currents of 300pA/cm^2 @ 25˚C were obtained.

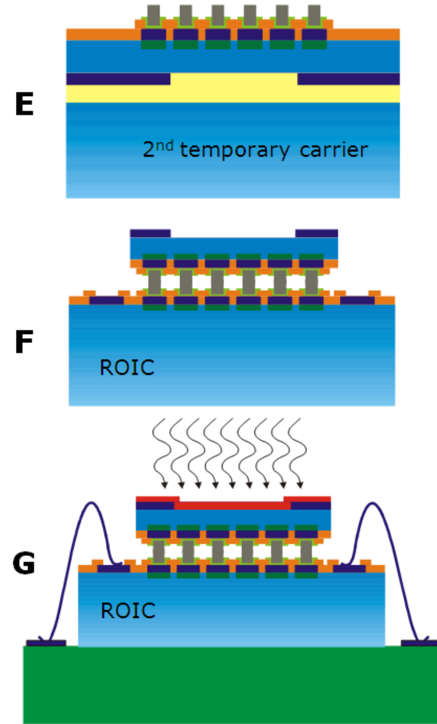

Figure 7: Post-processing of the detector array

E: Waferflip - Debonding of 1st temporary Si carrier + Indium bump definition

F: Dicing of detector array on carrier + flip chip assembly on the ROIC + debonding of 2nd temporary Si carrier

G: Mounting on PCB + wire bonding + ARC deposition

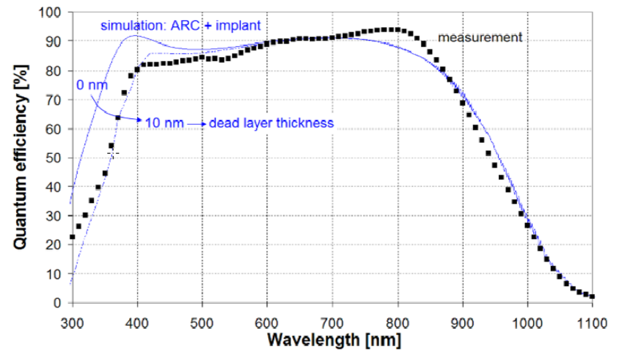

Figure 8: Excellent broadband QE was measured. The results are in agreement with simulations [2].

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Alternative micro bumping by means of CuSn

In previous section, excellent results were shown using Indium bump interconnections. Next to this we report on the feasibility of using electroplated CuSn bumps to assemble the detector die to the ROIC. A transient liquid phase CuSn bonding [6] enables the ability of stacking more than 2 dies with even more flexibility for future hybrid imagers.

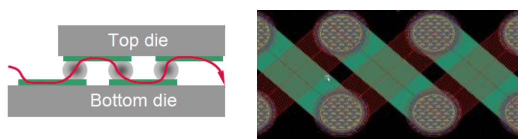

Figure 9: Interwoven daisy chain structures for bump yield measurements: top (right) and cross-section view (left).

Daisy chain structures were used in order to evaluate and optimize bump yield, prior to the assembly of hybrid imagers. In a detector array each unconnected bump will show up in the image as a black dot. Therefore investigation of the interconnection yield is critical. As typically the imager bump yield is very high, lots of interconnects need to be evaluated to detect any failures at all. Therefore this is done by using daisy chains, a series connection of bumps between top and bottom die (Figure 9). In this section, we only discuss very long daisy chains of 1750 bumps. On 44 positions of the die, 5 double interwoven daisy chains (see Figure 9 right) were measured. The bumps are 10µm in diameter with a 20µm pitch. In total, the 2cm x 2cm large dies consist of about 1M number of bumps.

In Figure 10, a top down SEM is shown of the top die using CuSn electroplated bumps. The bottom die looks similar but has Cu bumps and measurements pads.

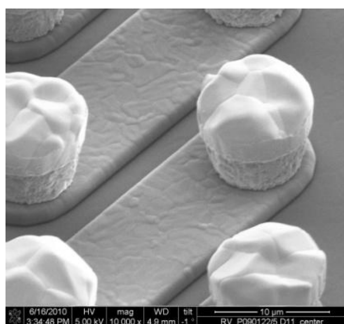

Figure 10: SEM picture of the top die: upper part of the interwoven daisy chain with 10um diameter CuSn bumps formed by electrochemical plating. The pitch of the bumps is 20µm. The die consists of 1M bumps.

In Figure 11, daisy chain measurements of an assembled die with CuSn bumps are shown. Next to the chain resistance itself (blue bars), interchain measurements were performed to trace back shorts (red bars). The blue bars indicate that the average chain resistance is about 300Ω and that some chains are open (missing bump(s)). At the other hand, no visible shorts between the interwoven chains are observed (red bars). To ease interpretation, the bar chart of Figure 11 was transformed to the one of Figure 12, where functional, open and short chains are shown, both for CuSn as for In bumps. 84% of the CuSn daisy chains are functional, while only 12% for the Indium case. Missing bumps are causing non-functional daisy chains for CuSn, while shorted bumps are the main failure for the In part. Missing or non connected bumps however cannot be neglected.

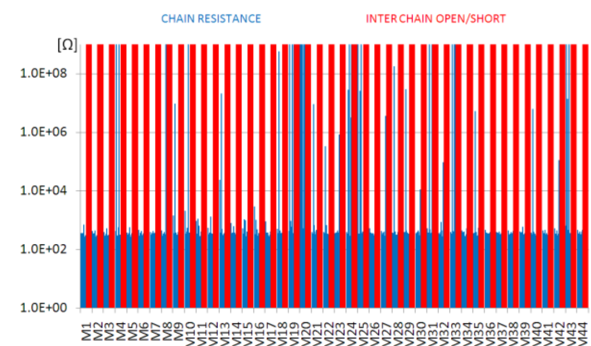

Figure 11: Interwoven CuSnCu bumped daisy chains (1750 bumps): chain resistance and open/short measurements versus die position (10 daisy chains per position, M1=left side die, M44=right side die).

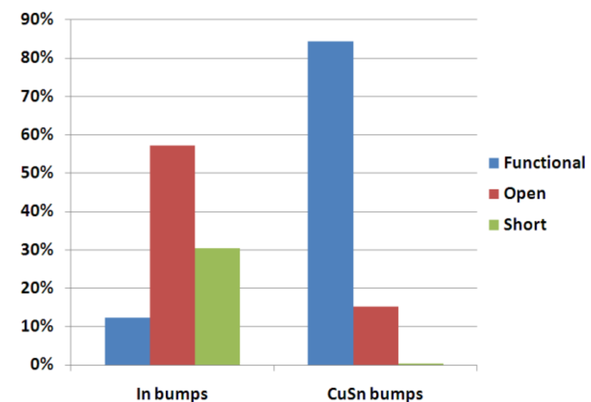

Figure 12: Daisy chain bump yield comparing Indium versus CuSn bumps.

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Indium is soft by its nature and smears out easily which can partly explain the higher fall-out of the daisy chains due to shorts. Opens are caused by missing bumps what might be originating in the lift-off definition by ultrasonic agitation. The daisy chain structures are very sensitive to this kind of failures as they were designed for high bump yield. It should be however noted that this daisy chain yield is not a direct measure for the bump yield. Daisy chain yield always will be smaller than bump yield. This bump yield can be derived by calculation from the daisy chain yield [5]. The average daisy chain yield of 84% for the CuSn assemblies translates into a bump yield higher than 99.99% (< 100 faulty bumps per 1.000.000). This is an excellent result. Even for the In bumped assemblies with an average daisy chain yield of 12%, a bump yield of 99.87% is obtained (close to the 99.93% measured on the imagers). This is indicative for the sensitivity of the daisy chain mask design, which is tuned for high bump yield numbers.

Considering these results we can conclude that for most applications CuSn microbumps are a good alternative to Indium bumps. However for advanced applications like space, more aspects need to be investigated (i.e. whisker formation, cyrogenic temperature, outgassing (of the flux), mechanical reliability under vibrations, etc ...) but this lies beyond the topic of this paper.

Acknowledgement

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Conclusion

A successful processing scheme of a hybrid backside illuminated 1024x1024 imager with a pixel pitch of 22.5µm is presented. All process optimizations that are implemented lead towards excellent broadband quantum efficiency above 80%. Cross-talk reduction can be obtained by introducing high aspect ratio pixel separating trenches. A novel backside alignment strategy to avoid the use of glass substrate as temporary carrier for thinning is presented. And finally a feasibility study was discussed, concluding that, looking at bump yield for very dense structures with tight pitch, CuSn bumps are a good alternative to Indium bumps.

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