A Miniaturized Ground Surface Perturbation Lattice for Noise/Coupling Mitigation in Packaging Applications

Antonio Ciccomancini Scogna
CST of America
492 Old Connecticut Path, #505, 01701 Framingham, MA
Phone: +1/ 508-665-4400, fax: +1/508-665-4401 – email - antonio.ciccomancini@cst.com

Abstract

The ground surface perturbation lattice (GSPL) is proposed to suppress parallel-plate noise in mixed signal systems. The design concept of the GSPL structure consists of circular pads and multiple vias in order to enhance the bandwidth of the mushroom like EBG structure. The present paper investigates the usability of a miniaturized GSPL for noise/coupling mitigation in packaging applications. A sensitivity analysis of the bandgap region with respect to the position of the vias, the radius of the patch and the dielectric permittivity is performed. It is proven how several parameters allow shifting the band gap region and designing the power bus according to the desired specifications. The signal integrity (SI) is also investigated by considering a line routed from top to bottom layer and comparing the GSPL structure with a standard PWR/GND layer. Because of the absence of etched PWR/GND layer, it is demonstrated how the GSPL represents a viable solution for the noise mitigation in mixed signal applications.

1. Introduction

With the trend of increasing clock rate, low voltage levels, high integration and simultaneous switching noises (SSN), it is becoming a major challenge to design high speed or mixed signal circuits. To reduce SSN, planar power/ground (PWR/GND) layers are used widely in multilayer packages. Besides the fact that they have lower parasitic inductance for power supply and current return path, they provide additional capacitance between PWR/GND layers. However, planar PWR/GND planes form a cavity in the package substrate, and the resonance modes can be excited by SSN and generating parallel-plate noises (PPN).

PPN propagating between power and ground planes will cause signal integrity (SI), power integrity (PI) and electromagnetic interference (EMI) issues.

Several previous researches have studied the suppression of the PPN. Eliminating the PPN by adding decoupling capacitors parallel between PWR and GND planes is a typical way. The decoupling capacitors can provide a low impedance return path for ac perturbation currents. However, the effective series inductance (ESL) will let the capacitor behave as an inductor above the self resonance frequency that is usually in the range of hundreds megahertz only. The embedded capacitor with a very thin dielectric layer between the PWR and GND planes is another mitigating solution, but the planes still allow noise to propagate at some specific resonance frequencies.

More recently, electromagnetic bandgap (EBG) structures are proposed to eliminate PPN in high speed or mixed signal circuits, such as high-impedance surface (HIS) structures [1], coplanar EBG structures [2], and the photonic crystal power/ground layer (PCPL) [3,4]. All of them isotropically suppress the PPN by using periodical pattern within the desired stopband.

The concept of the PCPL consists in periodically embed the high dielectric constant (high-DK) cylindrical rods into the original substrate between PWR and GND planes. Even though the PCPL performance has been highlighted [4], such structure can be very expensive due to the non-standard fabrication of the high-DK substrate in PCB or package fabrication.

In this paper, a new structure with similar concept is proposed to solve the cost problems of the PCPL by embedding ground surface perturbation lattice (GSPL) [5] instead of high-DK rod between PWR and GND planes. The GSPL structure is composed of metal pads and conductive vias which can be manufactured in a standard PCB/package fabrication process. The basic structure of the mushroom-like

EBG structure [1] is evolved in the concept of the GSPL geometry to enhance the electromagnetic attenuation performance.

It is found that the proposed structure can maintain or enhance the stopband of the PCPL design.

2. Model to hardware correlation

An elementary GSPL geometry has been introduced in [6-7] and since then several improvements have been proposed and analyzed, all substantially heading toward the widening the noise suppression band.
Since the principles that make the GSPL structure more effective for PI purposes than the simple mushroom type counterpart has been already discussed in [5-6], this section of the paper focuses on verify the accuracy of the design concepts and model to hardware correlation.

A test vehicle including GSPL structure and reference board has been manufactured by using 4-layer FR4 PCB fabrication. The reference board consists of solid power and ground planes on a dielectric substrate whose thickness is 0.6 mm. Figure 1 shows the fabricated sample of the GSPL structure. The dimension of GSPL PWR/GND plane is 60mm by 60mm with 3x3 unit cells. The geometric parameters of the GSPL along with the location of the two test ports are highlighted in the same Figure.

The parameter $|S_{21}|$ representing the noise coupling coefficient is measured by using an Agilent N5230A vector network analyzer and Cascade Microtech microprobes (ground-signal-ground with 350 μm pitch) on a microprobe station. Figure 2 shows the simulated (by means of [8]) and measured results and they are compared means of the feature selective validation (FSV) technique [9].
Due to the good correlation the developed simulation models have enough accuracy to predict the behavior of the proposed structure.

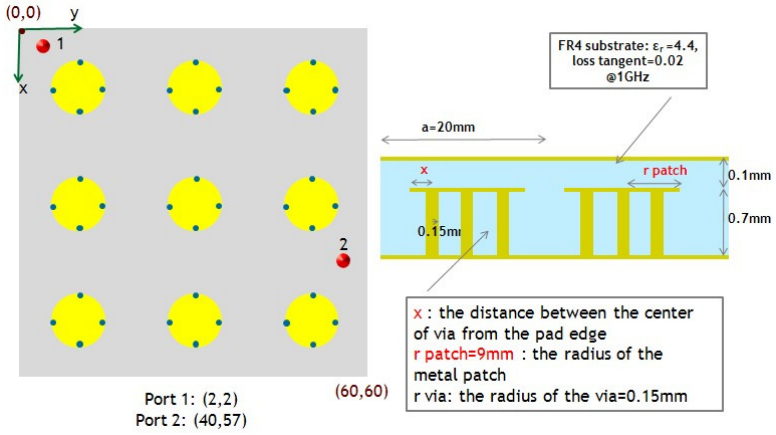
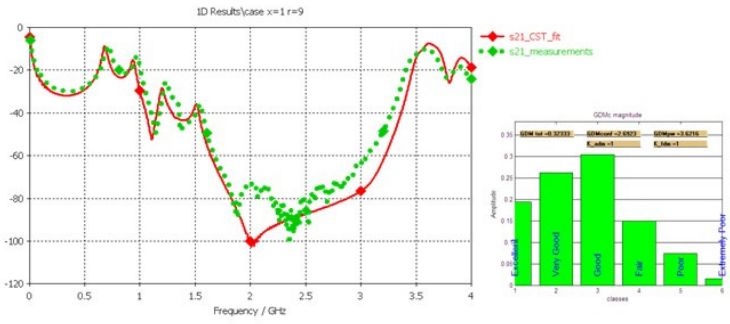
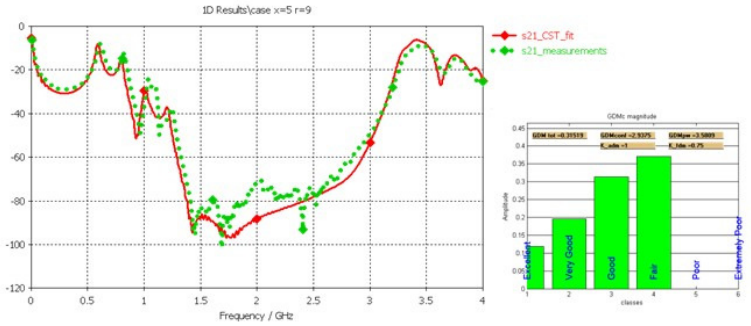


Figure 1 – Top view and cross section of the test GSPL board



(a)



(b)

Figure 2 – Noise coefficient S_{21} for a): x=1, r=9 and b): x=5, r=9; comparison between measured data and numerical simulation

3. PCPL and GSPL miniaturization

In this section the miniaturization of the proposed GSPL structure is analyzed and compared to a photonic crystal layer structure (PCPL), which has been originally proposed for PI applications by Wu in [3-4].

Figure 3 illustrates the PCPL test structure and figure 4 shows the noise coefficient results (S_{21} and S_{31}) for different values of the high dielectric permittivity (DK) used for the dielectric rods while keeping the radius of the rods constant.

Two values of DK are considered and the results (bandgap region) are summarized in the tables 1 and 2. The higher DK corresponds to broader bandgap region and a lower value for the cut off frequency can be achieved.

Table 1 – S21 bandgap for different DK values

r	DK	Bandgap [GHz]
2	100	2.6-4.5
2	300	1.5-3GHz, 3.2-4.7GHz, 5.5-6.8GHz

Table 2 – S31 bandgap for different DK values

r	DK	Bandgap [GHz]
2	100	2.4-4.8
2	300	1.2-3GHz, 3.2-4.7GHz, 5.5-7GHz

However it is well know that this PCPL technology is very expensive, since it require special manufacturing process, therefore a more standard structure based on the replacement of the dielectric rods with metallic objects is desirable.

Figure 5 depicts the proposed miniaturized GSPL structure, it consist of a 2x2 cells of 1mm each, a circular pad and 4 vias connecting the edge of the pad with the bottom layer.

It should be noted that through vias are implemented in order to keep consistency with the test board designed to perform model to hardware correlation of Figure 1.

The numerical model is validated by comparing 2 different numerical methodologies, finite element method (FEM) and finite integration technique (FIT). Results are illustrated in Figure 6 and good agreement is achieved over the whole frequency range.

Figure 7 compares the noise coefficient (both S_{21} and S_{13}) of the PCPL and the GSPL structure. The same cut off frequency is predicted, however the GSPL structure extends of 1GHz the bandgap region towards the high frequency values and it is a low cost fabrication process. Fixed values for vias location (with respect to the edge of the circular patch) and radius of the patch have been used, therefore the goal of the next section will be to explore whether it is possible to lower the cut off frequency and define some design parameters.

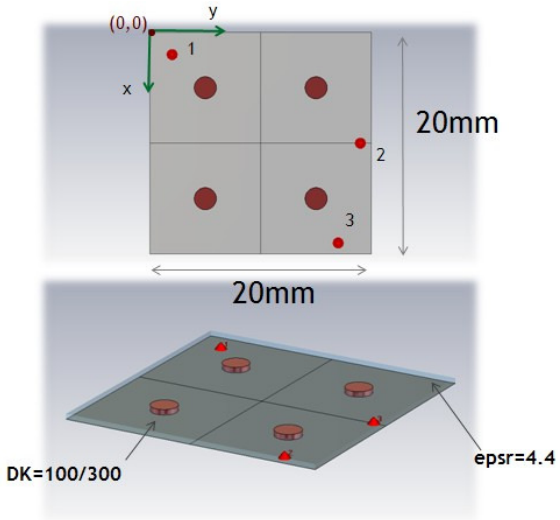


Figure 3 – Miniaturized PCPL (with 4 unit cells), top view and port location

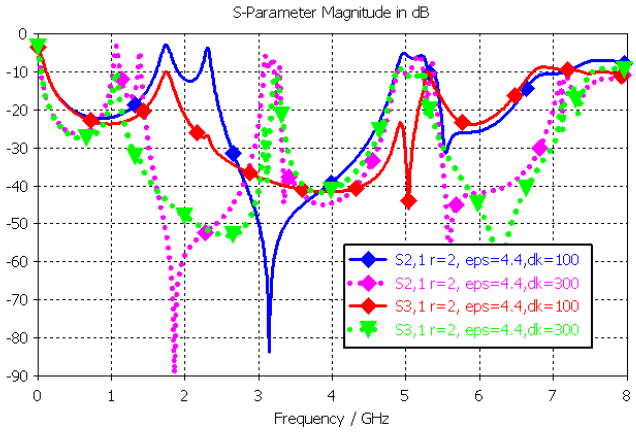


Figure 4 – Noise coefficients S_{21} and S_{31} for r=2, eps=4.4 and DK (rods) =100 and DK=300

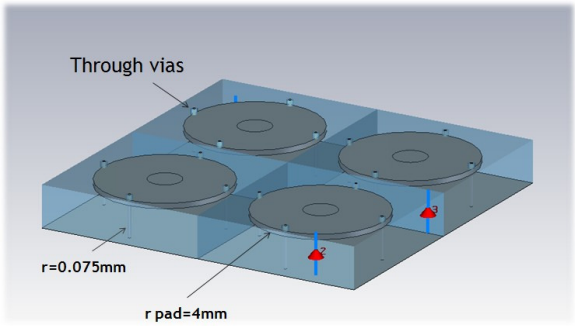


Figure 5 – Miniaturized GSPL (with 4 unit cells): perspective view and port location

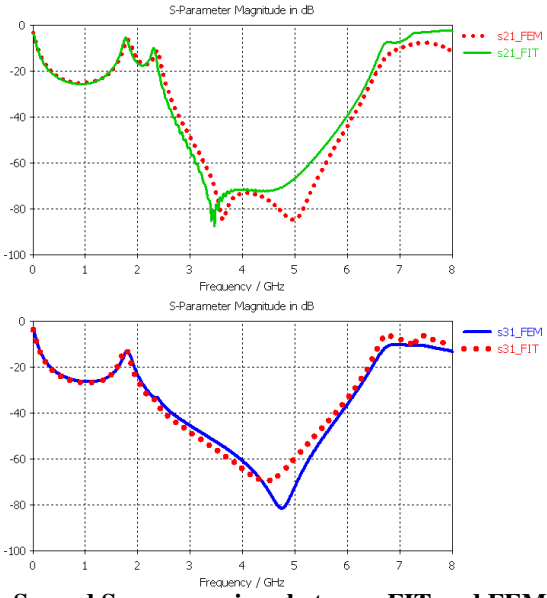


Figure 6 – Model validation: S_{21} and S_{31}, comparison between FIT and FEM numerical simulated results

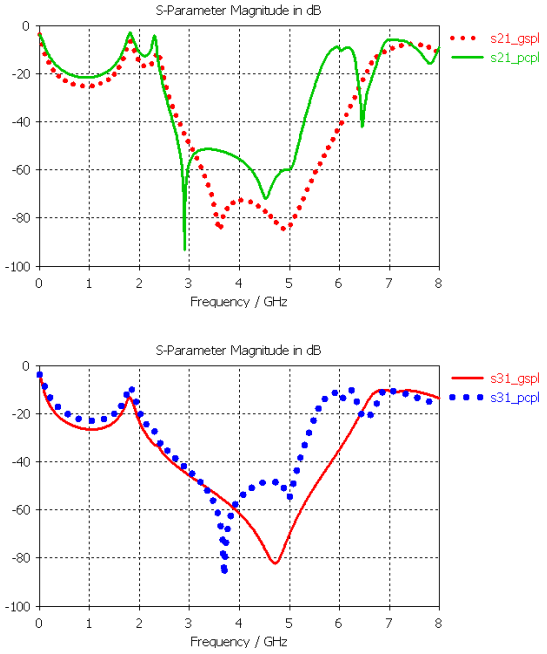


Figure 7 – S_{21} and S_{31}: comparison between PCPL and GSPL test board structures.

4. Power Integrity and Signal Integrity analysis of the miniaturized GSPL structure

The present section discusses the performance of the proposed GSPL structure with regarding to both SI and PI. A microstrip to microstrip transition from top to bottom layer is modeled in the GSPL structure, as illustrated in Figure 8. The dimensions of the design are the same of Figure 5, the trace width is 0.1mm, and the length of the two 90 degree traces is 8mm (top layer) and 10mm (bottom layer). The radius of the buried via is 0.05mm and the dielectric material has properties ε_r=4.4 with tgδ=0.01 at 1GHz. Port 4 and port 5 represent input and output for the microstrip transition, whereas ports 1, 2 and 3 represent monitor point on specific location of the GSPL structure and placed between the PWR and the

GND plane in order to measure the coupling coefficient.

From Figure 9 it can be clearly seen that a very similar value of the insertion loss is predicted for both the GSPL structure and the reference PWR/GND layer structure. This means that lines running on GSPL structures keep a good SI performance. Furthermore the noise coupling calculated for the GSPL structure is more than 30dB lower with respect to the PWR/GND layer in the bandgap region.

For instance the coefficient S_{14} presents a consistent reduction in the propagation noise (well below -40dB) within the frequency range 2-6GHz.
Similarly for S_{24} and S_{34} (Figure 10) a bandgap region can be clearly seen in the same frequency range, therefore proving the effectiveness and consistency of the proposed GSPL structure.

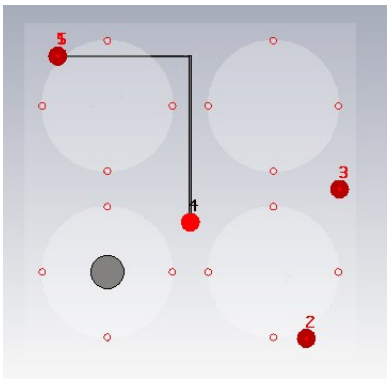


Figure 8 – Micro stripline top to bottom transition on the 4 unit cells GSPL board, ports 4-5 input/output of the trace and ports 3-5 PWR to GND plane connection

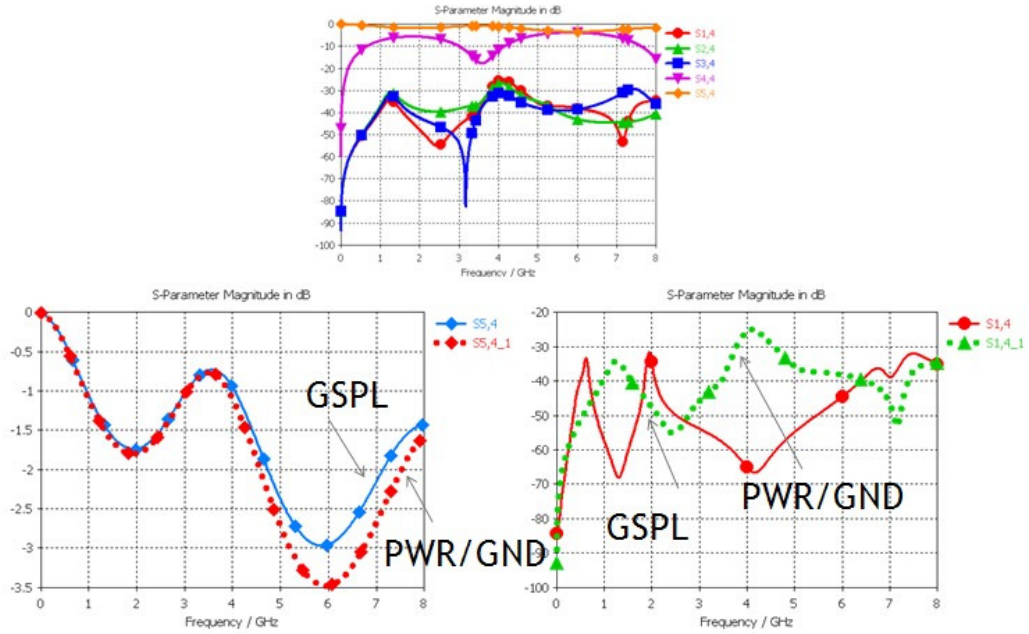


Figure 9 – S-parameter results for the configuration of Figure 6; noise coefficients and insertion loss comparison between GSPL structure and standard PWR/GND layer board

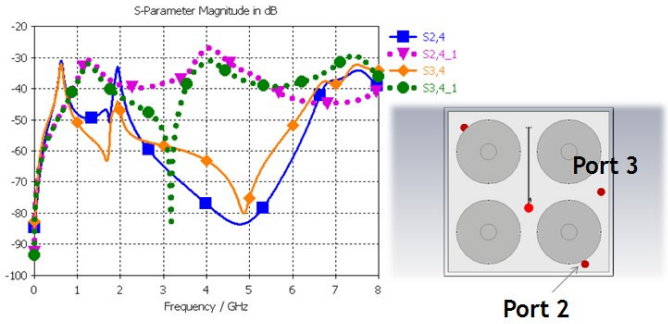
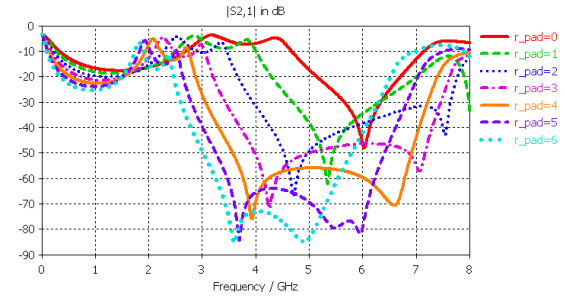


Figure 10 – Noise coupling coefficients S24 and S34: comparison between GSPL board and standard PWR/GND layer board.

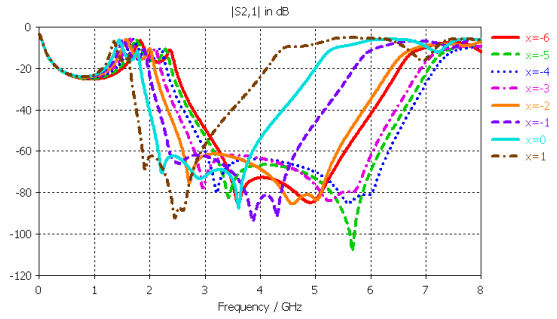
In order to understand possible design parameters of the GSPL structure, a sensitivity analysis is performed by varying the radius of the pad and the parameter **x**, which represents the distance between the vias and the edge of the circular path.
Results are illustrated in Figure 11, where the noise coefficient S_{21} is reported. In particular it can be seen how by increasing the radius of the GSPL pad, the cut off frequency can be lowered and, by reducing the value of the parameter **x** a similar effect can be noted. In this last case a lower frequency value of -30dB can be achieved while using the same dielectric material.

When increasing the permittivity of the dielectric (high DK material), the cut off frequency can be further lowered.

A parameter sweep on **x** and dielectric permittivity is then performed and results are reported in Figure 12. In particular the parameter **x** is varied between 7mm and 1mm, whereas ε_r is swept between 4 and 12. The 2 bounded curves are highlighter which corresponds to x=1 and ε_r=12 for the highest bandgap region and x=6, ε_r=12 corresponding to the lowest frequency. By changing the 2 parameters it is therefore possible to properly design the bandgap region within the wide frequency range 0.8GHz-6.5GHz.



(a)



(b)

Figure 11 – Noise coefficient S_{21} with respect to the variation of a) r_pad and b) x

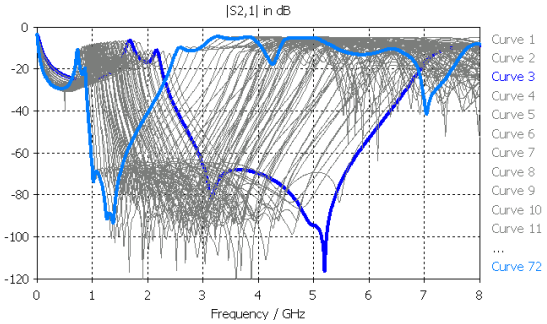


Figure 12 – S_{21}: parameter sweep of x and dielectric permittivity

5. Conclusions

A GSPL structure is proposed for the suppression of noise coupling in PWR/GND layers. Miniaturization is proven to be possible, therefore extending the usability of GSPL for packaging and mixed signal systems which combine high-speed digital circuits with analog and radio frequency (RF) circuits. GSPL is a promising alternative solution for SSN mitigation in PCBs/packages.

References

[1] R. Abhari, G.V. Eleftheriades, "Metallo - dielectric electromagnetic band gap structures for suppression and isolation of parallel-plate noise in high speed circuits", IEEE Trans. On Microwave Theory and Tech, vol. 51, no. 6, pp. 1629–1639, June 2003.

[2] T. L. Wu, Y. H. Lin, T. K. Wang, C. C. Wang, and S. T. Chen, "Electromagnetic bandgap power/ground planes for wideband suppression of ground bounce noise and radiated emission in high-speed circuits," IEEE Trans. Microwave Theory Tech., vol. 53, no. 9, pp. 2935–2942, Sep. 2005

[3] A. Ciccomancini Scogna, T.L. Wu, A. Orlandi, "Simultaneous Switching Noise Mitigation in PWR/GND Plane Pair by Means of Photonic Crystal Fence: Sensitivity Analysis and Design Parameters Extraction", accepted for publication on IEEE Trans. Adv. Packaging.

[4] G.-Z. Wu, Y.-C. Chen, T.-L. Wu, "Design and Implementation of a Novel Hybrid Photonic Crystal Power/Ground Layer for Broadband Power Noise Suppression," IEEE Trans. Adv. Packaging, vol. 33,no. 1, pp. 206-211, Feb. 2010.

[5] T.-L. Wu, A. Ciccomancini Scogna, A. Orlandi et Al. "Power Noise Mitigation and Bandwidth Enhancement by Using a Ground Surface Perturbation Lattice in Mixed Signal Circuits" to be submitted on IEEE Trans. on EMC.

[6] A. Ciccomancini Scogna, C.-D. Wang, A. Orlandi, and T.-L. Wu ,"Parallel-Plate Noise Suppression Using a Ground Surface Perturbation Lattice (GSPL) Structure", IEEE Electromagnetic Compatibility (APEMC), 2010 Asia-Pacific Symposium on, pp. 158-161, April 2010

[7] M-S. Zhang, Y-S. Li, C. Jia, L-P. Li, "A power plane with wideband SSN suppression using a multi-via electromagnetic bandgap structure," IEEE Microwave and Wireless Component Letters, vol. 17, no. 4, pp. 307-309, April 2007.

[8] Computer Simulation Technology, CST STUDIO SUITE 2010™, http://www.cst.com/, 2010.

[9] UAq EMC Laboratory, FSV Tool, downloadable at http://uaqemc.ing.univaq.it/uaqemc/FSV_1D_4_0_6/ University of L'Aquila, Italy, 2010.