Capacitance Calculation for Offset Via Structures Using an Integral Approximation Approach Based on Finite Element Method

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Abstract

A simple yet efficient approach is presented to extract the via-plane capacitances for an offset via structure. According to the integral approximation approach, the geometry of offset via is first divided into several segments with equally distributed angles from the origin. The two-dimensional FEM method for the concentric case is used for each segment based on its pad-stack parameters. Then, the final offset via-plane capacitance is approximated as the average of these 'segmental' capacitance values. Numerical examples demonstrated that the combined method has similar accuracy with a three-dimensional solver but it has much higher efficiency in both CPU time and memory cost.

Key words: offset via structure, via-plane capacitance, integral approximation approach, finite element method

I. Introduction

Via structures are commonly used in high-speed multilayer printed circuit boards. While they provide larger routing areas, via structures often inevitably introduce discontinuities in signal link paths, strong noise coupling to power distribution network and edge radiations. Thus, modeling the via-plate interaction is critical for analysis of signal integrity (SI), power integrity (PI) and electromagnetic interference (EMI).

A physics-based circuit model has been proposed to characterize via transitions in multilayer printed circuit board (PCB) [1][2]. In this model, a via is modeled as a short circuit for the barrel and two via-plane capacitances from the barrel to both top and bottom planes. Return path of the via is described as the impedance of the plane pair at the via location, which can be calculated using the cavity model method. If multiple vias are included in the plane pair, the impedance matrix is used to consider the via couplings. The physics-based model accurately describes the electrically small vias as lumped circuits and distributed effects of the parallel plane pair. Thus it works up to fairly high frequency based on several validations both with numerical simulation and measurement [1][2].

The via-plane capacitance plays a critical role in the physics-based model especially for high frequency S-parameter results. Thus, it is necessary to calculate the capacitance values accurately and efficiently for high-speed circuit designs. For axially symmetric case, the via-plane capacitances can be extracted using a two-dimensional (2-D) finite element method (FEM) on the ρ-z plane in the cylindrical coordinates. However, it is common in practical manufacturing that the center of a via drill is not at the center of its via pad and anti-pad. The offset makes the via geometry axially asymmetric, which has to be analyzed by a time-consuming three-dimensional (3-D) solver.

In this paper, the integral approximation method proposed in [3] is used so that 2D FEM can still be used to extract accurate via-plane capacitances for eccentric via structure. By transforming approximately a 3D structure into several 2D ones, hybrid integral approximation and finite element method is proved to be efficient yet accurate for engineering applications.

II. Two Dimensional FEM Formulation

Fig.1 illustrates a via which includes all possible via-plane capacitances. The top yellow part is showing the fringing capacitance between via and top plane. The middle green part is showing the via-plane capacitance inside the cavity (both capacitances between the via and top/bottom planes). The bottom blue part is showing the capacitance between the capacitance between the via stub extend to bottom signal layer and the bottom plane. All these capacitances can be calculated using the 2D FEM on

the ρ-z plane in cylindrical coordinates system. An example of the 2D meshing for the via-plane capacitance calculation is given in Fig. 2.

The basic governing equation used for the 2D FEM simulation is as follows: [4]

$$-\frac{\partial}{\partial\rho}\left(\rho\frac{\partial V}{\partial\rho}\right)-\frac{\partial}{\partial z}\left(\rho\frac{\partial V}{\partial z}\right)=0 \qquad (1)$$

where V is the electric potential in the computational domain.

Several boundary conditions may also be applied to solve the capacitance extraction problem appropriately [4]:

$$V = const \,@[\text{Condutor Surface}] \qquad (2)$$

$$\frac{\partial V}{\partial n}=0\,@\left[z=0\,\&\,\text{plane pair boundary}\right] \qquad (3)$$

$$\frac{\partial V}{\partial r}=\frac{1}{r}V\,@\left[\text{open boundary}\right] \qquad (4)$$

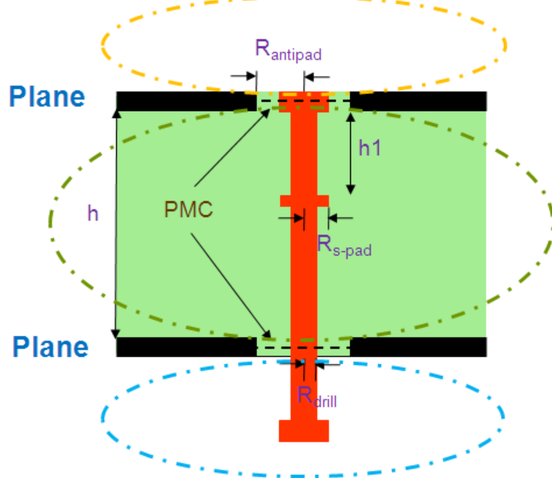

Fig. 1. A via structure includes all possible via-plane capacitances

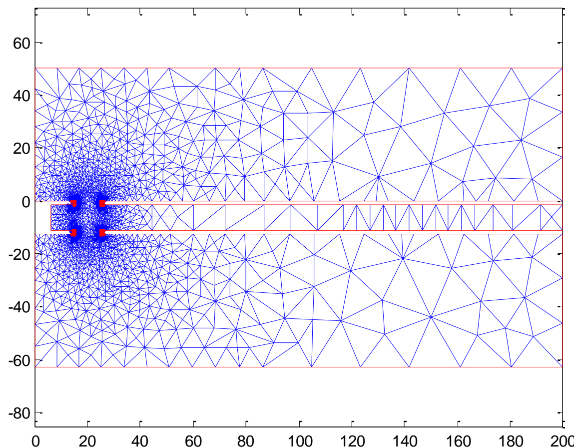

Fig. 2. 2D triangular mesh for via plane structure on *ρ-z* plane

where $r=\sqrt{\rho^2+z^2}$. Dirichlet boundary condition (2) is applied to the surface of the conductors (vias and planes) since voltage is constant on the surface of conductors. Neumann boundary (3) is applied to z axis because of symmetry of the geometry and it's also applied to the boundary of the plane pair boundary since we assume there is only tangential E component at the boundary of the plane pair. All the other boundaries (like top, bottom and outer boundary in Fig.2) of the computational domain will be treated as open boundary (4).

In order to extract the capacitance between the via and plane, a 3x3 short-circuit capacitance matrix is calculated for the three conductors (via, top plane and bottom plane). The diagonal terms of the capacitance matrix are extracted by applying 1V on one conductor and 0V on the other two conductors. The potential of the entire domain can be obtained by solving (1) and applying boundary condition of (2)~(4) using FEM. The electrical field can be further solved by calculating the gradient of the electrical potential and using the energy relationship shown as in (5), the diagonal capacitance can be obtained.

$$W=\iint_S \frac{1}{2}\varepsilon E^2=\frac{1}{2}C_{ii}V_i^2 \qquad (5)$$

where S is the whole computational domain, ε is the permittivity of the domain and V_i is the voltage applied to one of the conductors which is 1V. The off-diagonal capacitances are extracted by applying 1V on both two conductors and 0V on the third conductor. The electrical potential can be solved similarly and same for the electrical field. The energy relationship is used again as in (6) to get the mutual capacitances between two conductors.

$$W=\iint_S \frac{1}{2}\varepsilon E^2=\frac{1}{2}\left(C_{ii}V_i^2+2C_{ij}V_iV_j+C_{jj}V_j^{\,2}\right) \qquad (6)$$

where the absolute value of C_{ij} is the capacitance we want for the via-plane capacitance when i represents via and j represents either top plane or bottom plane.

The above 2D FEM method is developed for the concentric via structure. By introducing the integral approximation method, this 2D FEM method can be extended to extract capacitance for eccentric via structure which will be discussed in the next section.

III. Integral Approximation

The top view of an arbitrary offset via structure is shown in Fig. 3. From the via drill center

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a segment of the whole structure is also highlighted in Fig. 3.

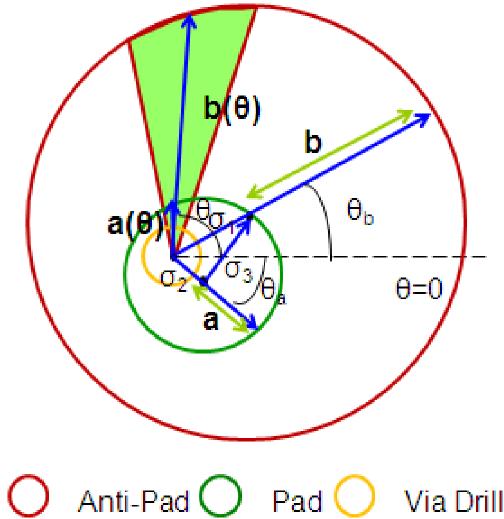

Fig. 3. Top view of arbitrary offset via structure

The radii of the pad and anti-pad (via hole) are denoted a and b; σ_1 and σ_2 represent the offset distance between the centers of the pad/antipad and the via drill and σ_3 for the offset between the antipad and the pad. θ represents the angle of the bisector in the segment of interest; θ_a represents the angle of the line connecting the centers of the drill and the pad (negative angle); θ_b represents the angle of the line connecting the centers of the drill and the antipad .

The equivalent pad and antipad radius inside the highlighted segment are denoted as a(θ) and b(θ). Their relation with the above distance and angle parameters are shown as follows:

$$b(\theta) = \sigma_1 \cos(\theta - \theta_b) + \sqrt{b^2 - \sigma_1^2 \sin^2(\theta - \theta_b)} \quad (7)$$

$$a(\theta) = \sigma_2 \cos(\theta - \theta_a) + \sqrt{a^2 - \sigma_2^2 \sin^2(\theta - \theta_a)} \quad (8)$$

To extract the via-plane capacitance for an offset via structure, the integral approximation [3] is used here:

$$\int_0^{2\pi} f(\theta) d\theta \approx \frac{1}{N_s} \sum_{n=1}^{N_s} f\left(\frac{2n-1}{N_s}\pi\right) \quad (9)$$

The via drill, pad, and anti-pad are divided into N_s segments with equally distributed angles from the origin. The bisector of each segment has a set of the pad-stack parameters such as pad radius, anti-pad radius and drill radius. The 2-D FEM method for the concentric case is used for each segment based on its pad-stack parameters as if it extends to a whole circle. Therefore, N_s different capacitance values are obtained using the 2D FEM method. Then, the average of these N_s capacitance values is calculated as the final offset via-plane capacitance.

This segmentation and averaging method is just the approximation of the real offset via structure. The validation discussed in the next section of this integral approximation with 3D full wave simulation actually shows that the error of this approximation can be sufficiently small if a proper N_s is chosen.

IV. Validations and Discussions

The geometry shown in Fig. 4 is used to validate the capacitance extraction results of the proposed method. The radii of the via drill, pad and anti-pad are 9, 17 and 23 mils, respectively. The offset between the via drill center and pad/antipad center is varying among 1mils, 3mils and 5mils. The results comparison with CST EM Studio, a 3D electro-static solver, is given in Table I.

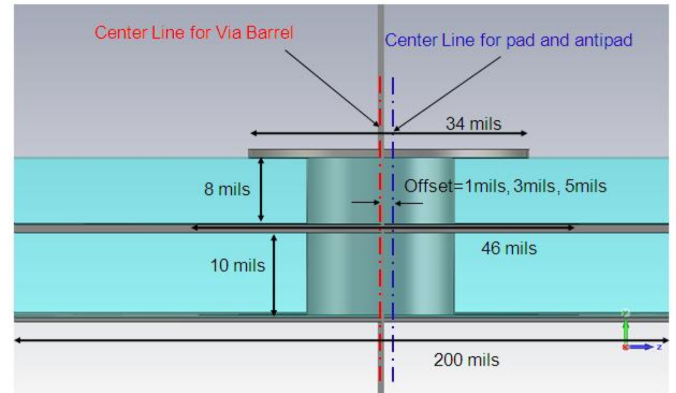

Fig. 4. Side view of a simple offset geometry

Table I Validation with CST EM Studio for geometry shown in Fig. 4

Offset	Capacitance (fF)	CST EM Studio	Our method
1mils	C_u	126.0	128.2
	C_d	34.3	34.3
3mils	C_u	127.1	128.6
	C_d	34.9	34.8
5mils	C_u	129.1	129.6
	C_d	36.1	36.0

C_u and C_d represent the capacitance between via and top/bottom planes. The results of our method are quite close to the results of CST EM Studio. The relative errors are within 2%.

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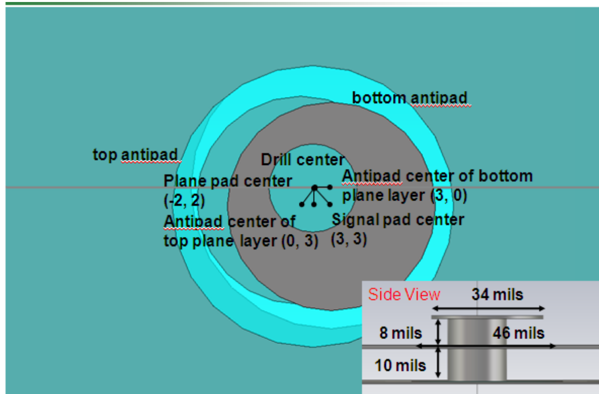

Fig. 5. Side view and top view of a complicated offset geometry

The geometry of a relatively complicated example is further used for validation shown in Fig. 5. The offset via geometry has top signal pad and top plane pad. The centers of top signal pad, top plane pad, top antipad and bottom antipad are all in different directions from the via drill center. Thus the coordinates of these centers are shown in Fig.5. The comparisons of via-plane capacitances with CST EM Studio are shown in Table II.

Table II Validation with CST EM Studio for geometry shown in Fig. 5

Capacitance	CST EM Studio	Our method
C_u (fF)	179.9	179.6
C_d (fF)	50.6	50.5

Again the comparisons in Table II show very good agreement between the proposed method and 3D full wave simulation (relative errors within 0.2%).

All the simulation is done on a workstation with Xeon X5450 processor with clock frequency of 3.00GHz and memory of 32Gbytes. Only one core is used for running the proposed approach of MATLAB code. The time cost for the case in Fig.4 is about 79 seconds and memory usage is ~300MB (By default, in MATLAB, all variables are stored in double precision format which it causes more memory than those of single precision format) while CST EM Studio spent up to 1091 seconds CPU time and required 3 Gbytes memory. For the case in Fig.5, our method used 88 seconds CPU time and about 300Mbytes memory. On the other hand, it costs CST EM Studio 1092 seconds CPU time and 3 Gbytes memory. It can be seen that the proposed method is much more time and memory efficient than a 3D solver.

Studies of via offset effects due to manufacture tolerances are critical for signal integrity analysis especially at high frequencies. The concentric via structure in multilayer PCB is shown in Fig. 6 and the eccentric via structure is shown in Fig. 7. The relative position of each pad/antipad center to the center of drill is also listed in Fig. 7.

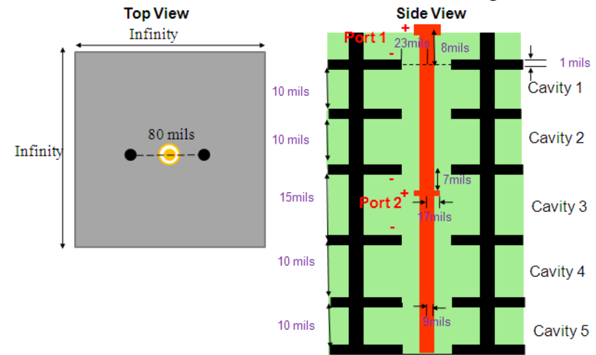

Fig. 6. Top view and side view of concentric via structure in multilayer PCB

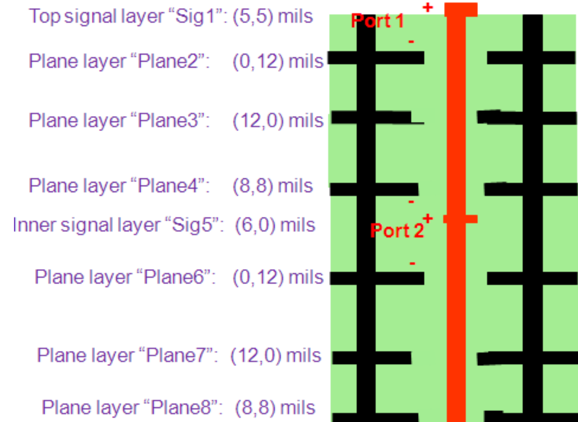

Fig. 7. Side view of eccentric via structure in multilayer PCB

The 2-ports S-parameters of the via transition in multilayer PCB can be obtained using the equivalent transmission line model [5] which is an extension of physics-based circuit model. The return loss S_{11} (magnitude) and insertion loss S_{21} (magnitude and phase) of both two cases in Fig. 6 and Fig. 7 are shown in Figs. 8, 9 and 10.

Fig. 8 ~ Fig. 10 indicate that via offset should be considered in accurately signal integrity simulations. The hybrid integral approximation and 2D FEM is demonstrated an efficient yet accurate approach to extract the offset via-plane capacitance, which can be used in practical via offset structure designs for optimization of signal integrity applications.

V. Conclusion

A simple yet efficient approach is presented to extract the via-plane capacitances for an offset via structure based on hybrid integral approximation and 2D FEM. The extracted capacitance values are validated by CST EM Studio. Via offset effects have been demonstrated and the hybrid method provides a

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fast way for via offset structure designs for optimization of signal integrity applications.

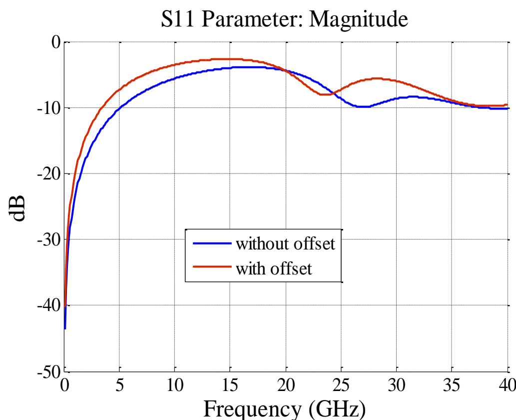

Fig. 8. S11 magnitude comparison of concentric and eccentric via structure

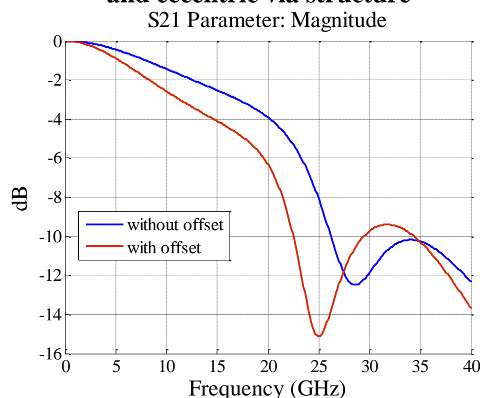

Fig. 9. S21 magnitude comparison of concentric and eccentric via structure

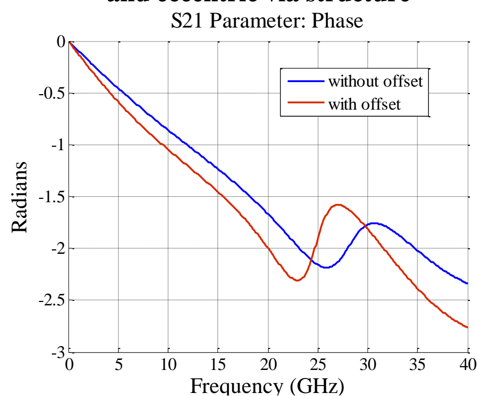

Fig. 10. S21 phase comparison of concentric and eccentric via structure

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