Successful Practices for the Modeling of Printed Circuit Boards and Substrates Using Electromagnetic Field Solvers

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Abstract

The aim of this work is to provide strategies for creating highly accurate models of printed circuit boards (PCBs) and substrates using electromagnetic field solvers. It will examine how to choose the correct field solver for a particular application from among full-wave, modal decomposition, finite element and boundary element methods. Tradeoffs between time and accuracy of the different solvers will be discussed. The focus is on model creation for use in time domain circuit simulators, but analysis of the frequency domain data will be used to correlate measurement to simulation. The problem of correlating simulation results with measurements is also discussed. A physical layer reference design (PLRD) board has been constructed, measured and simulated with the various field solvers. The results are analyzed to understand why differences occur between simulation and measured data. The impacts of these differences on system-level simulations of high-speed serial links are studied using a circuit simulator.

Introduction

Engineers and scientists have a variety of tools available to them today for the design and analysis of complex electronic structures. Analytical methods range from one dimensional circuit analysis techniques to full-wave three dimensional electromagnetic field solver approaches. This paper highlights several approaches available to engineers including the Finite Element Method, Method of Moments, and a Hybrid Modal Decomposition Method.

The first section provides a brief theoretical review of each approach along with references for additional reading. A general overview of computational electromagnetic (CEM) methods can be found in [1]. Next a discussion of accurate measurement techniques is given using the TRL method along with a description of the physical layer reference design (PLRD) board. The PLRD board is designed to provide a set of structures to identify electrical parameters of low-cost FR-4 dielectrics and high performance laminates. It has also been used to benchmark the electromagnetic analysis software with measurements. Transmission line segments and resonant structures are used to identify dielectric properties. Typical elements of single-ended and differential multi-gigabit data channels and some pedagogical structures are added to benchmark electromagnetic or signal-integrity simulators. All test structures are equipped with carefully optimized launches from SMA and 2.92 mm connectors to microstrip and stripline traces.

Finally, the different field solvers methods are used to analyze the PLRD board concentrating on commonly encountered geometries employed in electronic package and board fabrication. Differences encountered between measurement and simulation is discussed along with the advantages and disadvantages of the different simulation methods. A system level description detailing the effects in the time domain using a circuit simulator concludes the work showing the effects on multi-gigabit per second pulse responses, eye closure, eye jitter, and time domain reflectometry for the geometries studied.

Numerical Methods

Finite Element Method

Among the various numerical methods, the finite element method (FEM) is one of the most versatile and accurate techniques [2]. In the FEM, the problem exists within a domain that is enclosed by a finite boundary. The interior region may contain discontinuities, radiating or scattering objects, lumped elements, and ports. By discretizing the domain of interest into a number of smaller elements and by employing a variational technique, FEM can

be used to find the unknown electric and magnetic field distributions.

The transfinite element method is derived from the FEM by using specialized basis functions for the port boundary regions combined together with finite element interpolating functions for the interior region [3]. The FEM is used in this paper to compute fields and scattering parameters for arbitrary printed circuit boards and packages, but is not limited to this set of problems.

The solution starts from the following boundary value problem (BVP) for the vector wave equation:

$$\nabla \times \frac{1}{\mu_r} \nabla \times \vec{E} - k_0^2 \epsilon_r \vec{E} = 0 \qquad (1)$$

where $\vec{E}$ is the electric field, μ_r is the relative permeability, ϵ_r is the relative permittivity, and k_0 is the free-space wave number. This is subject to a set of boundary conditions including perfect electric and magnetic boundaries, absorbing boundary conditions, and port boundary conditions:

$$\vec{n} \times \vec{E} = \sum_{i=1}^{m} (a_i + b_i) \vec{n} \times \vec{e}_i \qquad (2)$$

Here it is assumed that the electric field patterns $\{\vec{e}_1, \ldots, \vec{e}_m\}$ for m port modes are known and $\{a_1, \ldots, a_m\}$, $\{b_1, \ldots, b_m\}$ are respectively the amplitudes of the incident and reflected waves for each mode. Application of Galerkin's procedure to the equations (1-2) leads to a sparse matrix equation where solutions for the electric field and scattering parameters are the unknowns of interest [4].

The solution process starts with generating a three dimensional finite element discretization. Tetrahedral elements are used in order to accurately model PCB and package geometries including but not limited to arbitrary plane configurations, traces, vias, pads, and bondwires. Hierarchical higher order interpolating functions are used and the order of interpolation within each element is determined automatically during the solution process based upon the field error within the element. Adaptive mesh refinement is carried out in the regions with the highest error and the solution process repeats itself until an accurate global field solution is obtained.

Since no simplifying assumptions are made regarding the geometry or materials used an accurate final solution is guaranteed. However, depending on the complexity of the geometry and the frequency band of interest, the size of the sparse matrix equation can approach tens or even hundreds of millions of unknowns. Consequently, this leads to large memory requirements and results in matrix solution being the most time consuming step in the adaptive process. There are several ways to speed it up. Specialized direct and iterative matrix solvers can be used that explore sparsity patterns and hierarchical properties of FEM matrices [5]. Alternatively, a discretization based domain decomposition method can be used to distribute the solution across a cluster of computers [6].

Method of Moments

In contrast to the finite element method where the electric and magnetic fields are the fundamental unknowns the method of moments (MoM) technique [7-8] solves an integral form of Maxwell's equations to determine the electric and magnetic currents on a structure. Normally, surface currents on conducting objects are computed, although volumetric currents can also be determined.

An integral equation formulation itself is exact and a MoM based solution can produce highly accurate predictions of circuit and package performance. However, in practice, numerous approximations are made to keep problem size and solution time tractable. The following paragraphs outline the basic ideas behind the method of moments and discuss some of the most commonly used approximations.

The solution process begins with the mixed potential form of Maxwell's equations as follows:

$$\vec{E} = -j\omega\vec{A} - \nabla V - \nabla \times \vec{F}/\epsilon$$

$$\vec{H} = -j\omega\vec{F} - \nabla\phi - \nabla \times \vec{A}/\mu \qquad (3)$$

Here $\vec{A}$ and $\vec{F}$ represent magnetic and electric vector potentials, respectively and V and ϕ are the electric and magnetic scalar potentials, respectively. These four terms are given by:

$$\vec{A}(\vec{r}) = \int \bar{\bar{G}}_A(\vec{r}, \vec{r}') \vec{J}(\vec{r}') dV$$

$$V(\vec{r}) = \frac{1}{\epsilon} \int G_V(\vec{r}, \vec{r}') \rho(\vec{r}') dV \qquad (4)$$

$$\vec{F}(\vec{r}) = \int \bar{\bar{G}}_F(\vec{r}, \vec{r}') \vec{M}(\vec{r}') dV$$

$$\phi(\vec{r}) = \frac{1}{\mu} \int G_\phi(\vec{r}, \vec{r}') \sigma(\vec{r}') dV$$

The electric and magnetic currents, $\vec{J}$ and $\vec{M}$, are the fundamental unknowns. The electric and

magnetic free charges, ρ and σ, are derived from the divergence of the currents. The various Greens functions, *G*, may all be the free space Greens functions but more often they are formulated to *analytically* include the effects of infinitely extending ground planes and dielectric layers, or rectangular cavities. Solvers that include these effects are known as "planar solvers" and are much faster for layered media because only currents on metallic portions of the structure (i.e. traces and vias) need to be calculated. Two significant approximations are introduced by including the layer effects in the Greens functions: the dielectric layers are homogeneous; and the dielectric layers extend (theoretically) to infinity.

The integral equation (4) for the currents is converted to a dense matrix equation using the method of moments [7]. Linear shape functions on a triangular grid are used most often. These can model arbitrarily shaped objects, thick metal layers, vias, and non-rectangular cross sections. Solution of the matrix equation yields an approximate description of the currents on the structure. Measureable performance metrics such as S parameters and fields can be then calculated from the currents.

So called fast algorithms [9-11] are often employed in practice to avoid memory requirements that increase as the square of the number of unknowns and solution times that increases as the cube of the number of unknowns when traditional matrix solution methods are employed. Fast methods allow modern "planar" solvers to analyze many small to mid-sized layered media structures more quickly than general FEM based solvers.

Hybrid Modal Decomposition Solvers

Hybrid solvers utilize a highly efficient modeling technique which analyzes complete power distribution systems along with signal nets for the characterization of entire electronic packages and boards. This includes multilayered power/ground planes containing multiple vias and multi-conductor signal traces. The total electromagnetic fields inside the multilayered structures (packages and boards) are decomposed into parallel-plate and transmission-line modes. Within each parallel plate waveguide region that is formed by a pair of power and ground planes a two dimensional wave equation is formulated and solved using the finite element method. For high speed digital designs only the fundamental, TEM, mode needs to be considered in these parallel plate waveguide regions. This is due to the high cut-off frequency associated with the higher order modes. Using these restrictions a modified form of Maxwell's equation needs to be solved.

$$\nabla_t \cdot \frac{1}{R+j\omega L} \nabla_t V_p - (G + j\omega C) V_p = 0 \quad (5)$$

The scalar unknown V_p represents the voltage drop between the planes, and *L*, *C*, *R*, *G* are respectively the inductance, capacitance, resistance, and conductance per unit area. The symbol ∇_t in (5) represents a two-dimensional gradient/divergence operator. Equation (5) is efficiently solved using a two dimensional finite element algorithm [12]. In addition to the power and ground planes, packages and boards have many signal traces passing between these planes. When a trace is present, the assumption that the electric field is orthogonal to the power and ground planes becomes invalid. Hence, a modal decomposition method is employed to decouple the transmission line TEM mode from the parallel plate mode [13, 14]. The traces between the planes and the microstrip line mode for traces on top/bottom of the package are modeled as admittance (Y) networks by using multi-conductor transmission line theory based on solving the Telegrapher's equation:

$$\frac{\partial^2}{\partial z^2} V_t - (R + j\omega L)(G + j\omega C) V_t = 0 \quad (6)$$

Here V_t is the modal voltage on the trace (a function of the distance parameter *z*) and *R*, *L*, *G*, and *C* are the trace parameters per unit length. Other discontinuities in the ground and power planes, such as through-hole signal vias, can be represented by equivalent circuits. The transmission line and via circuit parameters are determined by either analytical formulas or fast quasi-static field solvers. The circuit models for the traces and vias can then be combined with the two-dimensional finite element model of the planes to yield a matrix describing the entire system. With this hybrid methodology, large boards and packages can be solved accurately in a reasonable length of time, even when other three dimensional solver methods become intractable.

Test Bench

The physical layer reference design board (PLRD-1) is shown in Fig 1. It is designed to provide a set of structures for the identification of material parameters of low-cost FR-4 dielectrics and for benchmarking electromagnetic and signal integrity simulators using advanced VNA measurement techniques. There are 30 test structures on the board, comprising calibration structures, transmission line segments, and resonant structures, in addition to typical elements of single-ended and

differential multi-gigabit data channels. All test structures are equipped with optimized transitions from SMA connectors to microstrip lines to minimize measurement impedance discontinuities and extend the effective measurement bandwidth to beyond 20 GHz. These SMA transitions were designed to have a modal cutoff frequency of 35 GHz, well beyond the measurement bandwidth of the VNA.

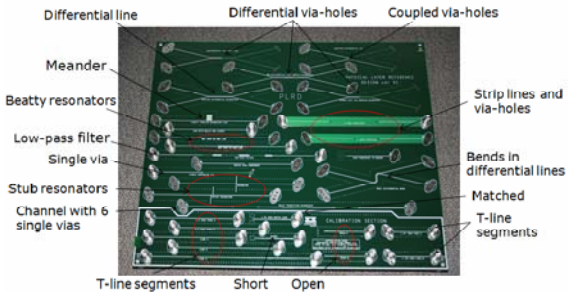

Figure 1: Physical layer reference design board (PLRD-1) with 30 test structures.

An Agilent N5230A 20 GHz 4-port network analyzer was used to measure S-parameters of the onboard TRL calibration kit, and for subsequent measurements of all 30 test structures. The impact of measurement cables, SMA connectors, connector-to-trace transitions, and lead-in traces are de-embedded from the measurements using TRL calibration techniques, yielding accurate measurements of the structures under test.

For example, Fig. 2 shows a test structure with a meandering coupled line. Measurements made with TRL de-embedding remove all cables, connectors, launches, and 1.5" of lead-in microstrip trace from each side of the meander structure, leaving the structure itself and 250 mil of microstrip on each side. This technique allows the full 20 GHz effective measurement bandwidth of the VNA to be applied to any target structure, without loss of fidelity.

Figure 2: Meandered coupled microstrip test structure.

To facilitate numerical modeling and simulation of the test structures, per-unit-length insertion loss and phase curves were calculated using the method of generalized modal S-parameters [15]. Dielectric and conductor material models used in the solvers were then fit to the Djordjevic-Sarkar [16] dielectric loss model, and to the Hammerstad-Jensen copper surface roughness model [17], using a heuristic approach with each target solver. All subsequent numerical modeling, simulations and correlations to measurement were performed with these heuristically extracted values as a starting point, with the understanding that FR-4 has well-known non-homogeneous and anisotropic properties that lead to large variations in electrical properties across single and multiple PCB fabrication units.

Numerical Results

The initial structure chosen for this work was a tightly coupled meandered microstrip shown in Figure 2. This type of geometry is often employed to length match signal nets. However, due to the electromagnetic coupling between the trace segments the overall electrical length is shorter than the equivalent physical length. For the specific test case the total physical length is 6,132 mils which would yield a 1.058 ns time delay for a straight trace according to [18].

$$T_d = \frac{l\sqrt{\varepsilon_r}}{c} \qquad (7)$$

where T_d is the propagation delay, l is the physical length, ε_r is the relative dielectric constant, and c is the speed of light in a vacuum. According to the measured and simulated TDR results, the propagation delay through the meandered line is approximately 685 ps, which is significantly lower than the 1.058 ns prediction based on the physical length. Comparisons between measurement and each of the CEM approaches mentioned in the Numerical Methods section are shown below. For the purposes of this work HFSS, PlanarEM, and SIwave have been used for the FEM solver, Method of Moments solver, and the Hybrid Modal Decomposition solver respectively, while DesignerSI has been used for the circuit analysis.

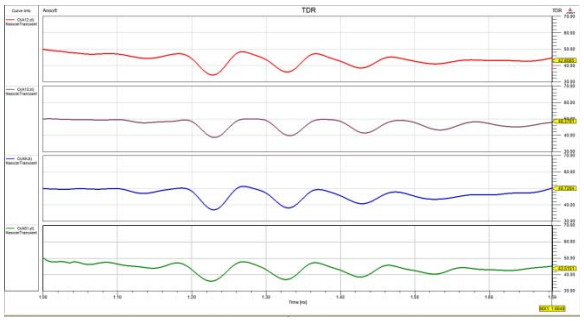

Figure 3: TDR results of meandered line: HFSS – top/red, SIwave – upper middle/purple, measured – lower middle/blue, and PlanarEM – bottom/green.

Frequency domain results from measurement and simulations show excellent correlation.

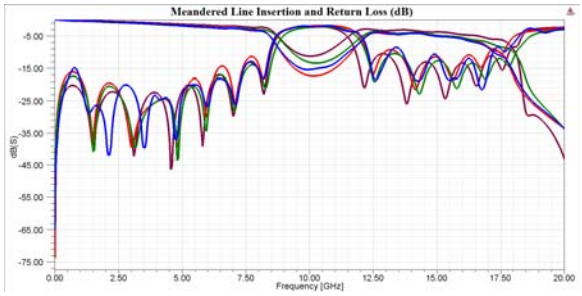

Figure 4: Comparison of insertion loss and return loss in dB for the meandered line: HFSS – red, SIwave – purple, measured –blue, and PlanarEM – green.

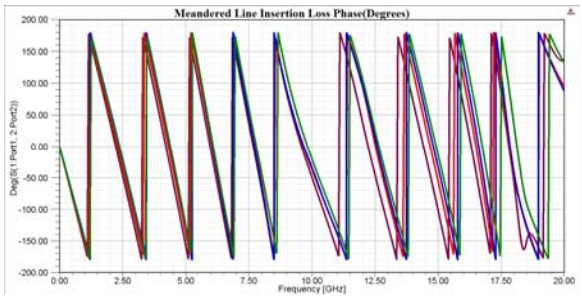

Figure 5: Comparison of insertion loss phase in degrees for the meandered line: HFSS – red, SIwave – purple, measured –blue, and PlanarEM – green.

Time and memory are the tradeoffs for better agreement between measurement and simulation. Table 1 compares the memory usage and simulation time for the various field solver methods used. All simulations were performed on a Dell Precision 490 workstation using two microprocessors with multiprocessing over four cores.

Simulation Method	Elapsed Time	Peak Memory	Total Cores
SIwave	11 s	54 MB	4
HFSS	1h 30m 7s	1.79 GB	4
PlanarEM	17m 53s	213 MB	4

Table 1: Comparison of compute resources for results shown in Figure 2.

The slight frequency shift in the Hybrid Modal Decomposition results shown in Figure 4 is due to the absence of a conformal solder mask during the simulation. Figure 6 corroborates this claim by comparing the Model Decomposition results to those of the FEM solver with the conformal soldermask was removed. Note that both sets of simulation results shift resonances to the left of the measured data when a conformal soldermask is not used.

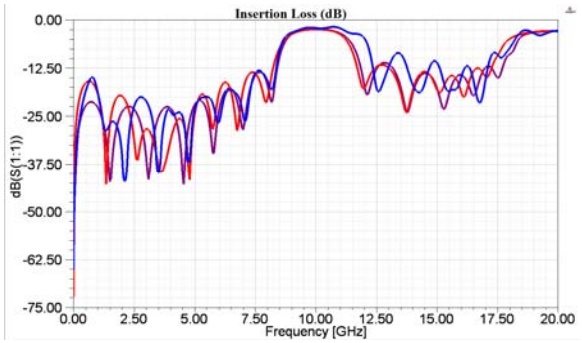

Figure 6: Comparison of return loss in dB for the meandered line: HFSS – red, SIwave – purple, and measured –blue.

It is important to understand the impact of simulation accuracy on system level performance. Meandering traces are commonly used to match the lengths of signal nets to help ensure proper latching of data at the receiver. Memory busses commonly length match data lanes to accommodate the source synchronous clocking architecture utilized in DDR, DDR2, and DDR3. To study the effect that minor frequency domain simulation differences would have on a single ended net at 2 Gb/s, each Touchstone® model has been placed into a circuit simulator and simulated using a convolution technique. Since this study includes only linear time invariant components a technique known as Peak Distortion Analysis (PDA) [19] was used to determine the worst cast bit patterns for each set of data. PDA provides the worst case eye closure and jitter and therefore yields the fairest comparison of the models in a real system that operated for multiple years. The measured data contains a passivity violation of 1.00066 at 300 KHz and did not include a DC data point. These problems are a source of error when using s-parameter files during circuit simulation.

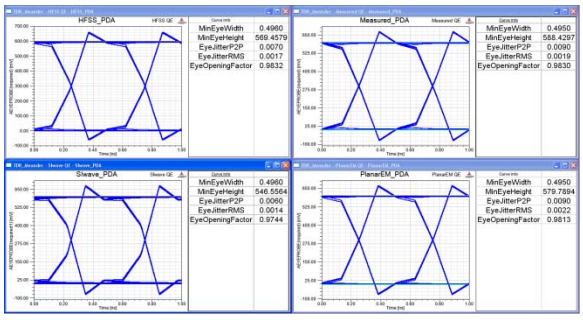

Figure 7: Comparison of time domain results from different models using PDA: HFSS – top left, SIwave – bottom left, measured – top right, and measured – bottom right.

Table 2 shows a comparison of the different eye quantities to give an indication of the effect on system level performance.

Measurement	TRL	HFSS	PlanarEM	SIwave
Eye Width	248ps	248ps	248 ps	248 ps
Eye Height & % Difference	588mV	569mV & (3.2 %)	580 mV & (1.4%)	547mV & (7.0%)
RMS Jitter	0.95ps	0.85ps	1.1 ps	0.7ps
P2P Jitter	4.5ps	3.5ps	4.5 ps	3.0ps

Table 2: PDA comparisons of Eye and Jitter between the TRL measurement and simulations for the meandered line.

The impact of the convolution technique can be determined by looking at the pulse response of the channel in the time domain. Differences in the pulse response add up via superposition, thereby creating the differences shown in Figure 8. These differences are due to inter-symbol interference (ISI) of the models, which is deterministic in nature. This simulation used a bit width of 500 ps (2 Gb/s) with a rise and fall time of 50 ps each. The reader can see minor differences between in the amplitudes of the cursor and post cursors which are the main contributors to the differences in the eye diagram shown in Figure 7 and Table 2. The tail of the pulse response decays to zero volts thereby reaching steady state and ensuring all ISI is accounted for during the convolution circuit analysis [20].

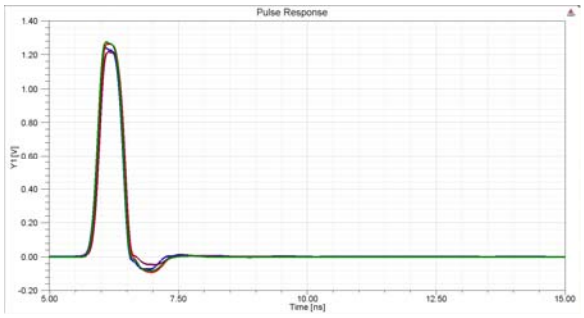

Figure 8: Comparison of the pulse responses obtained from the meandered line models: HFSS – red, SIwave – purple, measured –blue, and PlanarEM – green.

Several other structures including a Beatty resonator and a low pass filter have been studied using a similar technique to the previously discussed meandered line. The Beatty resonator shows excellent correlation between measurement and simulation. The author's will include the MoM simulation results in the final presentation and were not included here due to time deadlines for this work. However, based off the authors' experiences with MoM field solvers it is expected the results will correlate very well.

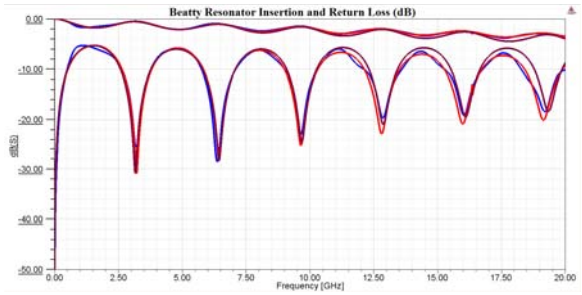

Figure 9: Comparison of insertion and return loss for a beatty resonator: HFSS – red, SIwave – purple, and measurement – blue.

Finally a comparison between a low pass filter and different simulation methods was performed. The insertion and return loss correlation is shown in Figure 10.

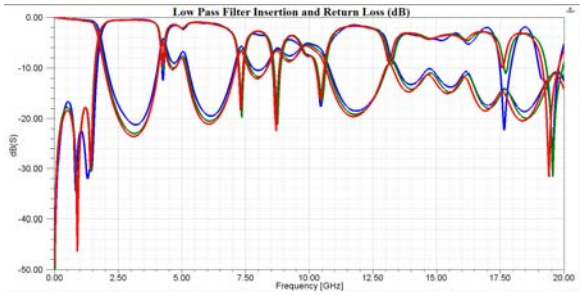

Figure 10: Comparison of insertion and return loss for a low pass filter: HFSS – red, measurement – blue, and PlanarEM – green.

The hybrid modal decomposition is not well suited for this type of filtering structure due to the highly divergent electric field where the structure jumps from a 6.3 mil wide trace to a 63 mil trace.

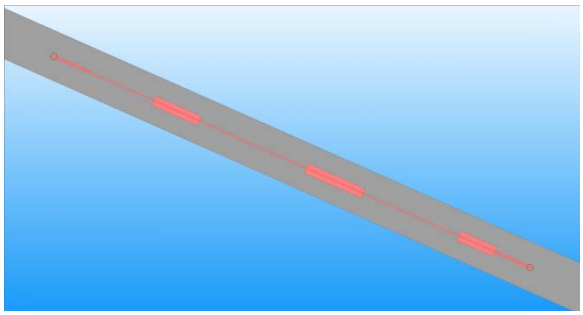

Figure 11: Low pass filter with trace width varying from 6.3 mils to 63.0 mils.

Up to approximately 5 GHz correlation is decent but beyond that the diverging electric field causes correlation to degrade. Figure 12 shows the

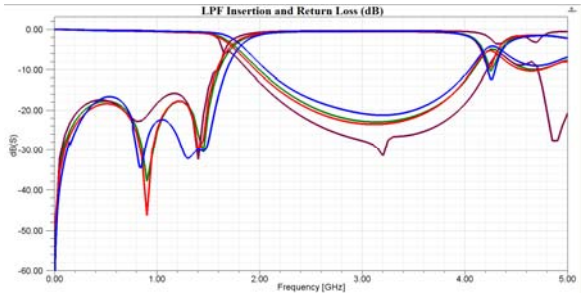

Figure 12: Comparison of insertion and return loss in dB for the low pass filter up to 5 GHz: HFSS – red, SIwave – purple, measured –blue, and PlanarEM – green.

insertion and return loss up to 5GHz with decent correlation for the hybrid modal decomposition solver where Figure 13 shows correlation out to 20 GHz, which shows that this solver technique would not be suitable for highly divergent trace sizes (10x) beyond about 5 GHz.

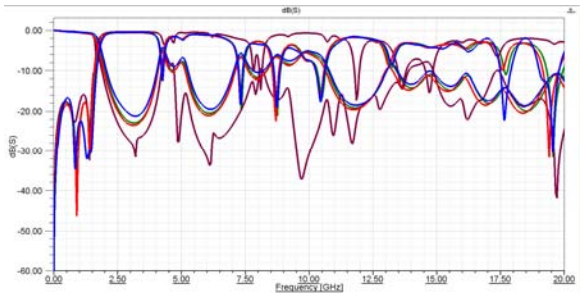

Figure 13: Comparison of insertion and return loss in dB for the low pass filter up to 20 GHz: HFSS – red, SIwave – purple, measured –blue, and PlanarEM – green.

However, Table 3 shows that if used correctly an engineer can quickly do an initial analysis with SIwave for immediate results while utilizing an FEM or MoM solution to tune the low pass filter after the initial design work is complete. The ability to make sound tradeoffs in seconds is invaluable to a design engineer where time to market is essential to a profitable business.

Simulation Method	Elapsed Time	Peak Memory	Total Cores
SIwave	43 s	37 MB	1
HFSS	13h 3m 6s	11.2 GB	1
PlanarEM	1h 37m 25s	294 MB	1

Table 3: Comparison of time and memory usage for SIwave, HFSS, and PlanarEM simulations.

Successful Practices

Advanced electromagnetic field solvers must be used with care if high accuracy and fast solution times are desired. The user should have some understanding of the underlying methods employed by the different solvers to achieve the best possible results. Port setup, meshing considerations and frequency dependent material behavior are three areas that require special attention for accuracy, speed, and memory usage along with passivity and causality considerations.

A highly accurate description of the geometry being modeled is critical. Conductor thickness, surface roughness and conductor cross section cause secondary effects in some designs but should be taken into account to achieve the best possible accuracy. In some situations these parameters can have a very strong effect. For the test designs shown above, results compared very poorly with measurements when 1 ounce copper was simulated rather than 2 ounce copper used in the fabricated hardware. In addition the effect of a conformal soldermask was shown as well. Differences due to the Dk/Df and surface roughness was outlined in [15] and found to be true for this work as well.

Perhaps the most important decision to be made when modeling printed circuit boards and associated components is the choice of simulator. No single numerical method is well suited for all types of problems and all simulators have classes of problems where they work best. For example, an FEM based simulator is very well suited for problems of very high geometric complexity (e.g. escape routing near complex connectors along with the connectors themselves) but may be less well suited for the analysis of full-sized printed circuit boards where a hybrid modal decomposition solver is better. A planar MoM based solver is often best suited for mid-sized PCB's of moderate complexity or components where very high accuracy is needed. In summary, the best possible results in terms of accuracy and simulation time will be obtained when the field solver is well matched to the problem at hand.

Other strategies for improving accuracy and confidence in simulated results include comparing the results from multiple simulators when possible and in doing parametric studies to see what physical and modeling setup parameters (i.e. mesh density or convergence tolerances) have significant effects on the results.

The PLRD board included TRL structures for de-embedding of the 2.92 mm connectors which provided a clean launch for comparisons of the data. An in depth understanding is required when performing TRL calibrations to ensure accurate measurements. In addition SOLT (short, open, load, thru) calibration can be performed for experiments however this requires additional modeling of the connector used along with the launch structures. Without this exact correlation is impossible to obtain making it difficult to understand if the channel characteristics such as IL, RL, NEXT and FEXT are due to the channel or the extraneous connectors.

Finally, no amount of cross-solver correlation compares to rigorous benchmarking against precision measurements, as was performed in this paper due to the inability to properly define material properties. Due to the wide variability of published material properties in high volume manufacturing sophisticated statistical analyses must be employed to ensure accurate modeling and system performance over all process corners. Package and printed circuit boards must be accurately measured and used for initial numerical model correlation to quantify future modeling approaches. Complete confidence is gained by incremental correlation to complex resonant and coupled structures, with well-defined characteristics and electromagnetic boundaries. Only then can an honest assessment of the capabilities, limitations, and performance of a particular simulation method be performed.

Conclusions

This work has discussed several common computational electromagnetic approaches and their application to the PLRD board. Each approach has shown that when applied correctly excellent correlation can be achieved with measurement (and with other simulation methods.) It is important to consider the tradeoffs each approach brings between accuracy, simulation time, and memory usage. Similarly it is important to understand that measurement accuracy requires precision and an understanding of the different measurement methods to achieve highly accurate extracted models. In order to validate measurement and simulation a comparison between each is needed and sometimes independent verification between simulation methods will be the best approach to ensure high quality models for usage in a circuit simulation.

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