A Systematic Approach for Creating a System-In-Package (SIP)

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Over the past several decades the quest to design electronics that boast ever increasing capabilities while continuously decreasing their size and weight has led to the development of a series of new packaging solutions. As the need for more functionality in less real estate increased, Multiple Chip Modules (MCM) were no longer satisfactory in many applications. Today, these applications call for a highly integrated packaging approach which often incorporates multiple functionalities into one package. In situations where time to the market for SOC (System on a Chip) is too slow or too costly the approach of System-in-a-package (SIP) can be the ideal solution.

One element in modern packaging is the use of new 3D structures and high-k dielectric materials. The second element is advanced packaging methods. New technologies such as chip-on-chip assemblies have been developed. The third element has been the progression in design tools that allow engineers to seamlessly design an overall, highly integrated system. The forth element, testing, is often an expensive part of product development. With SIP technology that cost can be significantly lowered, making new product development economically more feasible.

In this paper we present a systematic approach to designing highly integrated and miniaturized SIP packages. This approach enables rapid design, prototyping and time to production while achieving a new level of integration, miniaturization and reliability.

Finally, a case study is presented to demonstrate a typical maturity cycle of a SIP, in this case for a wireless application.

Definition for a System-in-Package

System-in-Package (SIP) integrates multiple active electronic components of different functionality with passives and other devices like MEMS or optical components. These components are assembled into a single (preferably standard) package that provides multiple functions associated with a system or sub-system.

The SIP approach meets the growing demands for miniaturization of electronic devices that support multiple functions. SIP performs full functional system or sub-system functions at the package level. SIP has evolved into 2D & 3D integrated modules of several chip packages lined up side-by-side or stacked. Passives or other required components are added into the package.. Many applications of SIPs fall into the family of 4C products (Computer, Communication, Consumer and Car electrics). However, application possibilities of these devices are nearly endless.

Benefits of System in a Package

Industry and market trend shows great convergence of 4C's in handheld products such as cell phones, GPS, PDA devices and so on. The main benefits the SIP approach offers are:

- ✓ Small form factor with innovative functions,
- ✓ Flexible design and high level of integration: Incorporate multiple flash devices, SRAMs, DRAMs, microcontrollers,ASICs and passive components into very thin packages that can fit into sleeker, more stylish, and yet more complex electronic gadgets.
- ✓ High electrical performance: Better electrical performance is also achieved because of the shorter interconnections within the SIP.
- ✓ Low cost and rapid time to market: Drastic reduction in development time and competitive advantage via being able to bring a new product to the market much more quickly.
- ✓ Excellent alternative to System-on-Chip (SOC): SOC can be difficult to design and

build as different functions are combined into one fabrication technology. SIP can combine multiple die (manufactured using different wafer fabrication processes) without performance tradeoffs. As a result time to market can be reduced, development costs are lowered and supply chain management becomes more effective (**Figure 1**).

Overall, SIP provides an excellent solution for ease of system level manufacturability and design. By integrating critical components into one SIP package, the system complexity, size and component placements can be reduced.

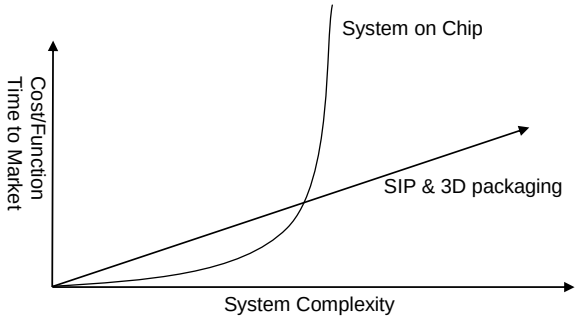

Figure 1: Cost/function and time to market versus system complexity for System-in-Package (SIP) compared to System-on-Chip (SOC).

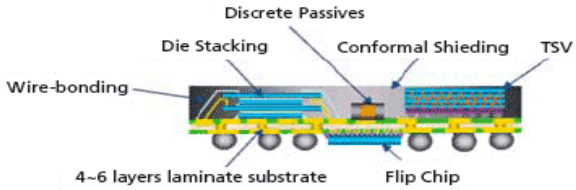

Figure 2: SIP module cross-section.

The Systematic Approach

The challenge: An interconnect solution that provides the end customer with the smallest footprint, lightest weight and best performance SIP.

The solution: Systematic approach for the development of SIPs is summarized in Figure 6.

Here we present a case study for a cell phone transmitter with three chips, however, the approach can be used among many other applications where space saving and reliability are critical factors.

Phase I: Pathfinder

A concept is developed working closely with the user. Various requirements are defined (e.g., mechanical, electrical, thermal, test, cost.

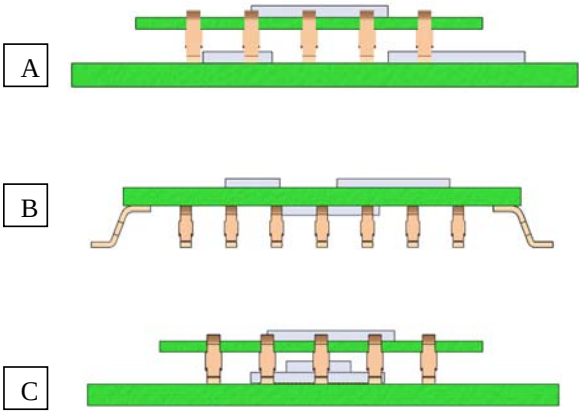

Figure 3: Case study SIP Phase I (pathfinder). Different design options are shown. A: Die attach with wire bond and board stacking. B: Die attach and wire bond with 2-sided board and leadframe. C: Die Flipchip and die stacking with board stacking.

Phase II: Preliminary/Critical Design Review (PDR/CDR)

- First level modeling and simulation (mechanical, thermal, electrical).
- Board layout (Gerbers, fabrication drawing)
- Scheduling and cost estimates
- Signal Integrity (SI) analysis
- Development of test plan

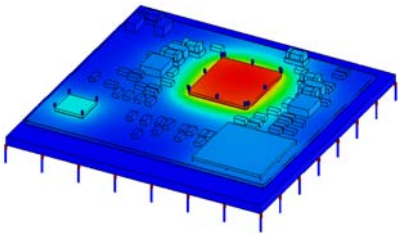

Figure 4: Case study SIP (PDR/CDR). Thermal simulation.

Phase III: Assembly

- Develop the BOM (Parts list)
- Substrate fabrication
- Process development and tooling
- Prototypes to pre-production and to production quantities
- Documentation (process flow chart, traveler, assembly drawings, etc.)

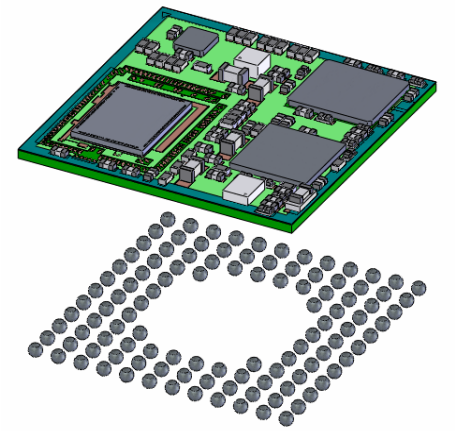

Figure 5: Case study SIP Phase III (Assembly).

CONCLUSION

The term "System-in-Package" refers to an innovative, highly integrated semiconductor device that incorporates multiple chips and components in a single package. Electronic devices consist of several individually packaged IC's with different functions. SIPs enable tremendous space savings and significant miniaturization of electronic devices.

Drastic reduction in development time, risk and product-to-market schedule are some of the clear advantages of the SIP approach. With SIP technology product developers are able to integrate multiple flash memories, SRAMs, DRAMs, microcontrollers, ASICs and passive components into very thin packages Sleeker, more stylish, and yet more capable electronic gadgets result.

Aside from shorter time-to-market, SIP reduces overall manufacturing and test costs since only one package needs to be assembled and tested. Better electrical performance is also achieved because of the shorter interconnections within the SIP. SIP's also simplify the process of assembling the final application module by requiring simpler PCB layouts because the complex interconnections required by the system are contained within the SIP.

A systematic approach to designing SIPs (Figure 6) further enhances the potential of the SIP technology because it leads to optimum and efficient designs. The case study that is presented in this paper is only one of many possible applications of using the SIP methodology. The method allows product developers to respond to the demand for highly miniaturized electronics with increased functionality and performance. The approach also enables developers to be more price competitive

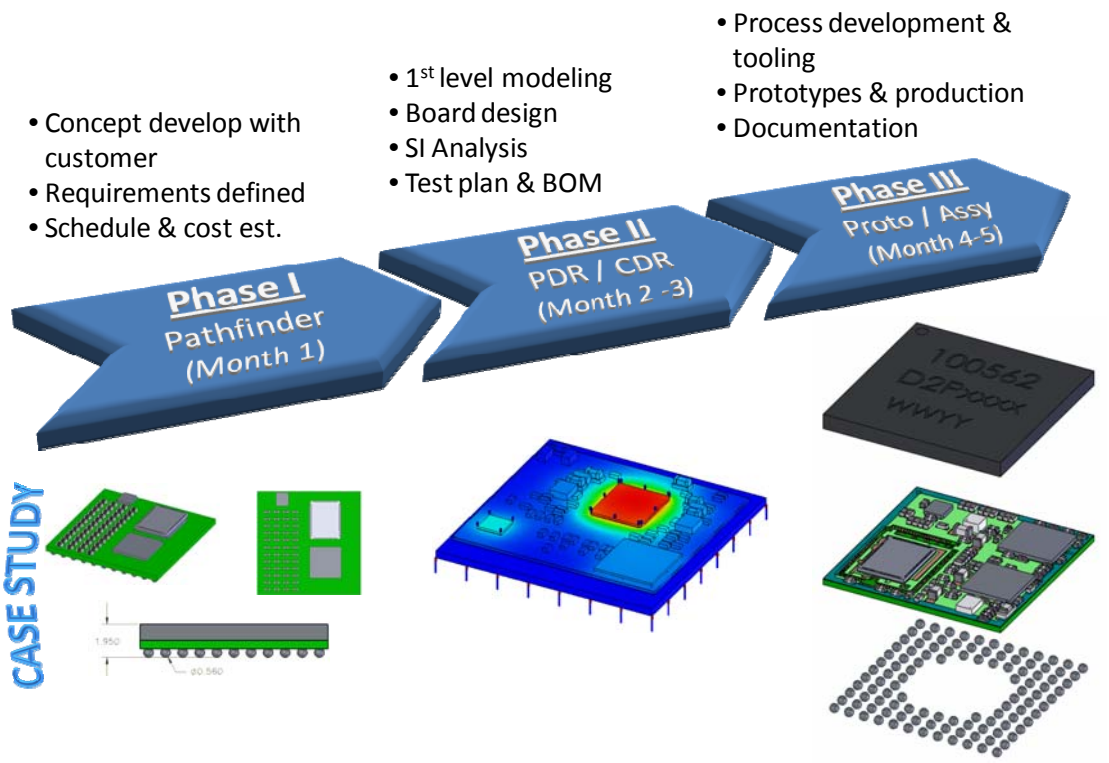

Figure 6: Depiction of the systematic SIP development approach.

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