Chip-last Embedded Actives and Passives in Ultra-Miniaturized Organic Packages with Chip-First Benefits

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Abstract

Embedded actives and passives are being pursued by chip-first and wafer-level fan-out approaches to address high functionality and miniaturization. A next generation embedding alternative- "chip-last embedding", which retains all the benefits of chip-first, has been demonstrated at Georgia Tech for complex multi-component heterogeneous systems. This paper presents detailed results from the first demonstration of this novel technology called Embedded MEMS, Actives and Passives (EMAP) with Chip-Last (CL) interconnections. This technology is targeted at highly integrated modules and systems with multiple 2D and 3D ICs for RF, Digital, Analog, MEMS and passive devices.

Ultra-thin (55µm) silicon test dies were embedded in a 60µm deep cavity within 6-metal layer substrates yielding a total module thickness of 0.22mm. The robustness of substrate materials and processes was demonstrated using thermal cycling of the blind-vias and through-holes. The embedded IC was bonded to the substrate at 160°C by ultra-fine pitch (30-50µm) and low-profile (10-15µm) Cu-to-Cu interconnections with polymer adhesives. Two different die-sizes 3mm x 3mm and 7mm x 7mm were investigated for reliability performance of these interconnections, which passed 1000 thermal cycles, in addition to Highly Accelerated Stress Test (HAST) and High Temperature Storage Test (HTS).

Comprehensive analysis of new materials and processes used in the chip-last embedding technology has been carried out demonstrating the advantages and robustness of this promising technology. Due to manufacturing process simplicity and unparalleled set of benefits, the chip-last technology provides the benefits of chip-first while enabling highly miniaturized, multi-band, high performance modules with embedded actives and passives.

Keywords: Embedding, Chip-last, Cu-to-Cu, Adhesives, Interconnections

Introduction

Ultra-miniaturized and low-profile mobile products are driving the need for embedded active and passive component integration technologies. Two such pioneering technologies, based on "chip-first" embedding are currently being pursued by the industry- 1) embedding in wafer level packages by wafer-level fan-out (WLFO) to get higher I/Os than previous wafer level packages [1], and 2) embedding in organic substrates to enable thinner packages [2]. These technologies are based the chips simultaneously mounted on either- 1) detachable tape molded by carrier or molding compound, or 2) rigid core laminates followed by interconnection using thin film package or PWB processes.

Georgia Tech Packaging Research Center (GT-PRC) is pioneering next generation embedding technology, called chip-last, to overcome some of the manufacturing and business challenges of chip-first, and to enable highly miniaturized multi-functional systems.

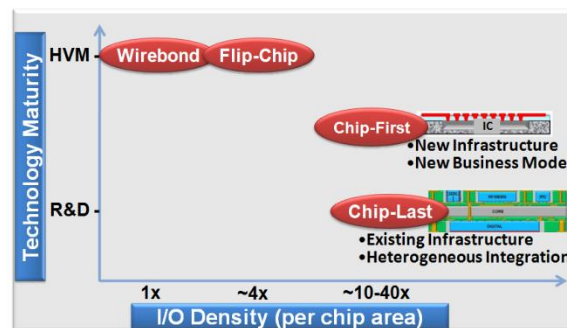

Figure 1: Two Approaches to Embedding- Chip-First and Chip-Last [3].

The Embedded MEMS, Actives and Passives (EMAP) Technology is being developed at GT-PRC with chip-last (CL) interconnections and chip-first benefits [4] to demonstrate ultra-miniaturized sub-systems with digital, RF, analog, Mems and sensor functions, through an industry consortium. Figure 1 depicts the chip-first and chip-last interconnection approaches to embedding as compared to existing flip-chip and wirebonding technologies.

Challenges in Chip-first Technologies

The biggest challenges [4] with chip-first technologies have been the yield of a functional and packaged embedded die, and the lack of "substrate" testability before packaging. These challenges become compounded for multi-chip packages and therefore, chip-first embedding is widely accepted as suitable for single chip packaging. If the embedded active device is a single chip package, it can be discarded. Chip-first technologies for embedded die in substrate suffer from lack of manufacturing infrastructure and product liability issues because ICs get assembled at package integrators which make it difficult to ascertain whether the yield loss is due to bad IC or thin-film package interconnections. Wafer-level fan-out embedding suffers from die shift and warpage resulting from molding while embedded-die in substrate suffers from die cracking and microvia misalignment which result in additional yield issues.

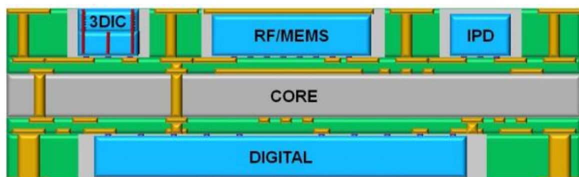

Figure 2: Georgia Tech's chip-last embedding approach.

What is Chip-Last Technology?

Figure 2 depicts the Georgia Tech PRC's chip-last embedding approach with digital, RF, MEMS and passive components. As the name suggests, chip-last technology is an embedding technology in which the last step deals with embedding one or more chips in the substrate at ultra-fine pitch and extremely low stand-off height, comparable to the chip-first mentioned above. While the concept is similar to flip-chip, the chip-last is about 10x smaller than flip-chip in interconnect dimensions. The fabrication process flow involves high density substrate fabrication to support I/O pitch down to 30µm, precise cavity formation, and chip placement and assembly. Such a process is expected to provide high I/O density comparable to chip-first technology and make complex multi-component integration possible with high volumetric efficiency while eliminating the above-mentioned challenges of chip-first such as yield loss, manufacturability, testability and manufacturing infrastructure.

The main advantages [4] of Georgia Tech's chip-last embedding approach include:

1. Known good substrate before assembly and functional test after assembly
2. Ultrathin subsystems, less than 0.3mm thickness
3. Double-side wiring and components due to through-package-vias
4. Repairability after assembly, if necessary
5. Ultra fine-pitch and ultra-short, chip-first like chip-to-package interconnections
6. Minimal change to manufacturing infrastructure
7. Precise placement of dies using current assembly processes and tools
8. Not limited by panel or wafer size due to the post placement of ICs
9. Allows for heterogeneous integration by embedded dies, thinfilm passives, IPDs and discrete passives with different thicknesses and materials
10. Top surface cavity allows MEMS device integration
11. Effective heat transfer due to the exposed die

This paper presents design, structure, materials and process details for four key building block technologies that enable chip-last integration- 1) the novel RXP core and build-up dielectric materials, properties, high density wiring and thermo-mechanical reliability studies, 2) high precision cavity fabrication process, 3) 30µm pitch chip-last interconnections and embedding, and 4) embedded RF filters and high frequency electrical characterization. The paper will conclude with results from a proof-of-concept demonstration of chip-last embedded actives and passives fan-out package in RXP substrates.

1) Core and Build-up Substrate

The key features of the EMAP organic substrates for chip-last embedding include: (1) thin package profile with halogen-free, ultra-thin core and build-up dielectrics, (2) high I/O wiring and dielectrics with fewest layers using ultra-fine pitch lines and vias, (3) low CTE and low moisture substrates for high reliability, (4) low-loss to GHz frequencies with heterogeneous integration of RF, analog and digital functions in a single package, and (5) ease of manufacturing and low cost by maintaining compatibility with current FR-4 manufacturing infrastructure.

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Two new dielectric materials [5], RXP-1 (core) and RXP-4 (build-up) in the RXP material system were used for embedding high Q RF passives and ICs by chip-last method. RXP-1 is a glass-reinforced high Tg (>300^0C), medium-CTE (10-15ppm/°C), and low-moisture uptake (<0.1%) laminate core in the thickness range of 50-110um. The RXP-4 is a 20um-thick unreinforced build-up film available as free standing film or as a resin-coated copper (RCF).The dielectric properties of RXP-1 and RXP-4 were characterized from 1GHz to 110GHz. A numerical based extraction method using corner-to-corner probing on a cavity resonator was employed for the measurements. The extracted dielectric constant of RXP-1 was 3.41+/- 0.06 with loss tangent tanδ <0.006 up to 110GHz. The extracted dielectric constant of RXP-4 was 2.98+/- 0.05 with loss tangent tanδ <0.005 up to 110GHz. The combination of the newly developed RXP-1 and RXP-4 provides a highly reliable, high performance low cost organic platform for wide band applications.

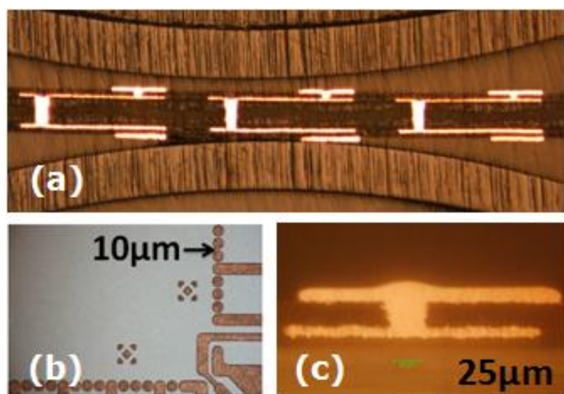

Figure 3: (a) Cross section of build-up substrate with 4 metal layers, (b) 10µm spacing to enable high-density routing, and (c) Cross-section of 25µm diameter Cu-filled blind micro-via.

To enable high density routing needed for assembling and escape routing of ultra-fine pitch interconnections, the fabrication process was optimized to demonstrate 10µm line width and spacing, as shown in Figure 3. In addition, Cu- filled through-vias as small as 40µm in diameter and blind microvias down to 25µm diameter were demonstrated for high density routing. These structures were subjected to MSL-3, 3x solder reflow and thermal shock test in air from -55°C to +125°C. Electrical continuity of the daisy chains was checked every 200 thermal cycles for assessing the reliability. Figure 4 shows the collected test data from 25µm blind vias on a test board, which contained 6,000 blind vias [3]. The vias performed exceptionally well during the reliability testing indicating that the low moisture RXP material has very low failure rate.

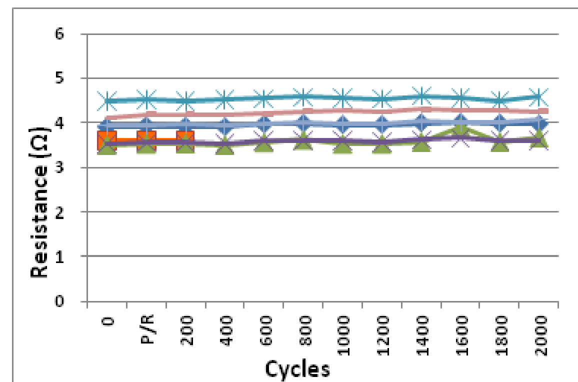

Figure 4: Collected test data from 25µm diameter blind vias.

2) *High Precision Cavity*

Highly-precise cavities matched to die thickness are a critical element for the success of chip-last embedding. In addition, the cavity fabrication process needs to be compatible with industry standard high throughput methods. In current work, cavity fabrication was explored by various processes such as laser ablation, plasma processing and photo-lithography. A comparison of precision, throughput, infrastructure compatibility and ease of fabrication for all three approaches was used to down select laser ablation as the primary approach.

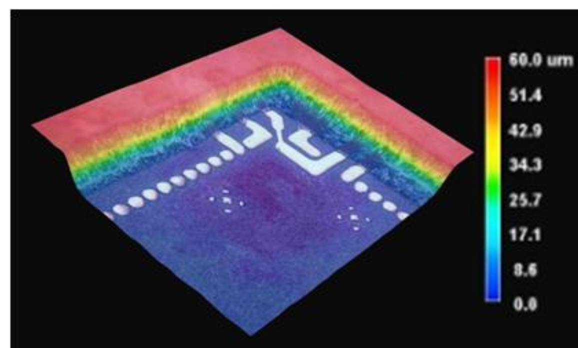

Figure 5: 3D image of one corner of laser ablated cavity in 60µm thick RXP-4.

High-precision cavities with chip-to-cavity clearance as small as 50µm were fabricated in 60µm thick RXP-4 dielectric by CO_2 laser processing. In addition to single cavities for 3mm x 3mm and 7mm x 7mm ICs, other cavity structures were evaluated including neighboring cavities for embedding two 3mm x 3mm ICs, one large cavity for embedding two 3mm x 3mm ICs, and cavities on top and bottom side

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of the core for embedding two 3mm x 3mm ICs. Figure 5 shows a 3D image of a corner of CO_2 laser-ablated cavity in RXP-4 after laser and post-ablation cleaning processes to expose the fine-pitch metal pads inside the cavity. After cavity fabrication process optimization, Cu pads of 30-50µm pitch were successfully demonstrated with no damage from the laser ablation process. The fabrication process was further optimized by using a laser-stop layer to achieve <2µm depth variation at cavity bottom.

3) Ultra-Fine Pitch Interconnections

Chip-last technology provides the flexibility in the choice of interconnection materials, processes, geometries and structures. In this work, interconnections were formed using copper bumps fabricated at ultra-fine pitch of 30µm with bumps of ~15-16µm diameter and 5-12µm height to enable ultra-high density I/Os and minimize interconnection parasitics.

Electroless-Nickel Immersion-Gold (ENIG) was used as the surface finish on both the die bumps and the substrate pads in order to prevent surface oxidation of copper. Two assembly loads (14N and 21N), two adhesive materials (NCF and nano-ACF with nano-silver as conducting filler) and two structures (cavity and non-cavity) were investigated for reliability performance under High Temperature Storage Test (HTS), Highly Accelerated Stress Test (HAST) and Thermal Cycling Test (TCT).

The assembly process involved pre-bonding of nano-ACF or NCF to the substrate at 90°C, followed by removal of nano-ACF or NCF carrier. After alignment of the die and the substrate, thermo-compression bonding was performed with 14 or 21N load at 160°C for 3-30 seconds. The reliability test conditions were based on JEDEC standards and mobile-product package test conditions.

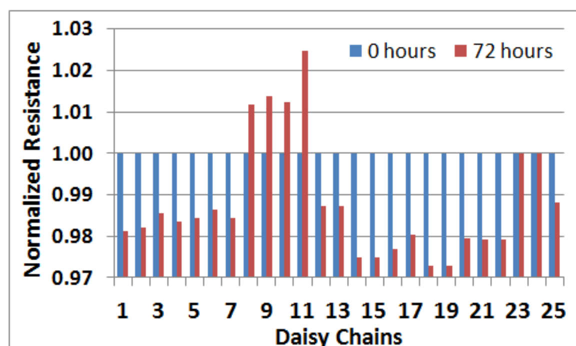

Figure 6: Normalized resistance for 25 daisy chains during HTS testing.

When subjected to HTS testing (72 hours @ 175°C), samples exhibited no failures and the resistance change was within ~3% [6] of the as-assembled resistance as shown in Figure 6. In addition, most daisy chain showed a decrease in resistance, which could be attributed to further curing and shrinkage of the adhesive materials during HTS. These results indicate that the interconnect scheme developed in this project shows excellent reliability during HTS test.

Moisture-induced hygroscopic swelling has been widely reported in the literature, as the primary failure mode for assemblies with adhesives [7][8][9]. In this work, the samples subjected to HAST (96 hours @ 130°C and 85% RH) test showed negligible increase in resistance and no moisture ingress or delamination, as shown in Figure 7. These results depict the robustness of Cu bump interconnect with nano-ACF/NCF.

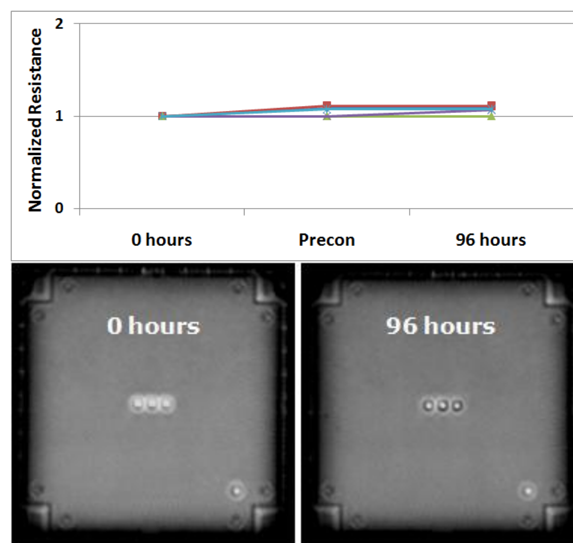

Figure 7: Daisy chain resistance and C-SAM images for a test package subjected to HAST.

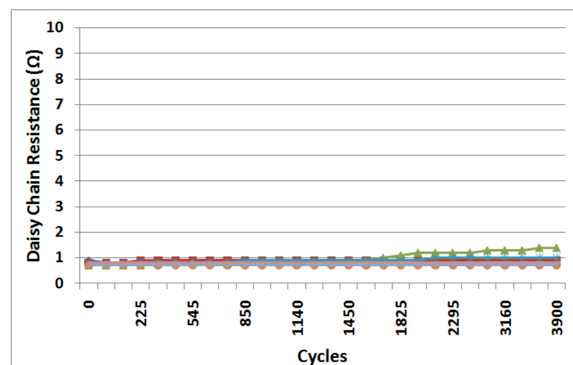

Figure 8: Daisy chain resistance of a test package during thermal cycling.

The TCT performance (-55°C to 125°C) of the assemblies was also found to be excellent [10]. Figure 8 shows the daisy chain resistance values of a test assembly through more than 2000 cycles. As is

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evident from Figure 8, the resistance changed marginally after 1800 cycles and the samples survived more than 4000 cycles, emphasizing excellent resistance of the chip-last interconnections for thermal cycle fatigue.

4) Embedded RF Filters

Lowest volume 2.4GHz bandpass filters with size of 2.2mm x 3.0mm x 0.2mm (1.2mm^3) were integrated in ultra-thin 4-metal layer, low-loss RXP substrate. Insertion loss of less than 2.2dB, return loss of greater than 15dB at 2.4GHz and attenuation of greater than 30dB below 2.0GHz and at 4.7GHz were measured [11]. Similarly, 5GHz filters with insertion loss of less than 1.2dB and with rejection better than 30dB were integrated, as shown in Figure 9.

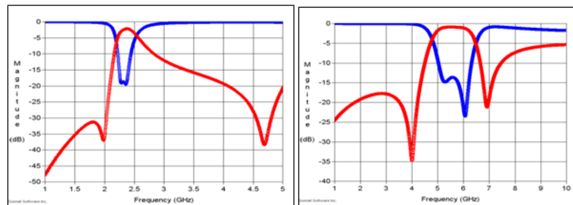

Figure 9: Measured data for representative 2.4GHz and 5GHz bandpass embedded filters.

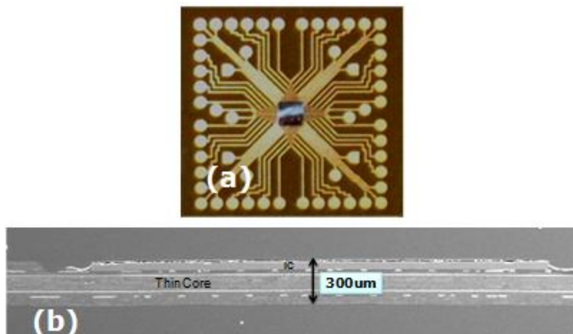

Figure 10: (a) Top view and (b) cross-section of 55µm thick embedded IC in <300µm thick organic substrate by chip-last method.

Chip-Last Embedding Demonstration

The four chip-last technologies described above were integrated in demonstration test vehicles to evaluate their compatibility with each other [4]. The first demonstrator of chip-last embedded IC in ultra-thin organic substrates is shown in Figure 10. The substrate core was made of a low loss, 110µm thick RXP-1 laminate, while the dielectric was made of a 20µm thick RXP-4. The bonding of ICs was accomplished at 30µm pitch using Cu-to-Cu interconnection with non-conductive adhesive at 160°C.

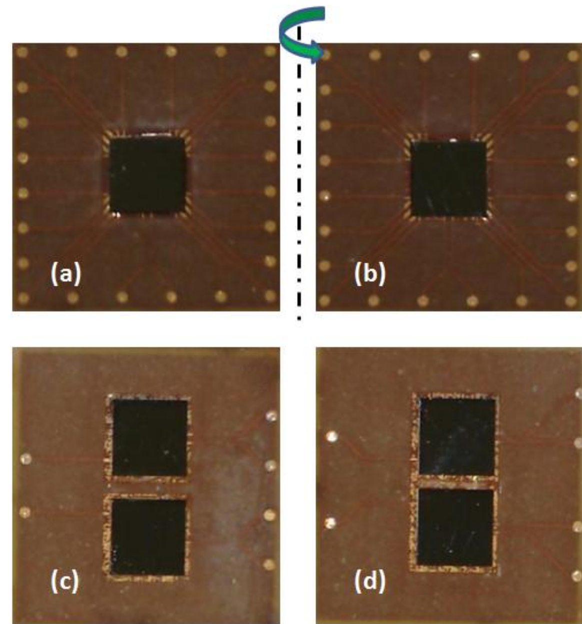

Figure 11: (a, b) Two ICs embedded on opposite sides of package, (c) Two ICs embedded in neighboring cavities, (d) Two ICs embedded in the same cavity

As mentioned earlier, one of the several benefits of chip-last technology is heterogeneous integration of multiple ICs. As a proof-of-concept demonstration for the same, various multi-chip packages emulating potential integration scenarios were fabricated using chip-last technology, as shown in Figure 11. The scenarios demonstrated, include 1) two ICs embedded in neighboring cavities, 2) two ICs embedded in the same cavity, 3) two ICs embedded on opposite sides of package, and 4) a large IC assembled on an embedded, smaller IC. These demonstrators reinforced the simplicity of the chip-last process and its ability to achieve highly miniaturized complex sub-systems and systems.

Conclusions

A new generation of embedding technology for actives and passives with chip-last methodology has been demonstrated for interconnecting ultra-fine I/O pitch (30-50µm) ICs. The chip-last approach goes well beyond leading-edge flip-chip interconnections in both pitch and stand-off height and beyond chip-first in testability, yield, ease of manufacturing and complex multi-component integration. Advanced materials and processes for chip-last embedding such as low-loss and low-moisture uptake RXP materials, semi-additive plating of 10µm conductors, copper filled through vias and blind vias of 30µm diameter, high precision laser cavities, and 30µm pitch Cu-to-Cu interconnections with 10-15µm profile were

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developed. Thin (55μm) Si test chips and high quality factor RF filters at 2.4GHz and 5GHz were embedded in 6-metal layer RXP substrates with total package height of less than 0.3mm. The chip-last embedded active and passive module technology described in this paper is a promising technology for highly functional, ultra-miniaturized and low cost mixed signal systems.

In summary, GT-PRC has demonstrated a novel, simple, highly-miniaturized and easily manufacturable chip-last embedded IC technology for single and multi component integration at package level with chip-first benefits.

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