Fast and Accurate Multi-Layer PDN Analysis for Power Integrity and EMC

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Introduction

Rapid power distribution network (PDN) analysis for complex printed circuit board (PCB) stack ups is very important to insure proper functioning of the PDN.

While there are a number of software tools and techniques to provide fast analysis of a single power/ground pair of planes, they are based on two dimensional analysis. Adding the third dimension usually requires a fullwave approach, making the solution time unacceptably long for real world PCB sizes with complex plane shapes.

This work uses a cavity resonance technique to solve each pair of planes in turn. Then, using analytical formulas to calculate the capacitance between vias (used for power or ground connections), the individual pairs can be combined to give the overall response of the entire complex PCB. Coupling from one power island to another power island on the same or on a different layer (for example, a 12 volt supply to a 1.2 volt supply) can be quickly analyzed and includes the via-to-cavity, via-to-via, and cavity-to-cavity coupling.

Cavity Resonance Theory

The cavity resonance method [1-2] assumes the power plane and ground-reference plane create a cavity where the electric field does not vary in the vertical direction, and does vary over the length and width of the planes. All resonant modes are summed for all locations between the planes assuming perfect magnetic conductor boundary conditions at the edges of the planes (i.e. there are no fringing fields). Capacitors and observation ports may be placed anywhere on the PDN and the capacitor's connection inductance, ESL, and ESR can be included. Rectangular and triangular shapes may be combined to create complex shapes. A circuit representation can be derived from the cavity resonance formulation, with a tank circuit for each resonant mode, which allows the PDN behavior to be coupled with driver and receiver models in a more complex SPICE simulation. Lastly, voltages can be calculated anywhere in the cavity, which enables the generation of a contour plot of the voltage distribution on the PDN for a given frequency.

A full derivation and description of the mathematics behind the cavity resonance method is beyond the scope of this paper, but a brief overview will be given here. Basically, in thin, parallel plate structures like the power/ground plane pairs in circuit boards and IC packages, a cavity is formed that only supports variation in 3 of the 6 electromagnetic field components. This reduces the computational intensity required to simulate the structure and allows a more efficient solution of the field distribution in the cavity. The form of the solution depends on the boundary conditions used and the shape of the power/ground plane pair. For regular shapes, like rectangles and isosceles right triangles, a closed-form expression can be found that captures the full-wave behavior.

For illustration, the case of a rectangular power/ground plane pair is discussed. A rectangular power/ground plane pair that is composed of two parallel, solid metal planes of size ***a*** by ***b*** that are separated by a dielectric layer whose thickness ***d*** is electrically small (as shown in Figure 1) can be modeled as a TM_{z0} mode electromagnetic cavity with two perfect electric conductor (PEC) walls (top and bottom walls) and four perfect magnetic conductor (PMC) sidewalls.

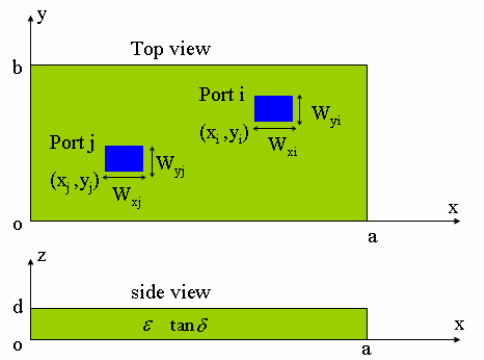

Figure 1. Via model for one signal via and one ground via in a plane pair.

Inside a TM_{z0} mode electromagnetic cavity, only the E_z component and H_x and H_y components are non-zero. These field components are also uniform along the z direction, and therefore the port voltage and port current are well defined at any x-y location in the cavity.

To calculate impedance of a irregularly-shaped planar power bus, a segmentation technique is used, combined with the cavity resonator model of a rectangular-shaped parallel plane pair. In the impedance expression below for a rectangular plane pair, each individual term in the series summation represents an individual resonant mode of the cavity. The first term with the mode numbers *m=0*, *n* = 0, is the impedance of the low-frequency inter-plane capacitance of the parallel plane pair. The sum of the remaining terms represents an inductive term.

$$Z_{ij}(\omega) = -\frac{j\omega\mu d}{ab}\frac{1}{k^2} + j\omega\left[\frac{\mu d}{ab}\sum_{m=0}\sum_{n=0}\frac{\varepsilon_m^2\varepsilon_n^2}{k_{mn}^2 - k^2} f(x_i, y_i, x_j, y_j)\right]_{m=n\neq 0}$$

$$= \frac{1}{j\omega\frac{\varepsilon ab}{d}} + j\omega L_{ij}(\omega) = \frac{1}{j\omega C} + j\omega L_{ij}(\omega)$$

where:

$$f(x_i, y_i, x_j, y_j) = \cos\left(\frac{m\pi x_i}{a}\right)\sin c\left(\frac{m\pi t_{xi}}{2a}\right)\cos\left(\frac{n\pi y_i}{b}\right)\sin c\left(\frac{n\pi t_{yi}}{2b}\right)$$
$$\cos\left(\frac{m\pi x_j}{a}\right)\sin c\left(\frac{m\pi t_{xj}}{2a}\right)\cos\left(\frac{n\pi y_j}{b}\right)\sin c\left(\frac{n\pi t_{yj}}{2b}\right)$$

As the formula shows, Z parameters can be calculated for each combination of observation ports at each frequency of interest.

This analysis approach has been validated against full wave tools [3].

Complex Model Assembly

The cavity resonance approach is used to find the impedance between a pair of planes (Z_{pp}). The capacitance between the via and the plane is added, as shown in Figure 2.

When multiple sets of power plane cavities need to be considered, ports can be defined where each via enters and exits each cavity. The input impedance of each port is a function of the capacitance between the via and the plane (across the antipad) and the input impedance of the power plane cavity (Z_{pp}). Multiple cavities are then combined by enforcing boundary conditions at each port-port interface and building a complete circuit of the entire stackup.

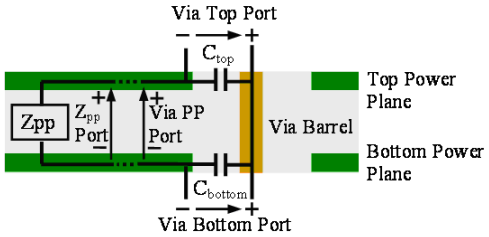

Figure 2 Building Block for each Layer of PCB

Initial PDN analysis

A 28 layer board is used for this example. There are nine ground-reference planes and six different power plane layers. The remaining layers are reserved for signals. Initially, the PCB stackup had a particular power layer on layer 16 and many power

and ground-reference pins in a dense pin field. Figure 3 shows an example of one of the dense pin fields for an IC to be analyzed. Each ground-reference via must be connected to all nine ground-reference planes, and the power vias are connected only to layer 16, and all other non-connected plane layers must be included in the analysis

The desired analysis was to show the effect of using layer 16 vs layer 3 (near the top of the stackup) as well as to show the effect of locating decoupling capacitors around the perimeter of the IC on the top of the PCB or locating the capacitors directly beneath the IC on the opposite side of the board.

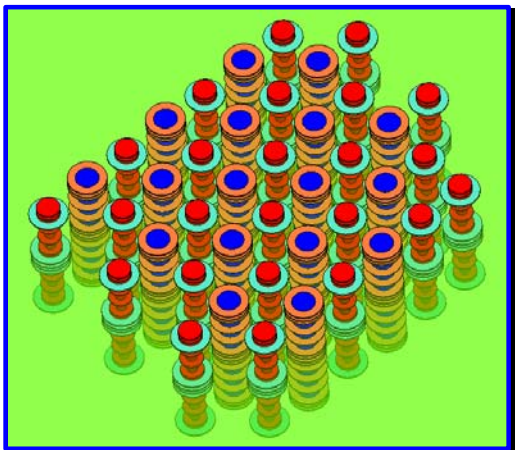

Figure 3 IC Via Array

Since this is a very complex structure to analyze, initially it was simplified to less complex arrangements of capacitors and vias.

Figure 4a shows capacitor/via configuration with a single pair of vias for the IC and a single decoupling capacitor[1]. The stackup for this case has the power plane on layer 16, as shown in Figure 5a. Power vias are shown in red and ground-reference vias are shown in blue.

[1] The values for the capacitor were selected so the total parallel capacitance, ESR and ESL were the same for the case of the single capacitor (1.7uF, 529uOhm, 49.4 nH) as when there were 17 capacitors (0.1uF, 9 mOhm, 0.84 nH each)

Figure 4b shows the configuration where a ring of 17 decoupling capacitors are place around the IC, but only one pair of vias are included for the IC. Figure 4c shows the configuration with 17 decoupling capacitors, and the IC has 17 power pins and 24 ground-reference vias.

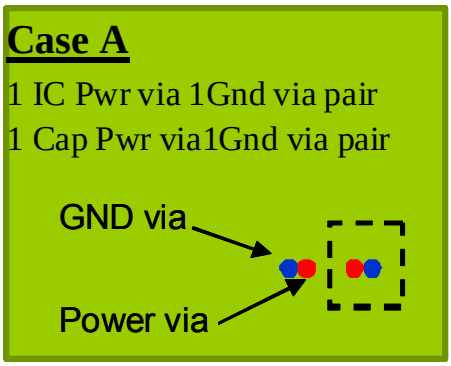

Figure 4a Initial Configuration

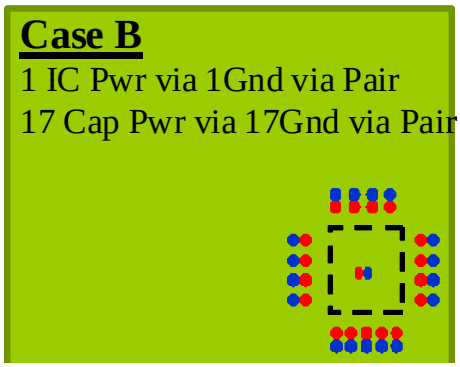

Figure 4b Configuration with 17 Capacitors

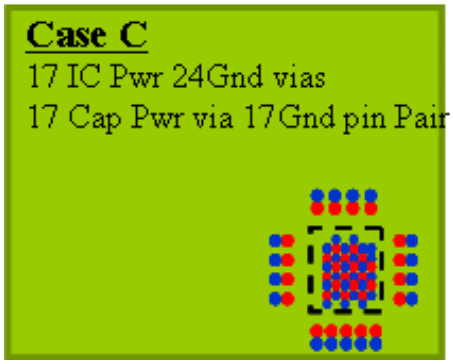

Figure 4c Configuration with 17 capacitors and many power/ground vias

Figure 6 shows the results from the analysis. Case A (one pair of IC vias and one capacitor) shows the highest impedance in the middle frequency range and shows high impedance at high frequencies. Case B (17 capacitors) shows lower impedance in the middle frequencies, but the impedance at high frequencies remains high due to the single pair of IC vias and the resulting high connection inductance between the IC and the power plane on layer 16.

Finally, Case C shows the lower impedance in middle frequencies (due to the capacitors) and lower impedance at high frequencies (due to the many power/GND vias connecting the IC to the power plane.

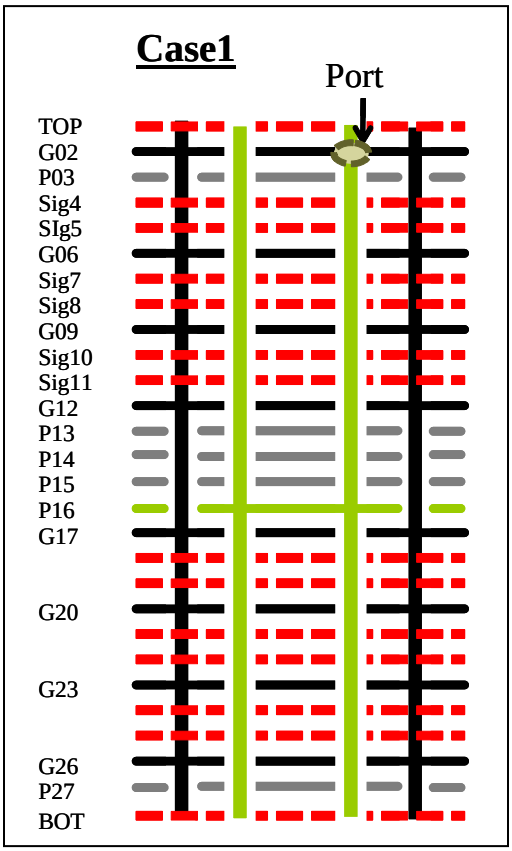

Figure 5a PCB Stackup with Power plane on Layer 16

PDN Analysis for Complex PCB

Once the relatively simple configurations were completed, the full desired analysis was performed. Figures 5a and 5b show the stack up configurations for the power plane on layer 16 (Case 1) and layer 3 (Case 2), respectively.

Figure 7a shows the 17 capacitors arranged around the perimeter of the IC, and Figure 7b shows the IC pin field with the capacitors located directly underneath the IC on the bottom of the PCB.

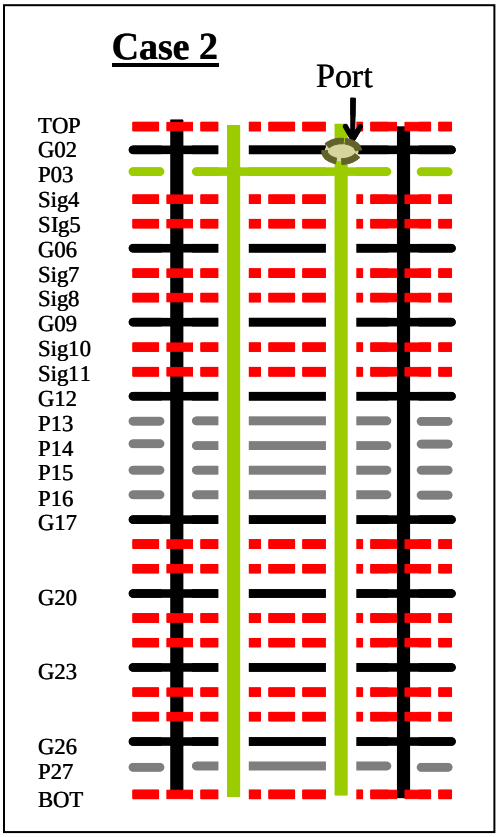

Figure 5b PCB Stackup with Power plane on Layer 3

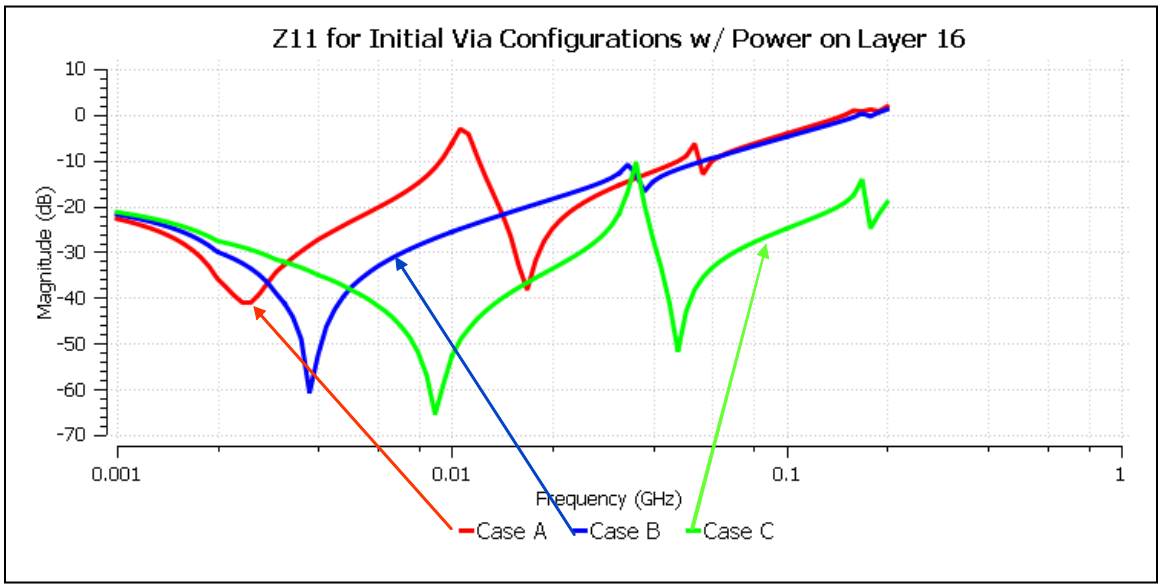

Figure 6 IC Port Impedance for Initial Configurations

Case A

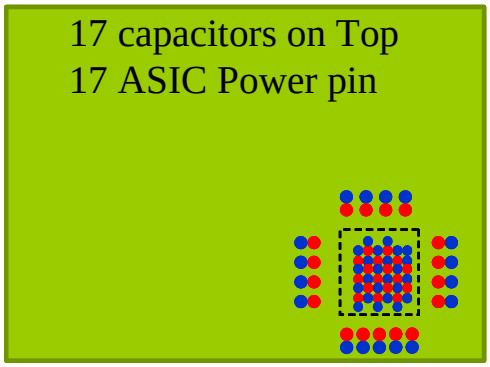

Figure 7a Capacitors placed on Top of PCB

The results from this analysis are shown in Figure 8. At low frequencies (below ~5 MHz), the capacitor dominates the impedance seen by the IC. Case 1A (power on layer 16 and capacitors on top) and Case 1B (power on layer 16 and capacitors on the bottom) both show higher impedances, especially at high frequencies. Case 2A (power on layer 3 with capacitors on the top) is the lowest (best) overall impedance across the middle and high frequencies. Case 2B (power on layer 3 with capacitors on the bottom) shows low impedance at high frequencies, but poorer impedance in the middle frequencies.

Case B

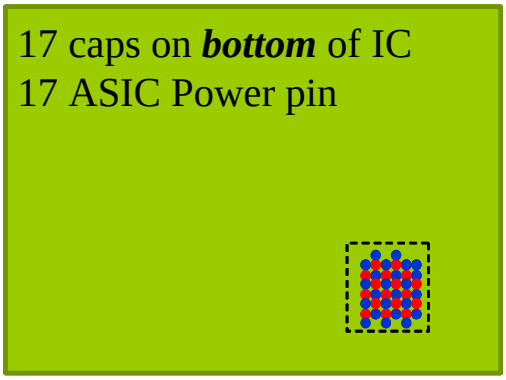

Figure 7b Capacitors placed on Bottom of PCB

From this analysis it is clear that it is better to place the power layer near the top layer for high frequencies when the IC is on the top layer. However, at high frequencies, the inductance of the connection of the capacitor to the power plane is too high for the capacitor to have any impact, and placing

them on the top or bottom has no effect at high frequencies. However, the location of the capacitors does impact the impedance at middle frequencies. When the capacitors are placed on the top of the PCB and the IC is on the top layer, the middle range of frequencies benefit from a lower impedance.

Summary

This work has shown that very complex via arrays, combined with many layers and cavities, and combined with many capacitors can quickly be analyzed using this technique. The simplest cases (which were still complex with many layers) solved in a few minutes, while the most complex cases with many vias and capacitors solved in 6-8 hours. Normal full wave tools would likely not be able to solve the complex problems at all, unless massive parallelization is used and extremely long run times.

References

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[2] G. T. Lei, R. W. Techentin, and B. K. Gilbert, "High-frequency characterization of power/ground-plane structures," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 562–569, May 1999

[3] Zhenwei Yu; Jun Fan; Connor, S.; Archambeault, B.; Drewniak, J.L., 'Modeling of noise coupling inside multilayer printed circuit boards using cavity model and segmentation technique', Electromagnetic Compatibility (APEMC), 2010 Asia-Pacific Symposium on Publication Year: 2010, Page(s): 321 – 324

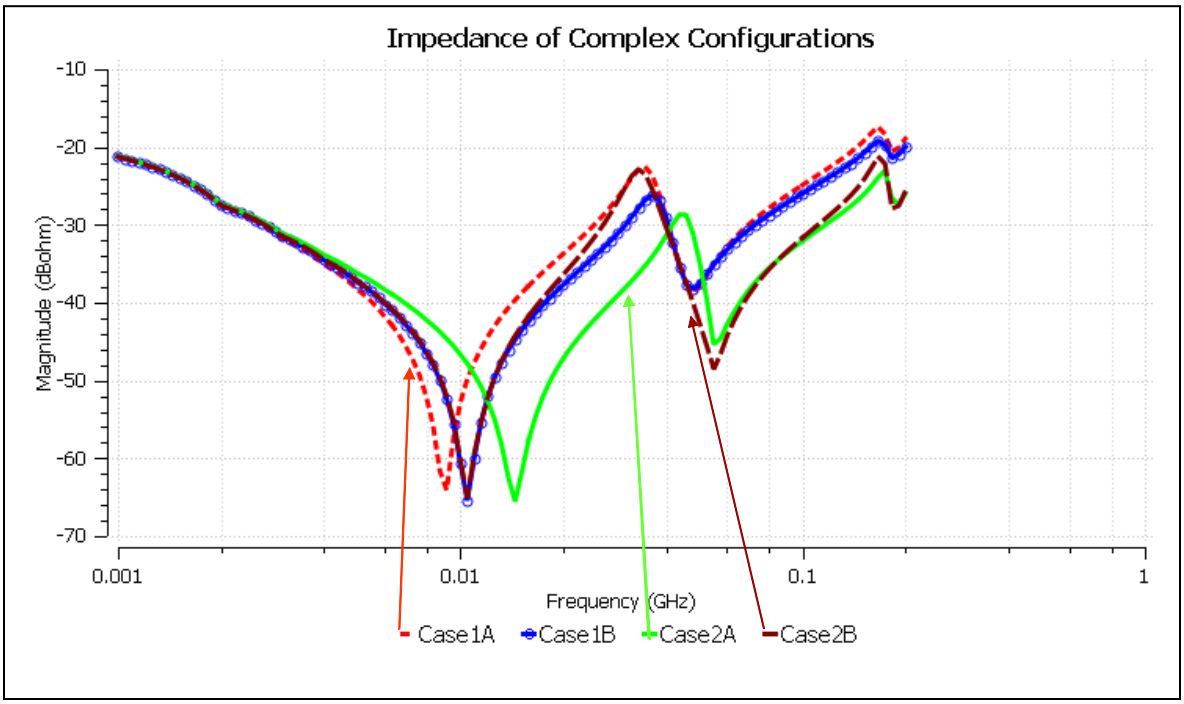

Figure 8 Impedance of Complex Configurations