Pinout Optimization for 10 Gbps+ Serial Link Routing

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Abstract

Definition and optimization a BGA (ball grid array) package pinout is a complicated process. Multiple factors must be considered, such as chip level floorplan, board placement of the component, the board stackup, escape routability, and signal and power integrity constraints. These tradeoffs and decisions impact package body size and board real estate, therefore overall system cost.

At high frequencies, such as >10 Gbps, the BGA to board via transitions cause visible impedance and noise mismatches and becomes a critical factor in the end to end channel design. Determining BGA pin assignments and their PCB transitions must meet the package crosstalk constraints within the required commodity PCB technology manufacturing rules. This paper describes a methodology of extracting 4 differential signal pairs in the board file from BGA ball to its PCB via transitions through BGA pin field into 3D field solver. The extracted geometry is simulated to determine near-end and far-end crosstalk noise levels between a single victim pair and its associated aggressors. Different pin assignment designs will have different number of aggressors to consider. Different routing layers will also produce different signal via stub lengths (specific resonant frequency) and signal via coupling contributing to far-end crosstalk noise. This may require back drilling of differential signal via stubs to minimize this noise.

The aggregated crosstalk noise level must be equal to or better than what the package can deliver. Once these design rules are determined, they can be leveraged across all channels running at the same frequency.

Introduction

Bandwidth across an interface is defined as the rate of data throughput. As the data rates of differential signals continue to increase, their rise and fall times subsequently increase proportionally to the clock period. The manufacturing tolerance deviation of the characteristic impedance of the transmission channel will result in reflection and crosstalk noise, causing loss of signal.

The channel can be decomposed to the chip to package transition, the package itself, the package to board transition, and the printed circuit board.

If separated into concatenated segments, the design deviation from the characteristic impedance of each section can be compensated in the design of the next section. This minimizes the overall impedance variations, but creates crosstalk noise, reducing overall signal-to–noise ratio and system performance.

The performance impact stems from reflection noise sources of such characteristic impedance discontinuities manifesting itself as crosstalk noise during signal via transitions. This effect can be minimized by greater physical separation between the signal pairs. Another strategy is placement of ground vias surrounding the differential signal pairs , which provides proper signal return paths (inductive path determining characteristic impedance of the via transition) and signal shielding isolating the pairs from each other. The number and locations of the ground vias are critical. The minimum number of return path ground vias for each signal via transition is two to balance the effect. Therefore a minimum of four ground vias are required for each differential signal pairs.

Modeling Methodology

A modeling methodology was developed to account for these interface discontinuities using a variety of commercially available tools. First, a three section model was developed:

1. Extract the package file (.mcm format) file from Cadence Allegro [1] into Ansys HFSS environment using AnsoftLinks [2]. This includes all aggressor nets and their associated power and ground references for the given victim net under study. Some modeling revision will be required after extractions to delete detached segments remaining from the original file.
2. Develop BGA (ball grid array) to PCB (printed circuit board) transition section. This includes BGA solder balls, mounting pads, dogbone dispersion traces on the surface layers, and signal/ground/power via transitions related to the extracted BGA balls.
3. Generate a model for the board stackup with respect to the via transitions, as described earlier.

In each section, geometric parameters and material properties such as the dielectric material for each layer, pad and antipad size for each via transition, and specific copper thickness, must be independently specified.

To optimize the design, each of the design variables in steps 2 and 3 above, should be parameterized. This is an option with the simulation structures manually built in HFSS. The extracted file from Allegro to HFSS using AnsoftLinks does not have that capability on its own.

Since different manufacturing ground rules apply to different designs and supply chain constraints, it is critical to choose the appropriate technology level for the cost optimized assembly.

As shown in Figure 1, this includes removing non-functional pads for signal via, minimizing via barrel size, maximizing anti-pad size for the signal via transition and minimizing signal pad sizes for optimal 50 ohm impedance match to the target characteristic impedance of a transmission line.

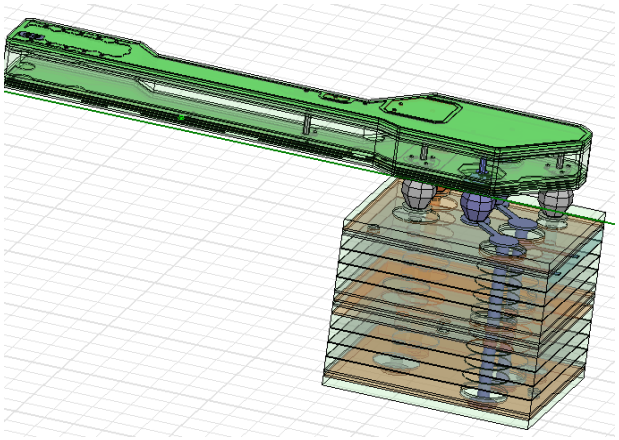

Figure 1: 3D BGA ball to board transition model.

The final segment of the design structure is signal via to differential signal trace transition. The goal is to minimize the effect of the signal via stub length and differential trace loss in the link model. One way to accomplish this is to exit on the bottom routing layer to minimize via stub length and short 50 to 100 mil trace lengths to minimize trace loss. Practically, there is a balance between minimizing trace loss (short traces) versus minimum trace length requirement to settle the excitation field from the source before it reaches an impedance discontinuity such as a via that reflects back the signal to the source and disturbing its behavior. The routing rule can vary depending on the impact of the via stub length when signals exit on different routing layers.

BGA escape study

When simulating the escape pattern from the BGA ball field to the board, a "checkerboard" pattern of PCB transitions was used for the crosstalk study, as shown in Figure 2.

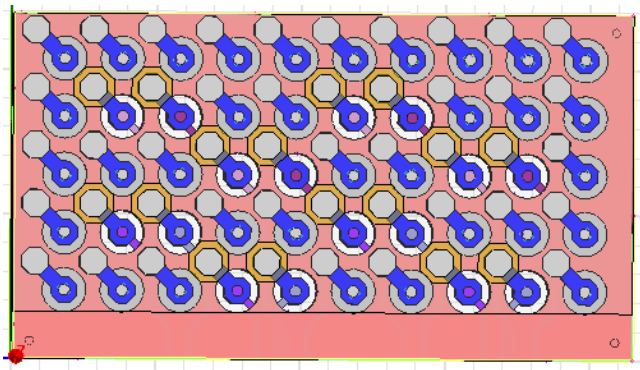

Figure 2: Checkerboard BGA pattern.

A Touchstone format [3] of as single ended s-parameter simulation model for each design condition under study is created after completing our simulations in HFSS. These S-parameter (Touchstone format) models are imported into Agilent ADS [4] in order to build a circuit level topology for cross talk noise level study.

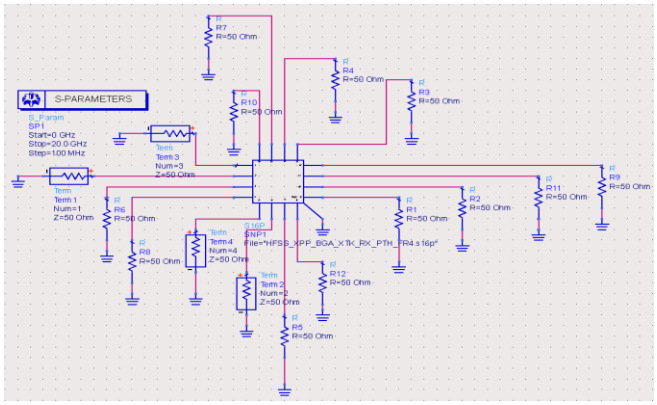

Figure 3: NEXT simulation for RX1 (victim) and RX0 (aggressor) nets in ADS.

Crosstalk is a proximity effect, a phenomenon caused by neighboring signals coupling to each other. This model allows deliberate assignment of which individual aggressor(s) can influence the victim. The individual crosstalk effects, nearend (NEXT) and farend (FEXT) of each aggressor, is calculated through the single ended to mixed mode conversion equation [5]. The magnitude of the NEXT depends on the mutual capacitance and inductance between the interacting lines, and increases to maximum amplitude as the coupling length increases until a saturation point. FEXT is an effect caused by the difference in velocity between the odd and even modes of propagation, which results in a reflected edge arrival at the end of the line. The best overall design will have the lowest aggregated crosstalk noise level from all the participating aggressors.

Figure 3 shows the NEXT simulation setup for the victim, RX1, and the aggressor net, RX0 (see Table 1a, 1b). Similar setup is arranged in ADS to determine the effect of aggressor net RX2 on victim net RX1. Then the total FEXT and NEXT noise contributions of the appropriate aggressor nets on a given victim net are calculated by adding all noise contributions for victim net RX1 (Table 3).

The NEXT and FEXT noise contributions for different victims; RX1 and RX2, are investigated with appropriate aggressors (Table 1a, 1b) and the results are tabulated in Table 3 in order to determine the worst case scenario noise levels.

Victim	RX0 NEXT	RX0 FEXT	RX2 NEXT	RX2 FEXT
RX1	-43.58dB	-51.48dB	-42.10dB	-46.42dB

Table 1a: NEXT and FEXT for RX0 and RX2 aggressor nets on RX1 victim net with staggered ball pattern.

Victim	RX1 NEXT	RX1 FEXT	RX3 NEXT	RX3 FEXT
RX2	-42.10dB	-47.13dB	-41.71dB	-47.97dB

Table 1b: NEXT and FEXT for RX1 and RX3 aggressor nets on RX2 victim net with staggered ball pattern.

Simulation results

Simulation results of two 1.0 mm BGA ball patterns of PCB transitions are presented, called a "checkerboard pattern", shown in Figure 4, and a "staggered pattern" illustrated in Figure 5. All the design parameters are kept consistent between the two patterns, so any differences in the model are strictly due to the BGA ballout and resulting escape route patterns.

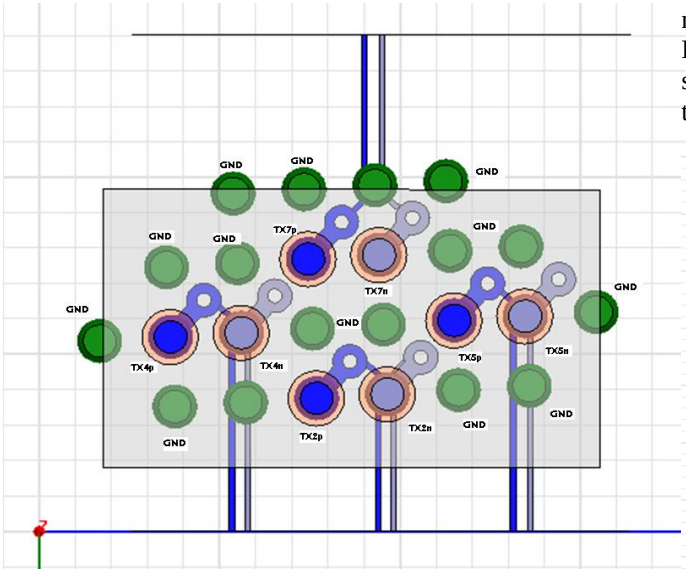

Figure 4: 2D "Checkerboard" pattern with TXn pair locations.

The checkerboard pattern has ground pairs in north, south, east, and west directions of each active signal pair. The closest active signal pair is on a 45° diagonal. An investigation for using low loss and Pb-free material such as Megtron-6 for 10Gbps+ applications was conducted, so the impact of NEXT and FEXT was quantified.

Material	FR-4	Megtron-6
SDD11@ 10 Gbps	-12.00 dB	-13.4 dB
TX2 & TX4 NEXT @ 10 Gbps	-44.27 dB	-45.17dB
TX2&TX4 FEXT @ 10 Gbps	-43.20 dB	-43.69 dB
TX2&TX5 NEXT @ 10 Gbps	-41.40 dB	-42.00 dB
TX2&TX5 FEXT @ 10 Gbps	-43.73dB	-44.47 dB
TX2 NEXT @ 10 Gbps	-36.7 dB	-37.4 dB
TX2 FEXT @ 10 Gbps	-37.4 dB	-38.0 dB

Table 2: NEXT and FEXT for checkerboard ballout pattern.

Table 2 shows the simulated NEXT and FEXT between different pair locations for two board materials, standard FR-4 (Dk=4.2, Df=0.02) and Megtron -6 (Dk=3.6, Df=0.002).

The effects of aggressor nets TX4 and TX5 on victim net TX2 on NEXT and FEXT noise are shown on the last two rows of Table 3 for comparing the difference between FR-4 and Megtron-6 board material. The differences are small enough to conclude that material impact in this investigation is minimal and can be ignored.

By contrast, the staggered pattern has a p- or n- from a neighboring signal pair adjacent in the north and south direction. East and west are adjacent to ground pairs. This gives better signal density, and can result in an overall smaller body size for the substrate.

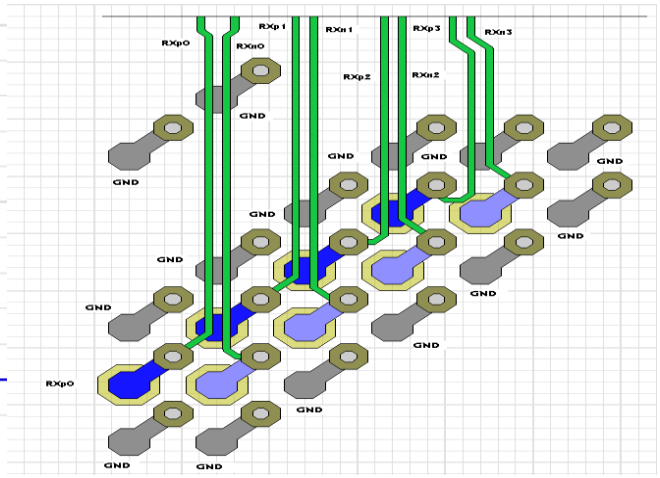

Figure 5a: 2D "Staggered" pattern with RXn pair locations.

Figure 5a shows a two-dimensional diagram of the staggered pattern with corresponding RXn pair pin locations. Figure 5b is the three-dimensional view of the board stackup and its four differential signal routings near the bottom layer 21 with approximately a 16mil via stub length. From left to right the signals are RXp0, RXn0, RXp1, RXn1, RXp2, RXn2, RXp3 and RXn3.

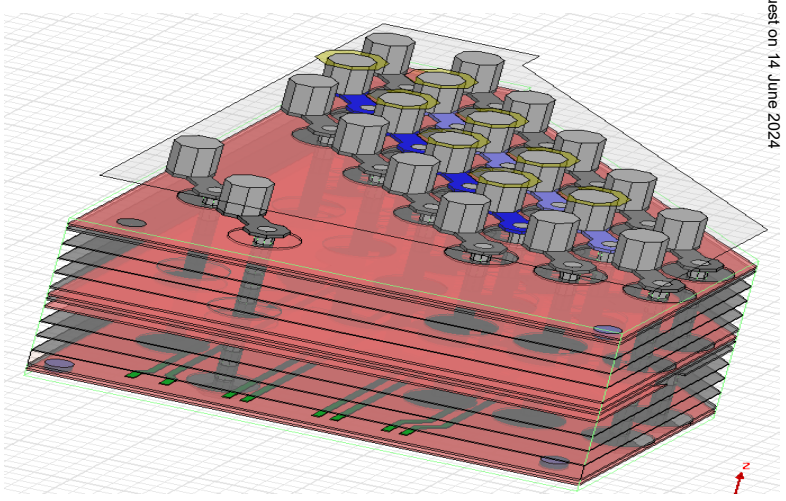

Figure 5b: 3D "Staggered" pattern with RXn pair locations

Table 3 combines the effects of two aggressor nets on selected victim net; RX1 or RX2 to determine the worst possible net for staggered BGA ball pattern. Note that due to number and locations of modeled reference grounds, the noise level may differ slightly between different selected victims as shown in the results.

Victim	NEXT @ 10Gbps	FEXT @ 10Gbps
RX1	-36.78 dB	-42.56 dB
RX2	-35.88 dB	-41.52 dB

Table 3: NEXT and FEXT for RX1 and Rx2 victim nets.

Table 4 shows the results comparison between the checkerboard and staggered design patterns in FR4.

BGA design	NEXT@10Gbps	FEXT @10Gbps
Staggered	-36.78dB	-42.56dB
Checker board	-36.7dB	-37.4dB

Table 4: NEXT and FEXT for staggered versus checkerboard BGA design patterns.

The NEXT noise level is approximately the same between the staggered and checkerboard BGA ball patterns. FEXT noise improvement in Table 4 is due to tighter differential signal via coupling between two pairs in the staggered BGA ball pattern versus the checkerboard pattern. This is valid only if there is no via stub resonance effect.

Table 5 shows the difference in NEXT and FEXT noise levels between long differential signal via transition (from top to near the bottom layer 21) and short differential signal transition (back drilled to layer 3) for the checkerboard BGA ball pattern in FR-4 material.

FR-4 checkerboard BGA	NEXT @10Gbps	FEXT @10Gbps
No back drill (L22)	-36.70 dB	-37.40 dB
Back drill (L3)	-45.69 dB	-53.07 dB

Table 5: Effect of back drilling on NEXT and FEXT.

NEXT and FEXT noise levels can be improved if the length of the differential signal via transition is minimized by backdrilling. This is true with any BGA ball pattern.

The next case study determines the effect of differential via stub resonant noise on NEXT and FEXT noise levels in the staggered BGA ball pattern. The query stems from establishing tighter coupling between differential signal pairs in the staggered BGA ball pattern that may be more damaging to the overall design if signal via stubs are allowed within signal transitions.

For purposes of this investigation, the nets RX0 and RX2 are rerouted on near the top layer 4 instead of near the bottom layer 21 without backdrilling (104 mil via stub length). Meanwhile RX1 and RX3 remain routed on layer 21 (16 mil via stub length) as shown in Figure 6. Because of the tighter coupling among differential signal pairs in the staggered BGA ball configuration, any via stub resonance from adjacent via will affect the crosstalk noise level detected.

Victim	RX0 NEXT	RX0 FEXT	RX2 NEXT	RX2 FEXT
RX1	-43.58 dB	-51.48 dB	-42.10 dB	-46.42 dB
RX1	-6.23dB	-36.38 dB	-26.62 dB	-44.74 dB

Table 6a: Effect of long via stub on NEXT and FEXT for the staggered BGA ball pattern at 10Gbps.

The higher susceptibility to via stub resonant noise in the staggered BGA ball configuration is demonstrated in the crosstalk investigation results shown in Tables 6a and 6b. In each of these two tables, the first rows are the crosstalk noise levels without via stub effect and the second rows are the effect of via stub resonant contribution.

Victim	RX1 NEXT	RX1 FEXT	RX3 NEXT	RX3 FEXT
RX2	-42.10 dB	-47.13 dB	-41.71 dB	-47.97 dB
RX2	-26.62 dB	-44.74 dB	-6.09dB	-37.35 dB

Table 6b: Effect of long via stub on NEXT and FEXT for Staggered BGA ball pattern at 10Gbps

The NEXT noise level increase due to via stub between RX1 and RX2 are similar and as expected. The FEXT noise level increase due to via stub effect varies between the nets and is dependent on the via stub length of the victim. Increasing the size of the simulation structure adds more space between the simulation boundary and via transitions on the edge of the model when the via stub effect is present.

Stub length depends completely on the board stackup and what layers the signals are routed on. The long via stubs in the staggered BGA case are shown in Figure 6. The board stackup layers are removed to show differential routings and their via stub lengths for clarity.

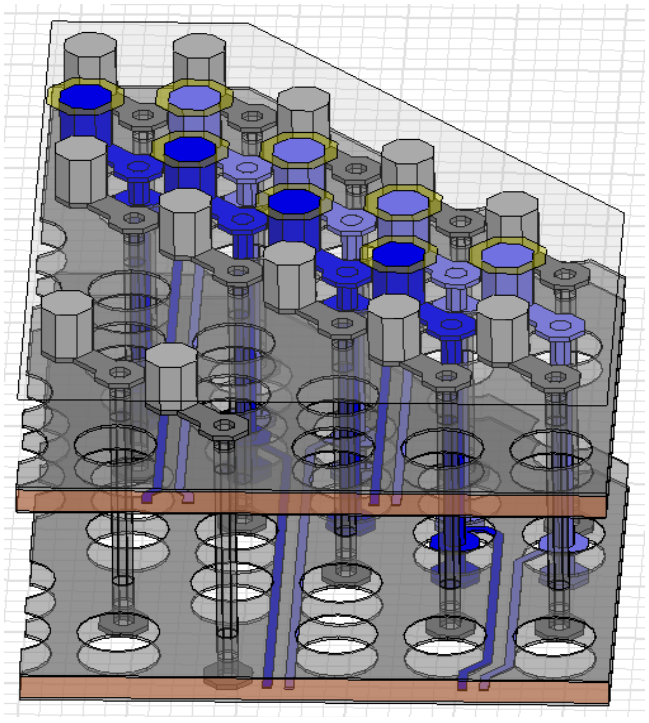

Figure 6: Solder balls with pads and via transitions

The insertion loss plots of these 4 differential signals are illustrated in Figure 7. RX1 and RX3 insertion loss are approximately 0.5 dB at 5 GHz with no frequency resonance. In contrast, RXp0 (high lighted in blue color) insertion loss is approximately -1.5 dB with resonant frequency around 9.5 GHz. Note that despite RX0 and RX2 have the same via stub lengths, the insertion loss value and the resonant frequency of RX2 and RXn0 are different. This difference is due to RXp0 having different number of supporting reference ground near the edge as shown from Figure 5a and Figure 6. This difference becomes evident when comparing supporting reference ground balls between RX0 and RX3 on the two extreme edges of extracted geometry in these figures. The same geometry difference is the primary contributor to the crosstalk noise level difference observed in Table 6a (-6.23dB) and Table 6b (-6.09dB).

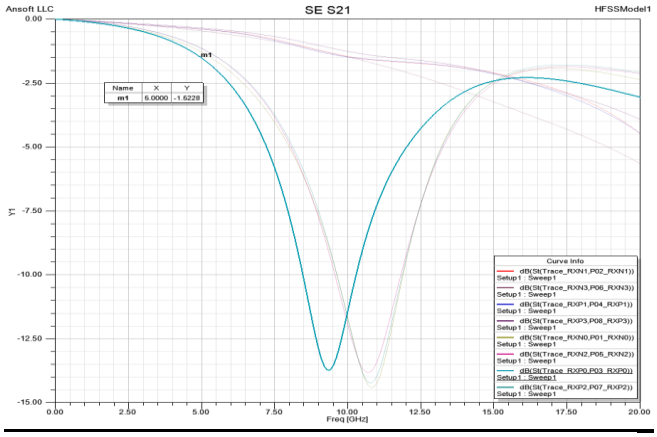

Figure 7: S21 frequency plot of RXp0 (in blue), RX2 (via stub resonance), RX1 and RX3

Conclusions

1. The simulation structures were built for three row deep signal with only two potential aggressors. Additional signal row will increase overall NEXT and FEXT accumulated noise level of our simulated structure. Differential signals will have slightly different behavior depending on their location in the device such as edge of the package.
2. Board material made about 1 dB difference between standard FR-4 and Megtron 6 in a checkerboard BGA ball pattern simulations. This may be different with a staggered BGA ball pattern.
3. In a checkerboard BGA ball pattern, the signal via transition contribution to crosstalk noise was approximately 16dB. We can gain this by backdrilling.
4. The full via board transitions vary by 5 dB between the checkerboard BGA ball pattern and the staggered BGA ball patterns for differential FEXT.
5. Via transition stubs have a noticeable impact on crosstalk noise levels and increase in the BGA ball to board transition. This was observed in staggered BGA ball transition.
6. Minimize signal via transition length by backdrilling which lowers crosstalk noise between adjacent differential pairs.
7. Even though not modeled in this paper, creating reference plane voids under surface BGA pads for high speed differential signals will improve return loss. These reference plane void shapes are about 2 mils wider diameter than BGA pad diameters. The actual size will vary with each board stackup. The reference plane voids are limited to a handful of critical high speed signals only since too many holes in power/ground planes under a device is undesirable for power integrity reasons.
8. Based on the IEEE 802.3ap 10GBASE-KR standard [6], 25 dB of loss is acceptable at 10 Gbps. The checker-board BGA ball pattern will have (36.7 dB – 25 dB) = 11.7 dB signal-to-noise performance. The actual length of the achievable channel in this case is related to the material selection (FR-4 or Megtron-6). To improve the calculated SNR for checkerboard BGA ball pattern, short signal via transitions and backdrilling should be considered. Backdrilling will increase the SNR for the checkerboard BGA ball pattern channel to (45.69 dB – 25 dB) = 20.69 dB.
9. The overall signal-to-noise ratio improvement in an end-to-end channel design is related to both reducing the noise as presented in this paper as well as minimizing the signal loss. The signal loss is determined by both dielectric material loss of selected board material (even though it had minimal effect in our BGA ball design study given our selection of materials) and skin effect loss due to copper foil surface roughness at 10 Gbps and beyond. It is important to consider the impact on system performance and cost tradeoffs when design decisions are made.

References

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[4] Agilent Advanced Design System®, rev 2009, 3.5.0.0, 2010.

[5] Application number: 9/954,962, Publication number: US 2002/0053899 A1, Filing date: Sep 18, 2001, Issued patent: 6653848 (Issue date Nov 25, 2003).

[6] IEEE Standard 802.3ap™- 2007 (Amendment to IEEE Std 802.3™ - 2005), (72. Physical Medium Dependent Sublayer and Baseband Medium, Type 10GBASE-KR).