High via density thin metal-core PCB using electro-coated dielectric

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Abstract

Conventional printed circuit boards (PCBs) may be replaced by thinner metal-core boards for some applications, as well as for package substrates. Using thin, metal-core technology may provide advantages for radio frequency (RF) circuits and packages, and increase heat dissipation for high power applications.

The metal-core technology has several layers including the metal core, electro-coated dielectric, sputtered metal layers, and electroplated copper. Especially for RF application and automotive electronics printed circuit boards with a metal core is gaining interest. The advantage of metal core PCB is the low thermal coefficient as well as the possibility to achieve a high density of vias and electronic component assembly.

This paper describes the realization of metal core PCB with a dense array of vias and with a low thermal coefficient . The dielectric layer is applied after vias have been formed providing a high density electronics assembly on a double sided PCB which exhibits the heat dissipation of a metal core with minimal thermal expansion. After photo-chemically etching an array of vias, the metal core can be optionally plated with copper. The insulating dielectric is applied using a highly reliable electro-deposited coating. Metal core substrate provides the opportunity to form a via to the metal core to provide electrical grounding. The final traces are fabricated on top and bottom and can be interconnected through via openings.

Keywords: High density via, Metal core PCB, electro coating, dielectric, package substrates, heat dissipation, chemical etching, RF

Introduction

The objective of this project is to increase Vertical Interconnect Access (vias) density of four fold from approximately 400 vias/cm^2 to approximately 2500 vias/cm^2 by using METCORE™ technology. This increase in vias ≤ 75 µm provides an increase in density in chip design which causes the chips to overheat. It is needed to have a chip packaging substrate which has a coefficient of thermal expansion close to that of the chip to eliminate failure and minimize stress. Also, it is needed for the substrate to have a high heat spreading capability in order to avoid excess heat build-up on the chip.

Goal

The goal of this work is to establish a full capability which will allow the development, testing, and validation of ultrathin METCORE™ substrates with high via and wiring density that are HVM compatible.

Goal for the viability of thin metal film core with conformal dielectric coating is to confirm the feasibility of preparation of thin film substrates with high density vias, and to determine the formulation and application parameters necessary for a successful conformal dielectric coating on the thin film substrates with high density vias.

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In order to achieve facile processing of ultrathin packages of less than 100 µm (as low as 70 µm) and via diameters of less than or equal to 75 µm, a new simplified process will be required. This process requires eliminating and reducing the thickness of several of the design steps mentioned above without compromising key properties such as interfacial adhesion.

Design Method

Design method for the MetCore process flow is a six sub-level layer, in which high density wiring is created between two layers and the two layers of the package. Once the layers are completed, the typical total substrate thickness should range between 200 – 250 µm.

Invar Stock

The supplied invar specimen was a 0.004” foil with a thickness varying from 100 - 125 µm. This Invar stock gets patterned and copper plated with a thickness between 25 – 50 µm, depending on the researcher’s traveler. Once the plating is completed, the Invar receives a dielectric (DE) application. This application starts with a pretreatment, followed by the dielectric application which is done by an electrophoretic coating technology. This process deposits the film conformally to the substrate providing a uniform coating to the surface of the package as well as the interior edges of the vias and all other features. Once the dielectric is deposited on the film, the entire substrate is cured. Once the previous process is finished, circuitry is created on the surface of the substrate with the vias providing electrical contacts between the top and bottom layers, with a thickness about 50 µm. To achieve this result, an adhesion later is sputter deposited on the surface of the substrate. The sputtered layer has a thickness of < 0.1 µm. The circuitry is formed by either partially additive technology or subtractive technology. The circuitization layer is of 25-50 µm thickness. The finished process has a substrate thickness between 200 – 250 µm, depending on the thickness of copper plating treatment and dielectric application.

For the copper stock, the process remains the same except it is not necessary to do a copper plating process

Experimental Details

Laser

Evaluations were conducted on 3 in. x 6 in. pieces of 1 mil invar. A Trumpf 532 nm wavelength green laser was used to etch the

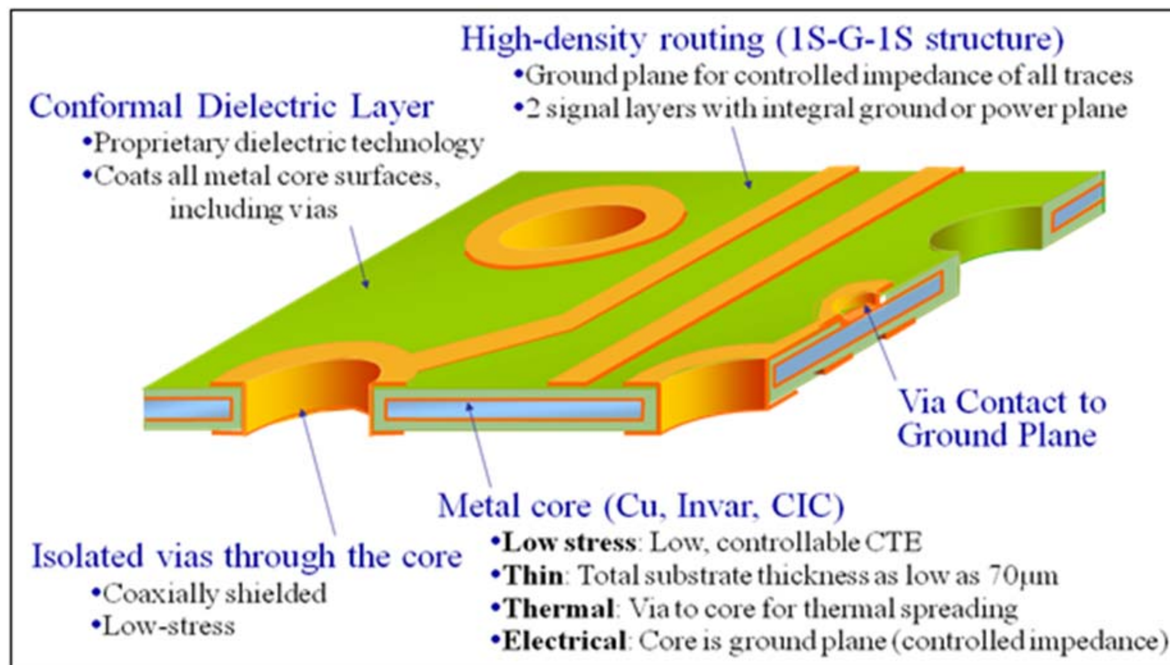

Figure 1: METCORE™ Structure [PPG Industries Inc.]

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features. Table 1 lists the parameters used by the laser. The item "Multiple Markings" in the table indicates the number of times a pattern is repeated in the same location to realize the desired definition and depth. Spot size is the size of the beam at its focal point. Power is a setting ranging from 0 to 100 percent for poser. The value of 100% is on the average equal to 4 Watts emitted form the laser. Velocity is the rate at which the focused beam traverses over the sample. Depth is the distance the laser etches into the invar. Pulse frequency is the number of pulses per second the laser emits. Fill-out spacing is the distance from one laser line to the next set up to ablate the area. [16]

I) Characterization of laser parameters to decrease invar deformation and discoloration

Many parameters dictate the characteristics for laser-etching invar. Beam width, pulse frequency, power, travel speed, and focus are some of the main parameters that characterize how the invar material is drilled. [16]

Power, pulse frequency, and multiple markings constituted most of parameters that needed to be optimized. Coincidentally, power output depends on the pulse frequency. Values for power and energy were provided by Trumpf Inc. and are shown in Table 2.

The testing of the high density vias started with the creation of multiple via designs. These designs implemented numerous different via sizes, tolerances, and pitch lengths. This design criterion allows for multiple test results in which to optimize via density to an optimal 2500 vias/ cm^2. (Figure 3 illustrates one pattern used as the via design.) Again this difference in size, tolerance, and pitch length must be a variable parameter which can be modified depending on the DE application and copper plating. (These dimensions are explained in Figure 2.)

Table 1: Parameters for the Trumpf laser marker

Constants	Abbreviations	Units
Multiple Markings	MM	
Width or Spot Size	s	μm
Power	P	%
Velocity	v	μm/s
Depth	Z	μm
Pulse Frequency	pf	kHz
Fill out Spacing	fs	μm

Table 2:
Trumpf laser power data from Trumpf Inc.

	Energy	Pulse frequency
Pulse Energy:	0.17 mJoules	20 kHz
	0.12 mJoules	33 kHz
	0.05 mJoules	60 kHz
Pulse Peak:	8.6 mJoules	33 kHz

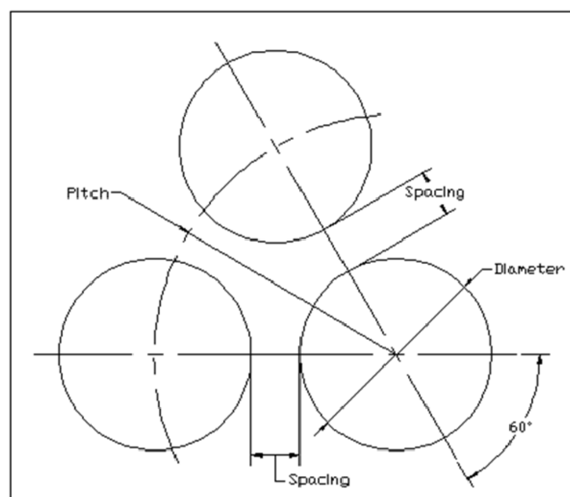

Figure 2:
Explained dimension of optimized design

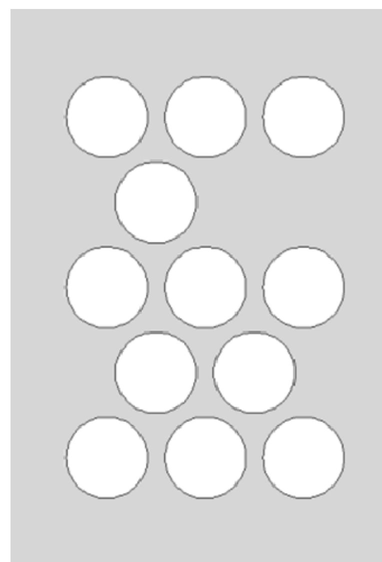

Figure 3:
Pattern used to increase number of vias/cm^2

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Once the DE is applied and the copper plating occurs, the diameter of the design via will be reduced, thus this must be taken into consideration when deciding upon dimensioning.

Initial tests were run on 5 mil Invar sheets. The 5 mil Invar was used strictly for preliminary tests to set up a baseline procedure for future tests. This thickness of Invar caused difficulties when developing the patterns using the Trumpf Laser. The thickness required multiple markings on each feature over 120 times. These multiple markings were time consuming, deformed the invar, and distorted the vias, as seen in Figure 4. The resulting Invar results varied due to these difficulties, thus the testing was moved to a 1 mil Invar sheet.

The 1 mil invar provided a faster development time, cleaner surface finish and fewer non-finished vias. This 1 mil invar is a much thinner sheet thus causing easier surface deformation. This can be limited by using a thin, level sheet of Polyimide underneath the invar during testing. The results of the 1 mil invar were much better than the 5 mil, the vias were cut more precisely with less erosion and discoloration around the vias, and via dimensions were much more consistent as seen in Figures 5 and 6.

Dimension of our theoretical design strongly correlated to the experimental dimensions. This was partly due to the precise laser capabilities of the Trumpf Laser. Also, the thin invar is a material which is widely used for precision instruments and areas where dimensional stability is of prime importance.

Discoloration around the pattern (as shown in Figure 5) has caused a concern, mainly due to invar deterioration in the future. This has been chemically treated using a series of etching and cleaning operations. This process removes almost all discoloration and reduces chances of future product failure once assembled for production. (Refer to Figure 6). An effort will be made to refine the process to alleviate this effect. Alternate lasers or chemical etching may also be evaluated.

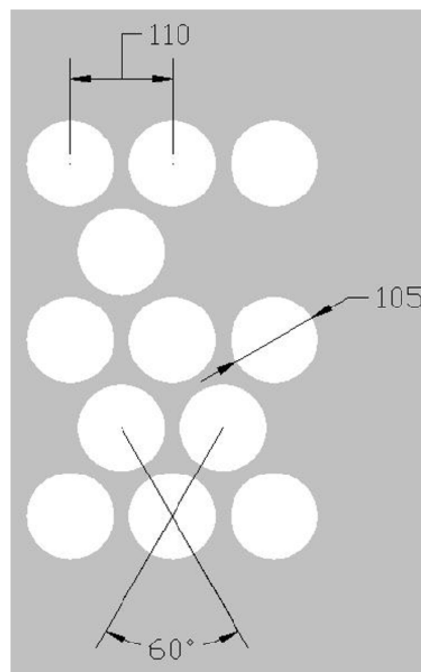

Figure 5: Theoretical design dimensions

Figure 4: Repeated MM created deformed invar and distorted vias

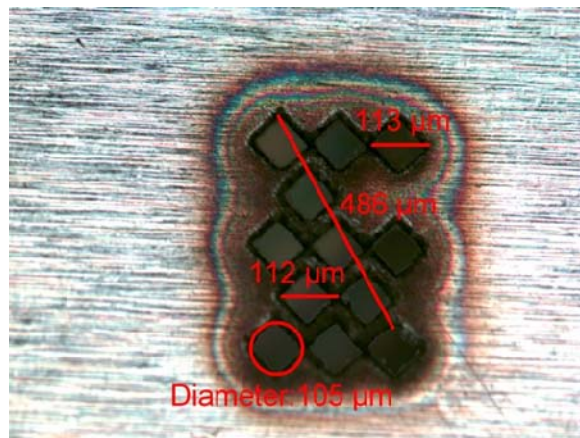

Figure 6: Experimental dimensions

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Electro Deposition

At the time of writing the first samples were just electro deposited with a 25 µm layer of dielectric coating and initials results are show here.

The laser etched vias have been electro deposited with a 25 µm layer of dielectric. Through the extent of the deposition, the vias have been conformally coated. Vias were left with proper hole spacing that was left after the deposition. Comparison of pre-deposition and post deposition have been studied and analyzed for results and further testing. (as seen in Figure 7,8)

This conformal coating and hole spacing will provide a large enough gap to apply a sputtered metal layer interface, along with desired metal coating.

This process has not yet been fully completed. Sputtered metal layer and metal plating still needs to be tested.

Results

Throughout via testing and analyses, many parameters have been optimized and altered to provide the closest results to our theoretical designs and dimensions. Many factors caused concerns such as discoloration, inconsistent laser power, and invar deformation. All of these issues have been addressed and accounted for by etch cleaning, laser optimization, and providing an underlying substrate for the Invar.

Multiple tests have shown that laser etched vias are capable of providing a significant increase in number of vias/cm^2. This has been accomplished by optimizing geometry design, dimensions, tolerances, and design method. These tests have shown that laser etching is a capable process for ablating vias into Invar metal core and constructing a ground electrical circuit throughout the substrate.

State of the Art Industry Implementations

State of the art (SOA) features and designs have been implemented periodically throughout industry. These SOA designs provide industry with a further reach to newer technology. The fallowing ideas have a strong impact on the designs of high density via structures in the future.

Via in Pad (VIP) approach places a via directly under a substrate's contact pad. This allows higher component density and improved routing. Also, VIP provides the designer significant PCB space savings. VIP offers far more advantages such as better thermal management, meets closely packed placement requirements, overcomes constraints such as low inductance, provides a flat, coplanar surface for component attachment, and no via plugging is required at component locations. [6, 7, 14]

In complex circuit designs, electroless nickel and immersion gold have become established as preferred solderable surface finishes for high reliability applications. The ENIG finish provides a flat surface that does not tarnish or discolor. It has a long shelf life, and the topcoat has an excellent electrical continuity. The nickel serves as a barrier against copper diffusion and prevents

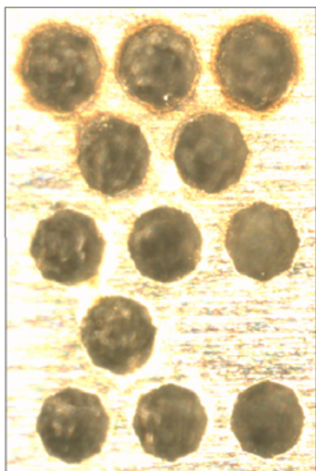

Figure 7: Pre-deposition vias

Figure 8: Post Deposition Vias

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copper contamination of the solder during wave soldering and rework operations. The finish also provides Electromagnetic Interference (EMI) shielding to the surface of the substrate. [2, 3, 9, 12, 13]

Coplanar Waveguides incorporates the use of a ground conductor that is coplanar with the signal conductor, thus the impedance is controlled by the single line width and the ground gap. This means you can keep the impedance constant as you taper the signal conductor's width down to meet a pin. This is exact matching to a component pin without changing the substrate thickness. [10]

Flex multilayer production of high density and high performance substrates at a reasonably high productivity, a new high-density multilayer technology named DSOL has been developed. This development is characterized by a new high performance dielectric material with very fine pitch Cu conductors, and mostly the same process and manufacturing facilities as a conventional build up PCB. Fluorene based resin was used due to the advantages of a low dielectric constant (3.2), low dissipation factor (0.002), low coefficient of thermal expansion (CTE) (40ppm) and high Tg (230°C). Also, fluorene has an excellent resolution, which is equal to that of photoresist used for the advanced semiconductor devices fabrication. [4]

Conclusions

By replacing conventional PCBs with thin metal-core boards, provides advantages for radio frequency circuits and packages, and increases heat dissipation for high power applications.

Facile processing of ultrathin METCORE™ substrates with high via and density that are HVM compatible has been successfully completed. These processes have been a success without compromising any key properties such as interfacial adhesion.

A finalized substrate has been completed using laser etching, although not time nor cost efficient. These results of a via to the metal core was formed to provide electrical grounding throughout the substrate.

Acknowledgements

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