Wafer Level Package with Y shaped TSV and Vacuum Sealing by Cu-Sn Isothermal Solidification for MEMS Resonator

Yuhan Cao, Le Luo*
The State Key Laboratories of Transducer Technology,
Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences,
865 Changning Road Shanghai, 200050 P.R.China
*Corresponding Author E-mail: leluo@mail.sim.ac.cn

Abstract

A novel WL- CSP structure for MEMS device is proposed. Key features are: "Y-shaped" TSV is fabricated to reduce cost; Cu-Sn isothermal solidification is used to achieve lower temperature bonding; I/O interconnection and vacuum sealing are achieved simultaneously simplifying the whole process. Average shear strength of 25.5 MPa and excellent leak rate of around 1.9×10^{-9}atm cc/s have been achieved, which meet the requirements of MIL-STD-883E. Four point probe setup is used to measure the resistance of the "Y shaped"-TSV and the contact resistance of the Cu/Sn IMC bond joint. "Q factor extraction method" is used to monitor the vacuum property of the packaging structure by integrating a MEMS resonator with a resonant frequency of 1.3 KHz. Reliability tests such as long-term and accelerated life testing are also performed both achieving good results.

Keywords: WL-CSP, TSV, Cu/Sn bonding, vacuum & hermetic packaging, MEMS resonator

1.Introduction

Wafer level chip scale package (WL-CSP) technologies have been developed for micro-system packaging because they can encapsulate and protect the delicate parts of the MEMS device prior to dicing therefore improve the yield as well as reduce form factor and cost. There are different methods to achieve I/O connection in wafer level packaging technologies among which through silicon via (TSV) fabricated by Deep Reactive Ion Etching (DRIE) has been frequently adopted recently[1-3]. TSV technology has its advantages such as high density, low resistance, parasitic capacitance and parasitic inductance, but it requires whole silicon wafer DRIE penetrating which is too costly to be widely used. In order to make WL-CSP technologies more attractive, improvements should be made. Besides, wafer bonding technology should also be properly selected to be compatible with the MEMS/CMOS fabrication processes.

In this paper, a novel wafer level package for MEMS resonator is proposed. Key features of this structure are: (1) A "Y-shaped" through wafer I/O connection structure is fabricated to reduce the cost compared with traditional TSV fabrication; (2) Cu-Sn isothermal solidification technology is chosen to achieve solder bonding at 350℃ compatible with most MEMS/CMOS processes; (3) I/O connection and cavity hermetic sealing are achieved simultaneously in bonding procedure which simplifies the fabrication process. Shear strength test and leaking rate test are performed. Four point probe setup is used to measure the resistance of the I/O connects. A MEMS resonator is integrated to detect the vacuum quality using "Q factor extraction method". Long-term and accelerated life testing are also performed to detect the reliability quality.

2.Packaging design

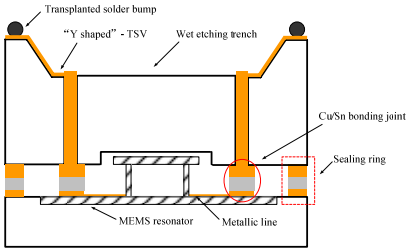


Fig.1 Schematic view of the proposed package after 2nd level packaging

Figure 1 shows the cross-sectioned view of the packaging structure after 2nd level packaging. Key features of the designed packaging structure are: (1) Tetramethylammonium hydroxide (TAMH) solution etching is used to form wet etching trench locally thinning the cap wafer. (2) "Y-shaped"-TSV

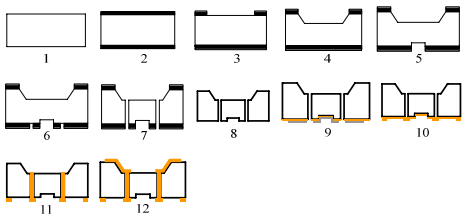


Fig.2 Cap wafer of the packaging structure fabrication process flow

structure is fabricated in the thinned region of the cap wafer. (3) Cu-Sn isothermal solidification technology is used to joint the cap and device wafers. (4) "Y shaped"-TSV, Cu/Sn bonding joint and metallic lines fabricated on the resonator together constitute the overall I/O connection structure. (5)Cavity hermetic sealing is achieved by bonded sealing ring. It is expected that such a packaging structure can achieve a preferable balance among cost efficiency, form factor and quality.

3. Fabrication

3.1.Fabrication process flow of the packaging structure

Figure 2 gives a brief description of the fabrication process flow for the cap wafer and the details are discussed as below:(1) Cap wafer is a 4 inch, 350 μ m thick silicon wafer with a resistivity over $2\times10^{4}\Omega\cdot$ cm. (2) 2 μ m thickness oxide layer is formed on the cap substrate by thermal oxidation process. (3) The first photolithographic process is done at the front side and the oxide layer is patterned using buffered oxide etch (BOE) solution etching with the backside oxide layer protected by photoresist. (4) TMAH etching is used to locally thin the cap wafer. (5) Similar measure as step (3) together with DRIE is performed on the backside to form the cavities for the movable part of the MEMS device. (6) The third photolithographic process is performed on the backside in alignment with the pattern on the front side and the oxide layer is patterned using BOE etching to serve as mask for the next dry etching process. (7) Use DRIE to penetrate the cap wafer to fabricate the TSVs. (8) 2 μ m uniform thermal oxide layer is formed on the sidewall of both the TSVs and the trench. (9) Seed layer is sputtered on the backside and coated by spraying photo resist. The fourth photolithographic process is then performed and photoresist at the position of the vias and the sealing rings is developed and removed. (10) Electroplating is used to deposit copper locally on the backside of the wafer to block the vias and form the sealing rings simultaneously. The deposited Cu will also serve as the UBM layer in the following bonding process thus has no need to remove. (11) Bottom—up copper electroplating is performed to metalize the vias [4]. During electroplating, only the front side of the wafer contact with the copper electrolyte so that the back side need not be protected. The plating operation will continue until copper columns protrude from the bottom surface of the trenches. After electroplating, the remaining seed layer on the backside is removed by ion beam etching. (12) Photoresist is sprayed on the front side and lift-off technique is used to finish the "Y shaped"-TSV structure [5-6].

Figure 3 shows the amplificatory "Y-shaped" –TSV structure. Note that the deposited Cu layer beneath the TSV will serve as the UBM layer in the following bonding process thus has no need to remove.

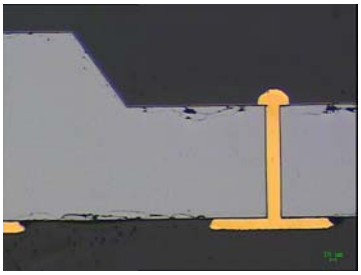


Fig.3 Cross-sectioned view of the "Y shaped"-TSV

3.2.MEMS resonator fabrication process flow

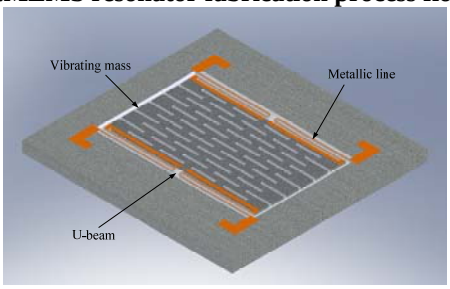


Fig.4 Schematic view of the MEMS resonator

A MEMS resonator is designed to be integrated in the packaging structure to monitor the vacuum of the sealed cavity. It primarily comprises of three parts: a vibrating mass, four U-beams at corners and metallic lines on the beams as I/O connections. A schematic view is illustrated in Detailed fabrication process flow is shown in Figure 5: (1) A N (111) orientation silicon wafer is used and 2um silicon dioxide layer is formed on wafer surface by thermal oxidation, (2) the silicon dioxide layer is then thickened to 4 um by LPCVD, (3) photolithographic process combined with reactive ion etching (RIE) is then used to pattern the silicon dioxide layer and at somewhere the silicon is exposed, (4) 50um deep trench is made at silicon area

by DRIE to form the "mass-beam" structure of the resonator, (5) another 1.5um silicon dioxide layer is formed onto the wafer resulting to 3.5um thick silicon dioxide layer outside the trenches and 1.5um thick silicon dioxide layer inside the trenches, (6) RIE is then utilized again to completely remove the silicon dioxide on the trench bottom while the "mass-beam" structure is still covered by remained silicon dioxide layer, (7) with the protection of the remained silicon dioxide layer, another 30um silicon DRIE is used to form the release trenches, (8) wet etching in TMAH solution is used to finally release the resonator , (9) the remained silicon oxide is completely removed by BOE solution etching and a new 2um thick silicon dioxide layer is formed again on the device wafer as passivation layer, (10-12) finally standard lift-off process is used to form metallic lines on the U-beams to accomplish the resonator fabrication process. Fabricated MEMS resonator wafer is shown in figure 6, bottom-right showing the SEM view of individual device.

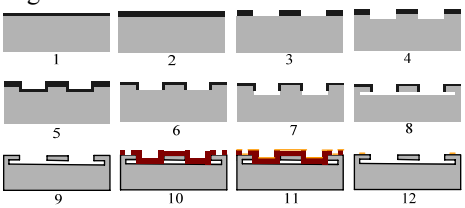


Fig.5 Resonator fabrication process flow

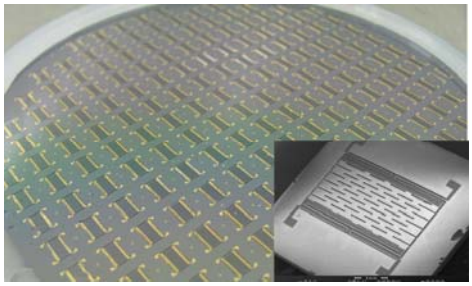


Fig.6 Microscope photograph of the MEMS resonator wafer,SEM view (bottom-right)

3.3.Improvement of processes on the MEMS device wafer

Before it is used as the bonding wafer, improvement must be made on the MEMS device wafer to form bonding structures. As shown in Fig.7: (1-2) passivation layer is formed above the overall metallic lines except districts of four pads for I/O connection, (3-5) seed layer for electro-deposition is locally sputtered, (6-10) photolithographic process and electro-deposition are primarily used to form copper and tin layers onto the MEMS device wafer to achieve the bonding structures (including bonding pads and sealing ring).

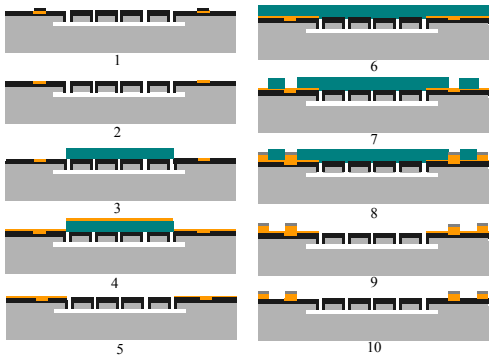


Fig.7 Improved resonator fabrication process flow

3.4.Key techniques utilized in fabrication process

3.4.1 Spraying photoresist

Nonplanar surfaces are encountered in the fabrication process and spraying photoresist technique is needed. Spray coating can transfer patterns to the bottom and sidewall of the cavities . Proper parameters such as photoresist type, solid content of photoresist, dispense volume and scanning speed should be chosen. In this work, the EVG101 spray system and diluted AZ4620 with butanone are used in the process.

3.4.2 Copper electroplating

Copper electroplating technique is used for the metal filling of dry etched TSV. Copper is chosen for its low cost, low resistance, superior resistance to electromigration and reducing RC time delay compared with Al etc., and also copper plating is a mature procedure widely used as well. A bottom-up electroplating method is used instead of the common electroplating method because it is more suitable for high aspect ratio feedthroughs. Such method includes three steps described as below:(1) Seed layer deposition on the back side;(2)Electroplating to block vias from the back side. Because the lateral growth of copper in electroplating, via with a width of D can be totally blocked if the thickness of the plated copper layer exceeds D/2;(3) Electroplating to fill the vias from the front side: Copper columns will grow from bottom to up if the copper electrolyte can permeate into the vias and contact with the upper surface of the bottom copper layer which blocks the vias. In order to achieve a void-free plating result, AIT plating system is used in this work which can provide agitation during the whole plating process. 20mA/cm^2 DC current density is maintained to fill the vias in about 16 hours.

Specially, in this work local electroplating is utilized to block the vias at step (2). The copper layer formed by local electroplating can also serve as the under bump metallurgy (UBM) layer in the

following bonding process, thereby avoiding the removing which usually needs CMP process.

3.5 Cu/Sn isothermal solidification

Since the bonding process is fluxless, the control of the Sn layer thickness becomes very important. On the one hand, a large amount of Sn will lead to the molten Sn overflowing from the edge of the bonding interface during bonding. Sometimes such an overflow is so disastrous to cause short circuit. On the other hand, Sn layer without enough thickness will lead to poor wetting during the bonding process finally affecting the bonding quality. Whether to have the Sn layer on both bonding wafers also needs identification. In the theory of Bosco et. al.[7], a model of both bonding wafers including Sn layers is established and a critical thickness for the Sn layers is demanded to achieve a void-free bonding result. Such a critical thickness for this work (if both wafers have Sn layers) is calculated out according to Bosco's equations [7] but proves too large to avoid the molten Sn overflowing and thus Sn is only deposited on the dummy device wafer. Special experiments are designed and carried out in the prior work[8] with different Sn layer thickness of 3 μ m, 4 μ m, 5 μ m,6 μ m and 8 μ m under the same bonding condition to find the moderate thickness. The results are: (1) In all cases, Sn is completely consumed left the intermetallic compound (IMC) layers and the remaining UBM layers; (2) When the thickness of Sn layer is 3 μ m, considerable amount of voids like defects occur at IMC layers interface indicating poor wetting during bonding; (3) A void-free result can be achieved with 4-8 μ m thick Sn layer while the overflow of the molten Sn occurs when the thickness reaches 6 μ m. As a result, a thickness of 4 μ m is considered to be a moderate value for the Sn layer.

As for the thickness of the Cu layer, it needs not much accuracy. Large enough thickness should be provided to assure remaining Cu left after the bonding process for once the Cu layer consumed the IMC layer will contact directly with the underlying non-solderable layer and a poor adhesion between IMC and the non-solderable layer will occur. Besides, the remaining Cu layer can also be used as spacer to alter the space for the device inside. In view of all above mentioned points, it is determined that 6 μ m Cu should be electroplated on the dummy device wafer. The UBM layer on the cap wafer is just the Cu layer formed in the former steps used to block the TSVs and its thickness is determined by the dimension of the TSVs. In this encapsulation structure each TSV is 20 × 20 μ m2 size so that the thickness of the Cu layer on the cap wafer is about 10 μ m.

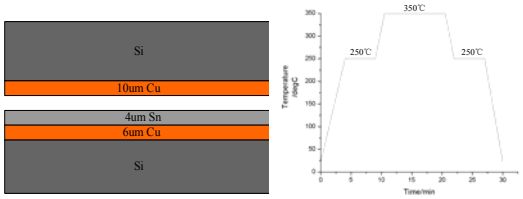


Fig.8 (a) "Cu-Sn-Cu" bonding structure, (b) Temperature-time profile of bonding

The cap wafer together with the device wafer constitutes the "Cu-Sn-Cu" bonding structure as shown in Figure 8a. Prior to the bonding process, surface treatment is very important for good bonding quality. Sn is easy to be oxidized even at room temperature and both wafers have gone through photolithographic process after which small amount of photoresist or other contaminations will probably be remained on the surface. Ar plasma cleaning using the Ionfab300 Plus ion beam platform is applied to complete the surface treatment in order to acquire a void-free bonding result. Power and etching time is controlled to avoid Sn from melting. Generally the power of plasma is 500W and the cleaning time is 170s. After the surface treatment, wafers are aligned and brought into the SB6 bonding machine to complete the bonding process. The SB6 bonding machine keeps a vacuum environment around 3×10^{-5} mbar in the chamber during the whole bonding process. The bonding force is 200N and the temperature-time profile is as shown in Figure 8b. At the end of the bonding process, N_2 is filled into the chamber to fast cool down the hot trunk.

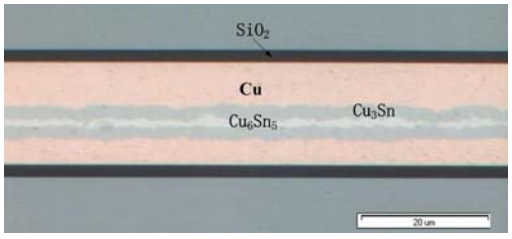


Fig.9 Cross-sectioned view of the Cu/Sn interlayer

Figure 9 shows the cross-sectioned view of the Cu/Sn interlayer after the bonding process [8]. It can be seen that Sn is totally consumed and the remaining Cu is left on both sides. The IMCs left after bonding is composed of two components: a light grey colored layer and a dark grey colored layer. EDS analysis shows that the light grey colored layer is Cu_6Sn_5 (η -phase) and the dark grey colored layer is Cu_3Sn (ε -phase). It can be seen that although the surface of the electroplated Cu layer is rough and not flat, there is no void at the interface

between the Cu layer and the IMC layer because of good wetting during the bonding process.

3.6. Fabrication results

Figure 10 left shows the infrared microscope photograph wherein encapsulated resonator is visible. Sixteen pads are fabricated at the periphery of the wet etching formed trench used to place solder bumps onto. The cross-sectioned view is shown on the right r, wherein vibrating mass, U-beam, TSV and sealing ring are all visible. Right-top shows the microscope photograph of the whole packaged MEMS device wafer.

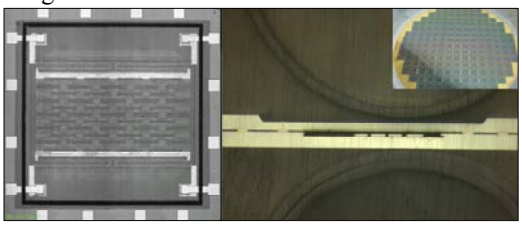
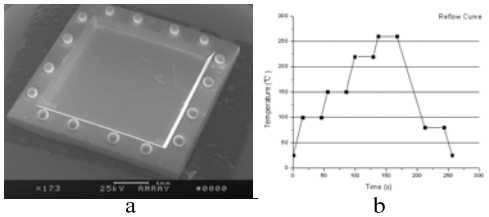


Fig.10 Photograph of the wafer level chip scale packaged MEMS resonator

3.7. 2nd level packaging design and experiment results

As motioned above, sixteen pads are made on the top surface of the packaging structure on where tin solder bumps with a diameter of 200 μ m are to be placed. Then the solder balls are reflowed in the Falcon 8500 reflow oven to achieve the 2nd level packaging structure. The result of SEM view is shown in figure 11a. The reflow line is shown in Figure 11b. Flip-chip technology is further utilized to attach the packaging structure to PCB boards. The average bonding strength of the solder bumps is measured to be around 0.36kg.



a b

Fig.11: (a) SEM view of 2nd level packaging , (b) Solder bump reflow line

4.Packaging Evaluation

4.1. Transition properties of the "Y shaped"-TSV by 3D FEM Simulation

The packaging structure is designed intentionally for the usage of a variety of MEMS devices. It is expected that for some very small scaled MEMS resonator, the resonant frequency could be as high as 1GHz. [9] So that the transition properties of the "Y shaped"-TSV at high frequency are worthy while investigation. Ansoft HFSS™ 3D electromagnetic simulator is utilized for simulation. Transition properties of two different structures remarked as A and B are simulated for comparison. A has the "Y-shaped" through wafer interconnection structure as proposed before composed of two parts: a copper strip on the side of a 150 μ m height trench and TSV with a height of 200 μ m. B has a 350 μ m height TSV. In both structures, the substrate is silicon wafer with a resistivity over $2\times10^4\Omega\cdot$ cm. Fig.12 shows the two structures and the simulation results. It can be seen that when the signal frequency is less than 500MHz the scattering parameters of the two structures have little differences. That means the two different through wafer interconnection structures have almost the same reflection loss and insertion loss below 500MHZ. In this work, the MEMS resonator to be integrated has a resonant frequency at about 1.3KHZ so that the proposed package structure is well suitable for use.

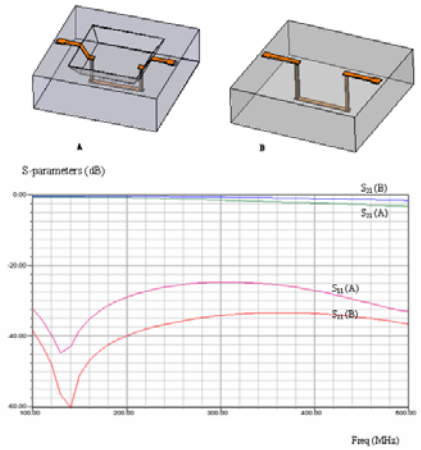


Fig. 12 S-parameters of two I/O connection structures by 3D FEM EM simulation

4.2. Resistance measurement

In order to measure the contact resistance of the bond joint and the resistance of the "Y shaped" -TSV, test structures are built (as shown in figure 13) and four point probe setup is used to lead current through the resistor to measure the voltage drop.Three different resistance measurement structures are fabricated and each average resistance is remarked as R_1, R_2 and R_3 in sequence. The resistance of the metallic line on the trench side can be simply calculated out from R_3 and remarked as R_4 by considering its proportion in the whole metallic line length. The resistance of each TSV can be calculated out by $(R_1–R_3)/2$ and the contact resistance per bond joint can be calculated out by subtracting

(R_2-R_1)/2. The resistance of the "Y shaped"-TSV can be calculated by R_4 + (R_1-R_3)/2. Final results show that the resistance of the TSV is about 0.4Ω and the contact resistance per bond joint is about 30mΩ which is quite small. The resistance of the "Y shaped"-TSV is about 0.7Ω. Such values are compatible with most MEMS devices.

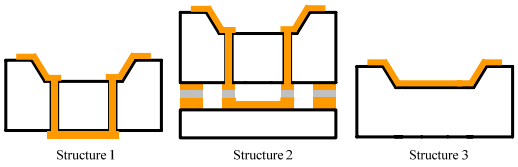


Fig.13 Schematic view of three resistance measurement structures

4.3. Shear strength test

The shear strength of the samples is measured using Dage series 4000B Bondtester. As a reference, MIL-STD-883E, method 2019.5, applicable for die attachment can be used. In this work, the bonding pattern is a 0.02cm wide, 0.52cm × 0.54cm closed square ring and four 0.02cm × 0.02cm squares inside with a total area of 6.28mm^2. The failure criteria of MIL-STD-883E, method 2019.5 requires that "all die area larger than 64×10^{-4} in^2 shall withstand a minimum force of 2.5kg or a multiple". Accordingly, shear strength of about 6MPa is needed for the samples in this work. Measurement results of 20 samples show that the maximum shear strength is 25.5MPa, the minimum shear strength is 13.4MPa and the average is 19.5MPa. The result demonstrates that the shear strength of the samples satisfies the MIL-STD-883E.

4.4. Hermeticity test

Fine-leak tests as well as gross-leak tests are done on the samples in order to characterize the hermeticity of the package.

4.4.1. Fine-leak test

The cavity volume of the sample is less than 0.001cm^3 and according to MIL-STD-883E, the leakage limit is 5×10^{-8}atm cc/sec. In the fine-leak test, the samples are first placed in a chamber, pressurized with helium and soaked for 3h at 5bar, and then transferred to the helium leak detector to be monitored. The average reject limit is 1.9×10^{-9}atm cc/s which is well below the leakage limit.

4.4.2. Gross-leak test

The gross leaks are tested using fluorocarbon and are based on the "bubble method". Packaged samples are placed under fluorocarbon liquid FC- 84 in a vacuum chamber full of N2 with the pressure of 5 bar for 5h.Then the samples are removed from the bath, dried in the air and immersed in fluorocarbon FC-40 which is maintained at 125℃. If gross leak is present, any trapped helium will have ample time to escape from the cavity to be inspected. In the test, all 20 samples pass the gross-leak test successfully.

4.4.3.Long-term hermitic stability test

Samples of resonators after packaging are tested at constant temperature 25℃ at the beginning and the end of 3 months. As shown in Table 1, Q factors of 10 samples are measured with an average degradation of about 4.34% in Q. The offset is considered due to the uncertainty in the measurement with the primary cause of discretization of frequency by the measurement tool. The test result proves the good hermeticity of the packaging structure. The method of acquiring the Q factor is to be discussed below.

5. Vacuum test

5.1. Q factor measurement of resonator before and after packaging

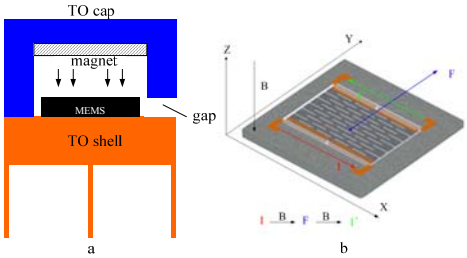


Fig.14: (a) Schematic illustration of the exertion of magnetic field, (b) Q factor measurement principle illustration

The unpackaged resonator is attached to a TO shell and a magnetic field is exerted perpendicularly by a magnet fixed on the TO cap as shown in figure 14a. A gap is specially made so that the gas pressure inside the TO cap is compatible

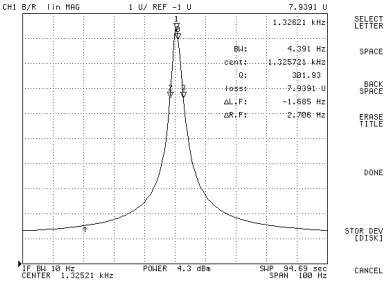


Fig.15 The frequency response of the micro-resonator before packaging

Table 1: Q factors of 10 samples tested in 3 months and the degradation of Q

Resonator	Testing at the begenning of 3 months		Testing at the end of 3 months		% dgradation in Q
	f(Hz)	Q	f(Hz)	Q	
1	1262	592	1249	571	3.54
2	1243	589	1252	563	4.41
3	1279	596	1264	573	3.86
4	1284	604	1275	586	2.98
5	1257	564	1216	531	5.85
6	1268	583	1285	580	0.51
7	1306	594	1254	539	9.26
8	1319	569	1286	531	6.68
9	1258	562	1256	542	3.56
10	1267	579	1264	563	2.76
average	1274	583	1260	558	4.34

the environment. An ac stimulating signal is applied at the input port and the response signal could be detected at the output port as shown in figure 14b. Actual Q factor measurement system comprising: the test circuit board, DF1731SB2A-the power supply and HP 4395A Network-sending exciting signal and receiving responding signal. Figure 15 shows the frequency response of the 1.3 kHz micro-resonator before packaging. The Q factor of the resonator before packaging is about 300.

5.2. Calibration

The vacuum package can be characterized by the integrated MEMS resonator according to the "Q factor-extraction method" [10]. In physics, the quality factor Q is defined as the ratio between the total system energy and the average energy loss in one radian at resonant frequency. So that larger Q factor of the integrated MEMS device dictates less dissipation by damping – i.e., the resonator is working under good vacuum condition.

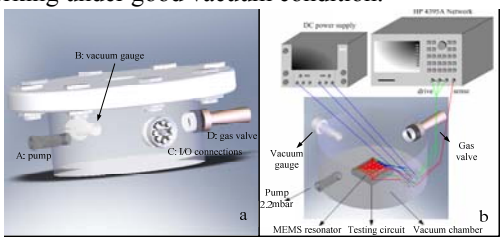


Fig.16: (a) Metal chamber for calibration, (b) illustration of calibration operation

Besides, calibration is needed to define the value of the vacuum provided by the package structure. In this experiment, a metal chamber is specially made to accomplish the calibration. As shown in figure 16a, the chamber primarily comprises: port A and B separately linked to pump and vacuum gauge, port C, an I/O connection between inside testing device and outside measuring equipments, and D, a gas valve. The unpackaged MEMS resonator is placed inside the chamber working under different gas pressures with definite values read by the vacuum gauge and the relevant Q factors are recorded by HP Network as shown in figure 16b. Figure 17 shows the calibration line wherein the Q factor of a packaged resonator with an average value of 583 dictates a 400mbar vacuum level in the cavity of the package structure. It is noted that the vacuum is not good with the reason currently presumably due to the incomplete disposal of water vapor before bonding. Further work is to solve the problem and enhance the vacuum quality of the packaging structure.

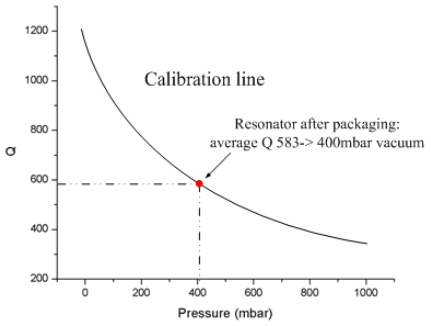


Fig.17 Calibration of the MEMS resonator after packaging

6. Conclusions

In this work, a wafer level package with simultaneous TSV connection and cavity hermetic sealing by low temperature solder bonding for MEMS devices such is proposed. Wet etching technology together with dry etching technology is utilized to fabricate a "Y shaped" -TSV structure to shorten the TSV in order to reduce cost. Cu/Sn bonding with a peak temperature of 350℃ is utilized to achieve hermetic sealing and TSV connection simultaneously to simplify the fabrication process. Average shear strength of 25.5Mpa and excellent leak rate of around 1.9×10-9atm cc/s have been achieved, which meet the requirements of MIL-STD-883E. Ansoft HFSSTM 3D electromagnetic

simulator is used to assess the transition properties of signal with the conclusion that the packaging structure can be used well in low frequency region. Through four point probe measurement and calculation, the resistance of the "Y shaped" -TSV is about 0.7Ω and the contact resistance of the bond joint is about 30mΩ, both are low enough for most MEMS device integration applications. A MEMS resonator with a resonant frequency around 1.3 KHz is integrated in this packaging structure, special metal chamber is designed and "Q-factor extraction" technique is utilized to monitor the vacuum of the packaging structure to be around 400mbar. Reliability tests such as long-term and accelerated testing are also performed indicating good reliability both on bonding joint quality and hermeticity. Further work is to enhance the vacuum quality of the packaging structure.

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