Resistive Open Defect Isolation in Nano-probing

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Introduction

In semiconductor failure analysis, hard open (resistance over 1MΩ) and direct short (resistance less than 1KΩ) defects are usually straightforward to isolate with well-established FI/FA flow. However, high standards of computer chip product quality require thorough detection and elimination of subtle defects such as resistive open, which resistance is typically in the range of 1KΩ to 1MΩ. This type of defect often associates with voltage sensitivity and ambiguity in optical FI, so nanoprobing plays a major role in overall FIFA flow for finding the root cause. In this paper, we present case studies of localizing resistive open defects using various FA techniques, including two-terminal IV, two-terminal Electron-Beam Absorbed Current (EBAC) [1], Electron Beam Induced Resistance Change (EBIRCh), Pulsed IV, Capacitance-Voltage (CV) and Scanning Capacitance Microscopy (SCM). The advantage and limitation of each technique will also be discussed.

Case Studies of localizing resistive open defects

1. Back-end (BE) resistive open detection using two-terminal EBAC on a backside sample

The sample was deprocessed from backside (silicon side) to look for backend (BE) interconnect defect, after exposing contacts, two-terminal IV measurement was performed between north end and south end of the suspected trace, the probe tips were landed on the contact of the backside sample. From IV characteristic (Fig.1), resistance of the interconnect between two ends exceeded 3MΩ, which indicates there is a resistive open on the trace.

Figure 1: IV characteristic of a resistive open. probe tips were landed at north and south ends of the suspected trace.

The conventional one-terminal (single tip) EBAC technique was used to localize the open on the blue trace in Figure 2(a), the acquired EBAC image in Figure 2(b) shows the full length of the blue trace, therefore the conventional single tip EBAC was not successful in localizing high resistance open. In this case, we used two-terminal EBAC [2]. For this technique, in addition to the conventional one-terminal EBAC, we added a second probe as a ground terminal. During EBAC acquisition, the signal probe was landed on one end of the resistive path, and the grounding probe was landed on the opposite end of the resistive path. The result of two-terminal EBAC is shown in Figure 2(c), instead of highlighting the entire trace, the two-terminal EBAC image clearly shows the signal discontinued about one third of the total length from the top end, by comparing the EBAC image with CAD layout, we can localize the high resistance defect to an exact location, then TEM analysis can be carried out at the defect location.

Figure 2: (a) CAD layout of the ROI trace, (b) conventional one-terminal EBAC image and (c) two-terminal EBAC result from the same trace.
Figure 3 shows the TEM analysis results of the high resistance defect. The interface between BE interconnect via and metal line is compromised, resulting to a resistive connection.

![Figure 3: TEM analysis results of the high resistance defect.](image)

**Figure 3: TEM analysis results of the high resistance defect.**

**Discussion of two-terminal EBAC**

Figure 4(a) and 4(b) are the illustrations of one-terminal EBAC and two-terminal EBAC setup. The dark oval shape embedded in the metal line is a resistive open. In the one-terminal EBAC setup, when primary electron beam of SEM scans across the metal line, the absorbed current flows to the signal probe, which is connected to a two-stage high gain amplifier. Due to the high gain amplification, even pA level of absorbed current can be collected by the signal probe, the current pass through a resistive open is usually more than pA, therefore the entire signal trace can be highlighted in EBAC image. [2] However, in the two-terminal EBAC setup, because of the additional ground probe, the absorbed electrons take the least resistance path to the ground, some current can discharge into the ground probe, instead of passing through the resistive open into the signal probe, so only the trace that is between the resistive open and the signal probe will be highlighted. By collecting two complementary two-terminal EBAC images, the resistive open defect can be precisely localized. The two-terminal EBAC can be very useful in failure analysis where one-terminal EBAC is unable to localize the defect.

![Figure 4(a) and 4(b) are the illustrations of one-terminal EBAC and two-terminal EBAC setup.](image)

**Figure 4(a) and 4(b) are the illustrations of one-terminal EBAC and two-terminal EBAC setup, red arrows indicate the electron flow directions.**

2. **BE resistive open detection using two-terminal EBAC on a front side sample**

The two-terminal EBAC can be applied not only to backside deprocessed samples, but also to front-side deprocessed samples [3]. For front-side samples, sample was mounted on SEM stub with Cu tape, the Vcc/Vss power supplies of the sample were electrically connected to the stub. When sample is loaded in a nanoproping tool, Vss is shorted to the chuck, then a DC measurement of the signal trace diffusion current can be performed between the signal trace and sample chuck.

Figure 5(a) shows the CAD layout of two metal lines at the same layer, these two metal lines are connected via lower layer metal lines. The same color in CAD layout indicates they are from the same net, one side connect to diffusion (driver), the other side connects to gate (receiver). Using front side (metal side) deprocessing, these two metal lines were exposed at the same time, two-terminal DC measurement results between metal lines and chuck are shown in Figure 5(b) and 5(c). Figure 5(b) shows the normal diode current expected from silicon, which was measured from the shorter (left side) metal line; Figure 5(c) shows the current measured from the longer (right side) metal line. The current level dropped more than five orders of magnitude, which is an indication that current measured from long metal line pass through a highly resistive path.

![Figure 5(a) shows the CAD layout of two metal lines at the same layer, they are connected via lower layer metal lines.](image)
To precisely localize the defect, high kV two-terminal EBAC was performed with two complimentary configurations. In Figure 7(a), the signal probe was landed on the left side shorter metal line, ground probe was landed on the right side longer metal line, the portion of the trace to the left of the resistive open was highlighted. In Figure 7(b), the signal and ground probes were swapped, the result shows the other portion of the trace to the right of the resistive open. By comparing two complimentary EBAC images with CAD layout in Figure 7(c), defect location can be determined precisely, which is indicated by the red arrow in the EBAC images and CAD layout. The follow-up TEM sample preparation can be done at this location.

The TEM analysis result is shown in Figure 8. The via landed on metal line has void due to blocked barrier deposition and via fill. The defect outlined by red dash line shows the barrier layer wrapping around metal filling material.
3. BE resistive open detection using EBIRCh on a backside sample

For resistive open defect where the resistance is over 100KΩ, the two-terminal EBAC is a powerful technique in most cases, however, for other cases where resistance is below 10KΩ range, two-terminal EBAC often shows inclusive results either due to amplifier overloading or poor contrast. In these cases, EBIRCh is more effective in locating the defect [4],[5],[6].

Figure 9 shows the IV measurement of a failing contact-via-metal-line chain structure. Despite the higher-than-expected resistance, the IV curve still shows ohmic behavior, indicating the defect is different from other cases in which the IV curves showed non-linear voltage dependence.

![Figure 9 shows the IV measurement of a failing contact-via-metal-line chain structure](image)

Figure 10(a) shows the EBIRCh and SEM overlay image of a contact-via-metal chain structure, 10(b) shows the layout of the chain structure, 10(c) shows TEM analysis shows the root cause of the defect.

4. FE resistive gate detection using two-terminal IV and SEM inspection on a backside sample

For front end (FE) defect, which involves gate or source/drain contact, if backside failure analysis approach is applicable, the two-terminal IV can be a straightforward method to localize a resistive gate open defect.

Figure 11(a) shows the SEM image of the backside sample, after silicon removal. Additional sample polish and ion beam milling was used to expose both gate and gate contact at the same time. For the electrical measurement, one tip was landed on failing cell gate contact, another tip was landed on a passing cell contact (not visible in the SEM field of view). Figure 11(b) shows the CAD layout of this gate, the grey color tip shows on which part of the gate contact that the tip was landed. Two-terminal DC measurement result is shown in Figure 11(c), which has ohmic behavior with low resistance.

![Figure 11(a) shows the SEM image of the backside sample](image)
Figure 11(a) shows the SEM image of probe tip landed on gate contact. Figure 11(b) shows the CAD layout of this gate, the grey color tip shows on which part of the gate contact the tip was landed. The IV measurement result is shown in Figure 11(c), which has ohmic behavior with low resistance.

After moving the tip from gate contact to the metal gate, the two-terminal IV measurement was collected from metal gate to the same passing cell contact. The measured IV curve in Figure 12 shows a resistance over Mohm range, the behavior is also different from ohmic contact. By comparing the results of these two measurements, it is safe to draw the conclusion that there is a resistive connection between the metal gate and the gate contact.

Figure 12(a) shows the SEM image of probe tip landed on metal gate. Figure 12(b) shows CAD layout where the tip was landed on the gate. Figure 12 (C) shows the IV measurement from failing cell metal gate to the passing cell contact.

5. FE resistive gate detection using Pulsed IV, C-V and SCM on a front side sample

For some resistive gate cases, the sample for failure analysis might be one-of-a-kind, from optical fault isolation, the defect could involve silicon fins, then the backside approach would be too risky of losing the defect. For such cases, silicon fins need to be preserved, and devices need to remain intact from sample preparation, therefore front side detection techniques need to be developed and proven effective for these cases.

5.1 Pulsed IV probing

While DC probing can identify most transistor defects, it is effectively only a static state analysis, many defects which cause a circuit or device to fail are problem with dynamic or switching response. For resistive gate defect, the DC probing cannot find any abnormality, because the gate has enough time to charge up, and the conducting channel of MOSFET can be formed. To detect such defect from front side, we use a pulse generator connecting to the gate to dynamically stimulate the transistor and use a high-speed oscilloscope connecting to the drain to record the output, looking at the device behavior on a nanosecond scale [7]. By comparing the dynamical response of a failing transistor with a reference, we can get insight of gate connection integrity.

Figure 13(a) shows the Pulsed IV input (blue curve) and response (red curve) from a passing MOSFET device. The input was connected to the gate terminal, while maintaining a constant source to drain bias, the response was monitored from drain terminal. The response follows input, there is no delay in turning on the device. Figure 13(b) shows the results from a failing device when the same pulse (20ns) was given to the gate. The response current level is very low, indicating the device cannot be fully turned on within 20nS time frame. The defect is likely to be a resistive connection to the gate. Figure 13(c) show the response of the failing device to a longer pulse (80ns). Since the metal gate, gate dielectric and channel are equivalent to a capacitor, when the gate has more time to charge up, the resistive connection to the gate would have less impact to the voltage that applied to the gate, so the device started to be turned on, but it did not fully turn on before the input dropped after 80ns. Figure 13(d) shows the device can be fully turned on if the input pulsed is increased to 360ns. The slope in the response curve is also consistent with resistive gate defect mode.
Figure 13(a) shows the Pulsed IV result from a passing MOSFET device, (b) shows the response from a failing device when the same pulse (20nS) was given to the gate, 13(c) and (d) show the response of the failing device to longer pulses.

5.2 Capacitance-Voltage (C-V)

An alternative to Pulsed IV probing, the Capacitance-Voltage (C-V) can be also used to differentiate a resistive open gate from passing gate. The sample has been deprocessed to contact layer. For C-V measurement, we use High probes on Source and drain, Low probe on gate, sample chuck is forced floating to minimize parasitic capacitance.

Figure 14 shows the C-V measurements of a PMOS gate capacitance on both passing and failing devices. The black curve shows the C-V characteristic of passing gate for AC frequency at 1MHz, while red and blue curves show the C-V of failing gate for AC frequency at 1MHz and 0.1MHz respectively. For the passing gate, when DC bias is at -1V, the conducting channel is formed for the PMOS, the gate capacitance can be measured from source to gate, therefore the C-V shows a clear increase of capacitance for the negative Vgs side.

For the failing gate, the measured capacitance at 1MHz (red curve) is lower than reference, indicating the gate has difficult to form the conducting channel at high frequency. When measuring the same gate at 0.1MHz, the capacitance at -1V Vgs is higher than that at 1MHz. This is due to the resistive gate takes longer time for the charges to accumulate and dissipate on the failing gate. At higher frequency, the resistive open of the gate has larger impact to the measured capacitance than that at lower frequency.

5.3 Scanning Capacitance Microscopy (SCM)

Another technique that can be used for visualizing the resistive gate defect is Scanning Capacitance Microscopy (SCM). The sample has been deprocessed to contact layer, the gate contact is exposed, while gate remains covered by dielectric. When a conductive probe scans over the gate, a Metal-Oxide-Semiconductor (MOS) system is formed on the sample. The capacitance of the MOS capacitor is a function of majority carrier concentration in the sample. Variations in the probe-sample capacitance are induced using an AC-bias applied between probe and sample. For heavily doped semiconductors, the carriers do not move far from probe, therefore the measured capacitance change is small. While for lightly doped semiconductor, the measured capacitance change is larger. The signal is rectified with a lock-in amplifier, the dC/dV signal can be separated into amplitude and phase data, revealing information about the relative concentration and carrier type.

In the SCM images, Figure 15(a) shows the contact mode topographic image of the sample. For SCM scanning only one probe is used. Figure 15(b) shows the SCM DataX image, the DataX equals to SCM Signal*\cosθ, where θ is the phase angle. In the image, white dotted line circles are the passing gate contacts within the scanned area, while red solid line circle is the failing gate contact. The failing gate contact shows clearly different contrast from all the passing gate contacts. Since the carrier types is known from process and layout information, the contrast is due to different response time of the failing gate to the high frequency AC bias during the scanning.
Conclusion

In this paper, we presented various failure analysis techniques that were used to detect and isolate different types of resistive open defects, with resistance range from 1KΩ to 1MΩ. For defects residing in both FE and BE, we applied these techniques to front-side and backside deprocessed samples. The successful localizations of these defects have been demonstrated and discussed.

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References


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