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FLEXIBLE CIRCUIT BOARD PACKAGE EMBEDDED WITH MULTI-STACK DIES

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ABSTRACT

Miniaturization of electronics modules is always required for various medical applications including wearable technology, such as hearing aids, and implantable devices. Many types of high-density packaging technologies, such as package-on-package, bare-die stack, flex folded package and Through Si Via (TSV) technologies, have been proposed and used to fulfill the request. Among them, embedded die technology is one of the promising technologies to realize miniaturization and high-density packaging. We have developed WABE™ (wafer and board level device embedded) technology for embedding dies into multilayer flexible printed circuit (FPC) boards. The WABE package is comprised of thin dies (85 μm thickness), multi-layer polyimide, adhesive films and conductive paste. The dies are sandwiched by polyimide films with Cu circuits (FPCs). The conductive paste provides electrical connections between the layers as well as the layer and embedded die. First, each FPC layer is fabricated individually, and via holes are filled with conductive paste, and the dies are mounted on certain layers. Then, all layers undergo a one-step co-lamination process, and they are pressed to cure the adhesive material and conductive paste at the same time. This WABE technology has enabled multiple dies to be embedded by the one-step lamination process. Even if multiple dies are embedded, the footprint of a package can be reduced drastically by embedding multiple dies vertically in stacks. This paper describes the details of the results of fabricating a test vehicle with six embedded dies (three-dies in two stacks side-by-side). The fabricated test vehicle had 14 copper layers with less than 0.9 mm thickness. This paper also reports the results of various reliability testing on the package. These results were obtained by electrical measurements of daisy chain patterns formed between some of the layers. The fabricated test vehicle showed high reliability based on the results of a moisture and heat test and heat-shock test. These results show that the WABE technology to embed multiple dies vertically in polyimide film is one of the most promising packaging technologies to significantly miniaturize electronic circuits such as medical electronics.

Keywords: Chip embedding, Chip stack, Polyimide multilayer, WABE technology, Reliability

INTRODUCTION

Electronic products have been miniaturized constantly and their functionality has also been expanded in various fields. Miniaturization and high functionality are required for medical applications such as wearable and implantable devices as well. To fulfill the requirements, many types of high-density packaging technologies, such as package-on-package, bare-die stack, flex folded package and through Si via (TSV) technologies, have been proposed and actually used. Among a variety of packages, embedded device packages allow much smaller footprints than those of conventional packages [1]. The reason for this lies in the structure, which can accommodate several devices inside the substrate, instead of the surface. Additionally, embedded packages can reduce signal delay and signal noise because electric paths between embedded devices and package terminals are shortened [2]. Fujikura has developed an embedded device package called WABE™ package (wafer and board level embedded device package). This product is produced by combining thin FPC (flexible printed circuit) boards and a back-grinded thin IC (integrated circuit) die and has achieved a thickness of 220 μm as the thinnest package embedded with a single chip [3].

However, in our conventional production method, if additional dies needed to be embedded in the package, the side-by-side structure was employed. The structure still had a challenge in reducing the package footprint. To realize further miniaturization of the package footprint, we have been developing new electronics packaging technology that will take

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WABE package to the next higher level. One of the effective methods is embedding multiple dies into a substrate in a stacked configuration. We have already reported on this embedding technology called Chip-stack WABE™ [4][5][6]. This technology is installed in the mass production of miniaturized medical device shown in Fig. 1.

Furthermore, we have developed a multi-stack die WABE package. The calculation results of the multi-stack die WABE package indicate that the package footprint can be reduced by 75% of that of a conventional package, in which all chips are mounted on the substrate as shown in Fig. 2.

This report describes the structure and production method of the multi-stack die WABE package and the results of reliability tests on test vehicles of the package. The test vehicle contained six dies (three-dies in two stacks side-by-side) and 14 copper layers with less than 0.9 mm thickness. The reliability tests are a moisture and heat test and heat-shock test.

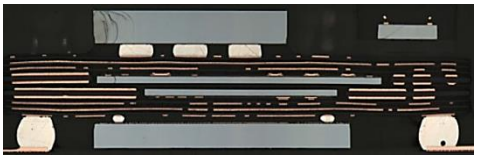

FIGURE 1: Chip-stack WABE used in microminiature electronic module

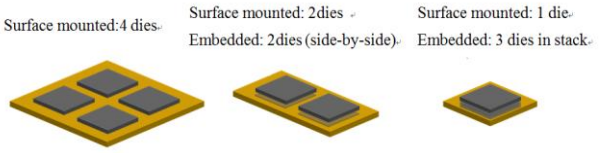

FIGURE 2: Reduction in footprint of multi-stack die WABE package

1.1 Structure of WABE Package

The WABE package structure with one embedded die is shown in Fig. 3. Basically, this package is comprised of a thin die (85 μm thickness), multi-layer polyimide, adhesive films and conductive paste. The die is sandwiched by polyimide films with Cu circuits (FPCs). Two base units of FPCs consist of single-sided FPC boards and a double-sided FPC board. In this fabrication process, all these materials are stacked up and cured in a vacuum press machine only one time (Fig. 3). The conductors of each layer and embedded dies are electrically connected by vias filled with the conductive paste. Multilayer boards embedded with multiple dies in a stacked configuration can be fabricated in the same fabrication method used for a single embedded die package by adding a type of layer called intermediate layer. This layer establishes electrical connections between the upper and lower structures with dies stacked vertically without an additional curing process [7]. The following is the details of the fabrication process for WABE package.

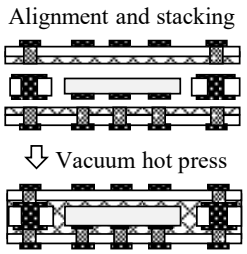

FIGURE 3: Fabrication process flow diagram of WABE package embedded with one die

1.2 Fabrication Process of WABE Package

1.2.1. Single-Sided FPC

Figure 4 is the fabrication process flow diagram of a single-sided FPC board. First, a copper circuit is formed on the copper clad laminate (CCL). Then, the adhesive film is laminated onto the CCL, and via holes are formed by laser drilling on the opposite side. This adhesive and conductive paste filled in these via holes connect FPC layers and dies mechanically and electrically during the curing process.

1.2.2. Double-sided FPC

Figure 5 is the production process flow diagram of a double-sided FPC board. This layer has roles as both an interlayer connector and a spacer for the embedded die. After forming via openings by a UV-laser drilling process, the vias of the board are filled with copper by electrolytic plating. Then circuits are fabricated by a copper etching process. Finally, cavities to hold dies are opened by a punching process or a laser drilling process.

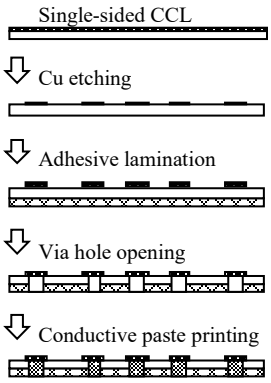

FIGURE 4: Fabrication process flow diagram of single-sided FPC

1.2.3. Intermediate Layer

In WABE packages with multi-stack embedded dies, the intermediate layer has a unique structure to connect facing conductors of single-sided FPCs or double-sided FPCs. Figure 6 is the fabrication process flow diagram of the intermediate layer. Adhesive films are laminated on both sides of the polyimide film. After forming through holes by a laser drilling process, the holes are filled with a conductive paste. This board is used as the unit layer that connects embedded die structures vertically.

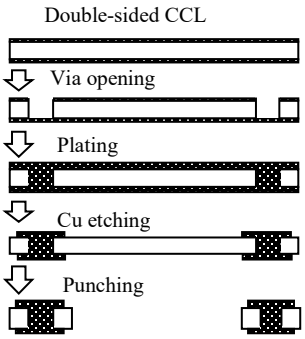

FIGURE 5: Fabrication process flow diagram of double-sided FPC

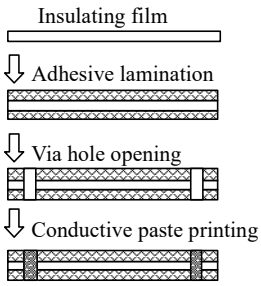

FIGURE 6: Fabrication process flow diagram of intermediate layer

1.2.4. Embedded Die

Figure 7 is the process flow diagram of stacking and curing of a multi-stack die WABE package. The die terminals are redistributed with additional layers called RDLs (redistributed layers) by a wafer-level packaging (WLP) process to match their pitch to that of the FPC boards. Then the RDLs are formed on the dies, and these dies are thinned down to 85 μm by back grinding. Each FPC layer is fabricated individually, and the dies are mounted on certain layers. Then, all layers undergo a one-step lamination process, and they are pressed and heated simultaneously. During the time, the adhesive melts and fills the gaps between the interlayers and the space around embedded dies before being cured, and the metal components in the paste alloy with the copper pads of FPCs and embedded dies. This unique process for making WABE packages is called co-lamination process. This process has advantages in fabricating each FPC layer at the same time and stacking known good layers and dies over conventional build-up methods, and this can save fabrication lead times and costs. After this process, the surface is covered with solder resist and the terminals are coated with gold or an OSP (organic solderability preservative) for protection.

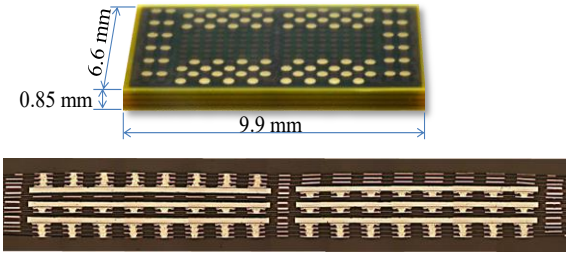

FIGURE 8: Test vehicle of multi-stack die WABE with six dies

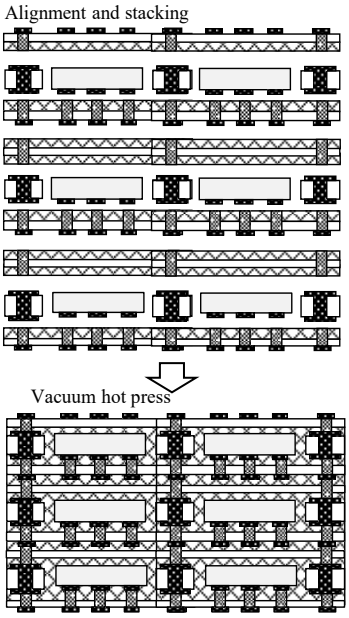

FIGURE 7: Fabrication process flow diagram of multi-stack die WABE package

1.3. Structure of Evaluation Test Vehicle

The test vehicle for evaluation is shown in Fig. 8. The fabricated test vehicle contains six dies in two stacks, each of which accommodates three dies, side by side. The fabricated test vehicle has 14 copper layers and the thicknesses of them are less than 0.9 mm. The specifications described in Table 1 cover the number of the layers, the module size, and the embedded die size. Figure 9 shows the electric paths of the test vehicle. The paths of A are daisy-chained and pass through each die. The paths of B pass through top to bottom but not through dies.

TABLE 1: Specifications of the Test Vehicle

Item	Spec
Wiring layer number	14
Module size	9.9 x 6.6 mm, 850 μmt
Embedded chip size	3.2 x 3.2 mm, 85 μmt

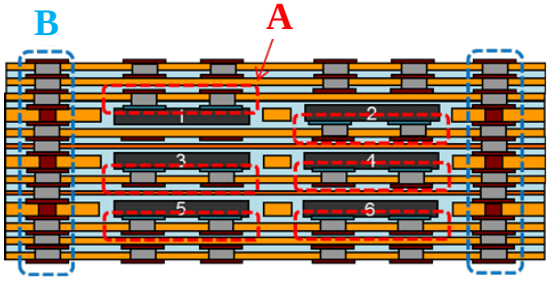

FIGURE 9: Electrical paths of multi-stack die WABE package

1.4. Test Procedure and Results

The resistances of the test vehicle were measured to evaluate the reliability of the vias because the interconnection vias were prone to undergo thermal stress caused by temperature changes.

First, we measured the initial resistance of the daisy-chained circuits. Moisture sensitivity level 3 test of the JEDEC (Joint Electron Device Engineering Council) standard was done before each test as preconditioning. The environmental tests included a thermal cycle test (-40 deg C, 30 min/125 deg C, 30 min, 500 cycle), high temperature storage test (85 deg C, 85%RH, 1000 hours) and unbiased highly accelerated stress test (130 deg C, 85%RH, 336 hours) [8]. The criteria of the environmental tests included appearance according to the standard of IPC-A-600 and open/short within the circuits. The criteria of the appearance consists of delamination, voids and discoloration. The test results are shown in Table 2. They showed that there were no visual defects and no electrically broken vias in the test vehicles.

This concludes that the multi-stack-dies WABE package has sufficient reliability of electrical connections. These results show that the WABE technology to embed multiple dies vertically in polyimide film is one of the most promising packaging technologies.

1.5. Conclusion

In this paper, we present the packaging technology to embed multi-stack dies based on WABE^{TM} technology, which has enabled multiple dies to be integrated by the one-step co-lamination process. The fabricated test vehicle contains six dies in two stacks, each of which accommodates three dies, side by side. The thicknesses of the overall package is less than 0.9 mm. To confirm the reliability of the test vehicles, we have performed the environmental tests comprising the thermal cycle test, the high temperature storage test and the unbiased highly accelerated stress test. After those tests, the test vehicle showed normal appearance without voids, delamination or discoloration. Furthermore, there were no electrically broken vias in this test vehicle. The above results proved that the multi-stack die WABE package has satisfactory reliability and performance as a package embedded with devices. Our new WABE package will lead a higher-density mounting technology that further promotes the downsizing and increase in functionality of future medical devices.

TABLE 2: Conditions and Results of Reliability Tests

Test item	Condition	n Path A	n Path B	Result
Preconditioning : MSL3	260˚C reflow 3 times, after 30˚C, 60%RH, 192 hours	192	192	pass
High temperature storage test	150 °C, 1000 hours	64	64	Pass
Thermal cycle test	- 40°C ↔ 125°C, 1 hour/cycle, 500 cycles	64	64	Pass
Unbiased highly accelerated stress test	130°C, 85%RH, 336 hours	64	64	Pass

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